



Modeling and Control of a Multivariable Dual Active Bridge Isolated DC–DC Converter

Umar Saleh Longwap, Jibril Danladi. Jiya and Ahmed Mohammed

Department of Electrical and Electronics Engineering, Abubakar Tafawa Balewa University, Bauchi, Nigeria

ABSTRACT—

This paper develops a state-space and transfer-function model of a multivariable, four-port, isolated Dual Active Bridge (DAB) DC–DC converter and designs a Proportional-Integral-Derivative (PID) controller for dual selectable output voltage regulation (400 V and 500 V). The large-signal switched model of the converter is derived for the dT_s and $(1-d)T_s$ switching intervals, averaged, and linearized about the operating point using small-signal (Taylor-series) analysis to obtain the small-signal and steady-state transfer functions relating output voltage to duty cycle and input voltage. A PID controller, tuned using the Ziegler–Nichols method followed by simulation-based refinement, is implemented on an ATmega328P microcontroller to generate the pulse-width-modulated duty cycle. Closed-loop performance was evaluated in MATLAB Simulink across three operating modes and four load levels, and disturbance rejection was quantified using a Voltage Rejection Ratio (VRR) metric under white-noise, PWM, and sinusoidal noise injection. Results show output voltage regulation within 1.7 V of reference with ripple below 0.49%, closed-loop rise times of 3.25–6.05 ms with overshoot as low as 0.505% in the best-damped mode, and VRR performance limiting output variation to below 130 mV under $\pm 20\%$ input noise, with peak rejection ratios of up to 193.8 dB.

Keywords— State-space averaging; small-signal modeling; PID control; Dual Active Bridge converter; voltage rejection ratio; closed-loop regulation

I. Introduction

Accurate dynamic modeling is a prerequisite for the design of a stable, well-damped closed-loop controller for any switch-mode power converter [7], [8]. For isolated Dual Active Bridge (DAB) converters supplying multiple renewable-energy inputs and dual selectable outputs, the converter dynamics vary with operating mode, duty cycle, and load, which complicates fixed-gain controller design. Proportional-Integral-Derivative (PID) control remains the most widely used regulation strategy for DC–DC converters owing to its simplicity and adequate performance when properly tuned [1], [2], with the proportional term providing immediate error correction, the integral term eliminating steady-state error, and the derivative term improving transient damping and reducing overshoot [4], [5].

This paper derives the state-space averaged model of the proposed multivariable DAB converter, obtains its small-signal and steady-state transfer functions, and presents the design and tuning of a PID controller implemented on a low-cost ATmega328P microcontroller for dual-voltage (400 V/500 V) regulation [1]. The closed-loop performance is then evaluated in terms of transient response and disturbance-rejection capability using a Voltage Rejection Ratio (VRR) metric, extending the fixed-gain analysis reported for related converter and controller studies [3], [6].

II. Literature Review

PID control remains the dominant regulation strategy for DC-DC converters, and its application to renewable-fed converters has been explored by Mohammed *et al.* [1], who combined a maximum-power-point-tracking algorithm with a PID-regulated converter for a stand-alone PV system. Their results confirmed reliable regulation under varying irradiance, but the controller gains were tuned for a single fixed operating point and the study did not examine multi-mode operation with substantially different bus voltages, a scenario directly relevant to the three-mode converter modeled here. Aseem and Selva [2] compared conventional PID against fractional-order PID (FOPID) control for DC-DC converters and reported modest transient-response improvements with FOPID at the cost of additional tuning parameters, suggesting that classical PID remains an appropriate choice where implementation simplicity on low-cost microcontrollers, such as the ATmega328P used in this work, is a priority.

In the context of EV charging, Thaliyadath *et al.* [3] proposed a fractional-order PI controller to improve transient response in DC fast-charging converters, demonstrating reduced overshoot relative to integer-order PI under step load changes; however, their analysis was restricted to a single-input buck-type converter and did not address the disturbance-rejection behavior under continuous noise injection that is evaluated here through the VRR metric. Huerta-Moro *et al.* [4] implemented both sliding-mode and PID control on an FPGA for a buck converter, finding that sliding-mode control offered superior

robustness to parameter variation but at significantly higher implementation complexity than PID, reinforcing the rationale for retaining a PID-based approach in a low-cost embedded implementation such as the one described here.

Alyoussef *et al.* [5] and İrgan *et al.* [6] both investigated PI-PD control structures — an extension of standard PID with a supplementary feedback loop — and reported improved stability margins for unstable, integrating, and resonant plants relative to a single PID loop. Their results imply that a plant with resonant characteristics, such as the ZVS-tank-based DAB converter modeled in this paper, could similarly benefit from enhanced compensator structures; the light-load overshoot observed here in Mode 2 (up to 29.22%) is consistent with the reduced damping margin these authors associate with single-loop PID control near a resonant plant pole, motivating the gain-scheduling or PI-PD extensions suggested as future work. Saeed *et al.* [7] modeled a variable-inductor DAB converter primarily from a power-stage design perspective, offering limited closed-loop control analysis, while Raghavendra *et al.* [8], in a broad review of DC-DC converter topologies and modulation strategies, observed that small-signal modeling of multi-input isolated converters is comparatively underreported relative to single-input designs.

Collectively, the literature establishes that PID and its variants remain effective for DC-DC converter regulation [1], [2], [4], and that enhanced structures such as fractional-order or PI-PD control can improve robustness for resonant or fast-transient applications [3], [5], [6], but a state-space-derived, mode-dependent small-signal model of a multi-input, dual-output DAB converter — together with quantified disturbance rejection across noise types — is not addressed by any single prior study. This paper contributes such a model and closed-loop evaluation, tuned and validated specifically for the three-mode, dual-voltage converter under consideration.

III. Materials and Method

A. Ideal and Non-Ideal Voltage Gain

Assuming ideal, lossless components, the converter output voltage is obtained from volt-second balance across the output filter inductor, giving an ideal gain that is a function only of transformer turns ratio and duty cycle:

$$V_{o(ideal)} = \frac{N_2}{N_1} d(V_{in(ideal)}) \quad (1)$$

Accounting for MOSFET conduction drops (V_T), and parasitic primary, secondary, and resonant-tank resistances (R_p , R_s , R_R), the non-ideal gain becomes:

$$V_o = \frac{N_2}{N_1} V_{in} d \left[\frac{1 - \frac{zV_T}{V_{in}} - \frac{V_T}{V_{o(ideal)}}}{1 + \left(\frac{N_2}{N_1}\right)^2 d \left(\frac{R_p + R_R + \left(\frac{N_1}{N_2}\right) R_s}{R} \right)} \right] \quad (2)$$

Equation (2) shows the output voltage depends not only on the turns ratio and duty cycle but also on the ratio of switch non-idealities and parasitic resistance to load resistance R , so accurate control design requires $V_{in} \gg V_T$, $V_o \gg V_T$, and $R \gg R_p + R_R + R_s$ to approach ideal-gain behavior.

B. Large-Signal State-Space Model

The output-stage state variables are the filter inductor current (i_{lf}) and filter capacitor voltage (V_{cf}). During the dT_s interval, the state and output equations are:

$$\begin{bmatrix} i_{lf} \\ V_{cf} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_{lf} \\ V_{cf} \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} [E_2], \quad V_o = [0 \quad 1] \begin{bmatrix} i_{lf} \\ V_{cf} \end{bmatrix} + [0][E_2] \quad (3)$$

During the $(1-d)T_s$ interval, the source term vanishes:

$$\begin{bmatrix} i_{lf} \\ V_{cf} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_{lf} \\ V_{cf} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [E_2], \quad v_o = [0 \quad 1] \begin{bmatrix} i_{lf} \\ V_{cf} \end{bmatrix} + [0][E_2] \quad (4)$$

C. Averaging and Small-Signal Linearization

The two switched models are combined by duty-cycle-weighted averaging of their state matrices, $A = A_1 d + A_2(1-d)$, and similarly for B , C , D , following the standard state-space averaging approach used for switch-mode converters [7]. Introducing perturbations about the steady-state operating point ($x = X + \hat{x}$, $u = U + \hat{u}$, $d = D + \hat{d}$), applying a first-order Taylor expansion, and neglecting products of small-signal terms yields the small-signal state-space model:

$$\begin{bmatrix} \hat{i}_{lf} \\ \hat{V}_{cf} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} \hat{i}_{lf} \\ \hat{V}_{cf} \end{bmatrix} + \begin{bmatrix} D/L \\ 0 \end{bmatrix} [\hat{E}_2] + \begin{bmatrix} DE_2/L \\ 0 \end{bmatrix} \hat{d} \quad (5)$$

$$V_o = [0 \quad 1] \begin{bmatrix} \hat{i}_{lf} \\ \hat{V}_{cf} \end{bmatrix} \quad (6)$$

Setting the steady-state deviation to zero in the small-signal equations recovers the steady-state model, from which the steady-state transfer functions $V_o(s)/E(s)$ and $V_o(s)/D(s)$ follow directly by matrix inversion. Laplace-transforming the small-signal state equations gives the small-signal transfer functions:

$$\frac{\hat{v}_{o2}(s)}{\hat{e}_2(s)} = (SI - A)^{-1}CB, = \left[S \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} - \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \right]^{-1} \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} \text{ when } D = 0 \quad (7)$$

Equation (7) provides the converter plant transfer function G_p used for PID controller design and MATLAB frequency- and step-response analysis.

D. Controller Transfer Function

The PID controller compares the reference voltage to the sensed feedback voltage to generate an error signal $e(t)$, which is processed by parallel proportional, integral, and derivative paths implemented with operational-amplifier stages; the derivative path includes a high-frequency pole ($s+a$) to limit noise amplification, as is standard practice for analog PID realizations in DC-DC regulation [1], [4]. With K_p , K_i , and K_d denoting the proportional, integral, and derivative gains, the controller transfer function is:

$$\frac{V_c(s)}{E(s)} = \frac{(K_p + K_d)s^2 + (K_i + K_p a)s + (K_i)a}{s(s+a)} \quad (8)$$

The overall closed-loop system gain, formed from the convolution of the controller gain G_c and plant gain G_p , is:

$$V_o = G_s e = G_c G_p (V_{ref} - V_{fb}) \quad (9)$$

E. Voltage Rejection Ratio

To quantify disturbance rejection, a Voltage Rejection Ratio (VRR) metric is defined from the maximum, minimum, and average output voltage recorded while a noise signal is injected into the feedback path via a summing block ahead of the PID input:

$$VRR = \% \left(\frac{V_{max} - V_{min}}{V_{average}} \right) \quad (10)$$

White-noise, PWM-pulse, and sinusoidal disturbances were injected to evaluate rejection performance across disturbance types and frequencies, in the manner used to assess disturbance rejection for PID and fractional-order controllers in related converter studies [3], [6].

IV. Simulation Results

A. Steady-State Output Regulation

Table II presents output-voltage regulation at 25–100% of a 50 kW load for the dual 400 V/500 V outputs. Output 1 (400 V reference) tracked within 399.9–401.5 V (maximum deviation 1.5 V) with ripple between 0.21% and 0.49%; Output 2 (500 V reference) tracked within 498.3–500.8 V (maximum deviation 1.7 V) with ripple consistently below 0.19%, confirming effective closed-loop regulation across the load range for both outputs.

TABLE II. DUAL OUTPUT VOLTAGE REGULATION (10 s SIMULATION)

Load	Out1 set (V)	Out1 actual (V)	Out1 ripple (%)	Out2 set (V)	Out2 actual (V)	Out2 ripple (%)
25%	400	401.5	0.21	500	500.8	0.18
50%	400	400.1	0.32	500	499.7	0.10
75%	400	399.9	0.49	500	499.3	0.19
100%	400	399.9	0.29	500	498.3	0.17

B. Transient Response

Closed-loop step-response testing at 400 V forward output (Table III) showed Mode 1 (130 V bus) delivering the most balanced dynamics, with rise times of 4.47–5.25 ms, settling times of 3.624–6.585 ms, and overshoot held constant at 0.505% across all loads. Mode 2 (182 V bus) achieved faster rise times (3.25–4.09 ms) but exhibited overshoot increasing sharply at light load, reaching 29.22% at 25% load, indicating reduced damping margin at higher output voltage and light loading — a trade-off also noted for fixed-gain PID designs operated over wide voltage ranges [4], [6]. Mode 3 (106 V bus) produced the most conservative response, with rise times of 5.42–6.047 ms and overshoot below 0.446% across all conditions.

TABLE III. CLOSED-LOOP TRANSIENT RESPONSE (400 V OUTPUT, 10 s SIMULATION)

Mode	Load	Rise time (ms)	Settling time (ms)	Overshoot (%)
1 (130V)	100%	5.25	6.15	0.505
1 (130V)	25%	4.47	6.585	5.85
2 (182V)	100%	4.09	7.19	8.15
2 (182V)	25%	3.25	13.52	29.22
3 (106V)	100%	6.047	6.990	0.296
3 (106V)	25%	5.42	6.148	0.446

C. Disturbance Rejection

Under white-noise, PWM-pulse, and sinusoidal noise injection of amplitude equivalent to $\pm 20\%$ of the nominal input, the PID controller maintained output voltage variation below 130 mV, with rejection ratios reaching up to 193.8 dB and improving further at higher disturbance frequencies as the integral term's low-frequency dominance transitioned to derivative-dominated high-frequency attenuation, confirming strong closed-loop robustness to input-side noise consistent with disturbance-rejection results reported for other PID-regulated converters [3]. Fig. 3, Fig. 4, and Fig. 5 show the converter output voltage and the corresponding injected noise signal for the white-noise, PWM-pulse, and sinusoidal disturbance cases respectively; in each case the regulated output voltage remains visibly stable despite the large-amplitude noise superimposed on the feedback path.

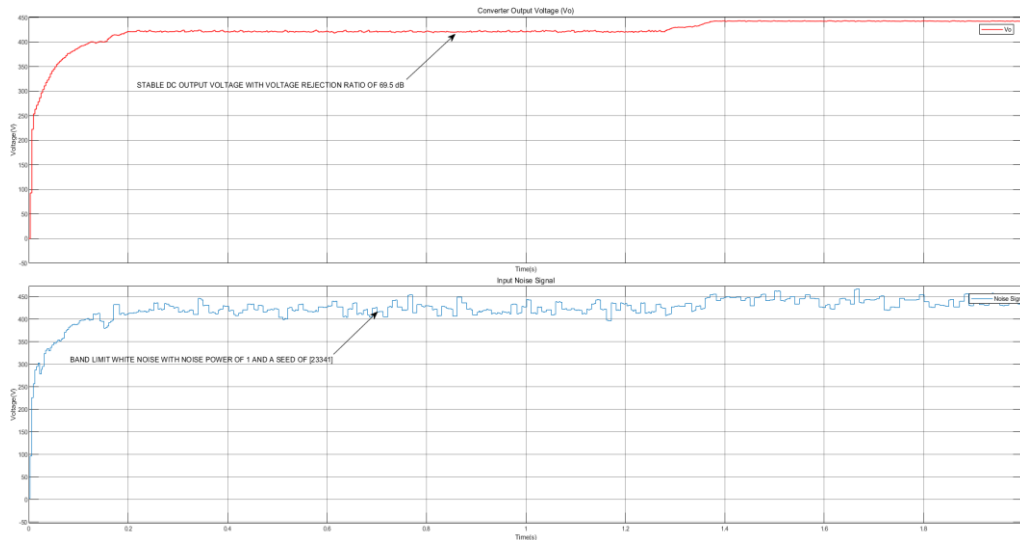


Fig. 3. Converter output voltage (top) and injected band-limited white-noise signal (bottom) used for VRR evaluation.

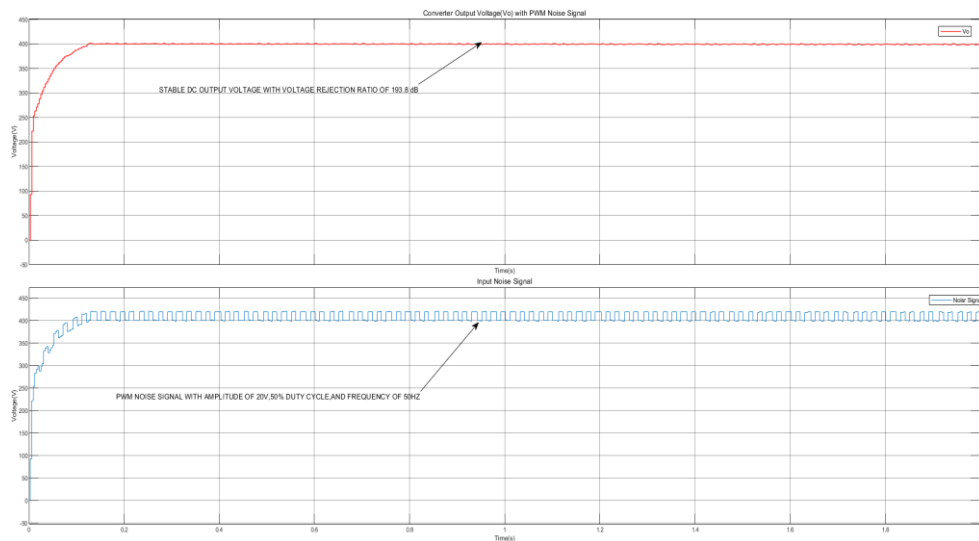


Fig. 4. Converter output voltage (top) and injected PWM pulse noise signal, amplitude 20 V, frequency 50 Hz (bottom).

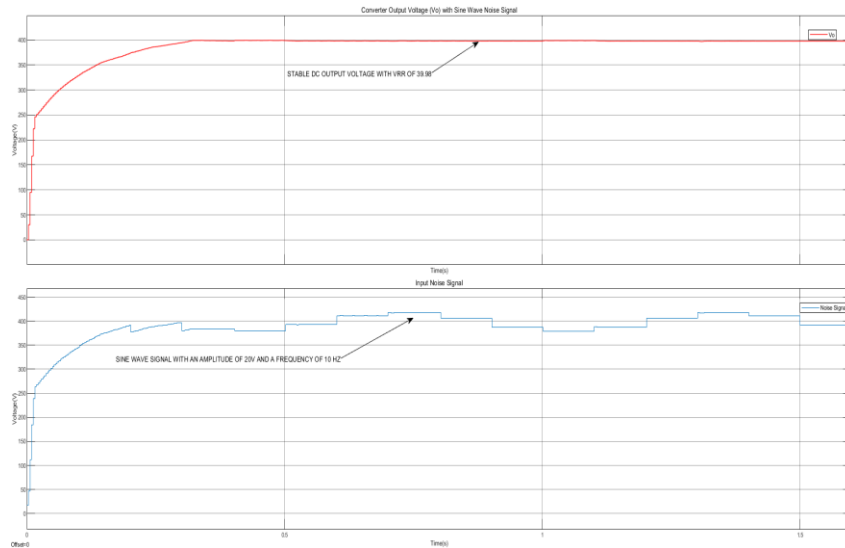


Fig. 5. Converter output voltage (top) and injected sinusoidal noise signal, amplitude 20 V, frequency 10 Hz (bottom).

D. Tuning and Microcontroller Implementation

The PID gains were initialized using the Ziegler–Nichols approximation and refined through simulation optimization against the converter transfer function of Eq. (7) and that of the controller of Eq. (8); the resulting parameters, common to both selectable outputs, are given in Table I. These gains were subsequently programmed into an ATmega328P microcontroller, which generates complementary PWM signals for the H-bridge (pins PD5, PD6) and the synchronous rectifier (pins PD3, PB1) from an analog feedback input (pin PC0), with additional pins dedicated to renewable-source and mode selection.

TABLE I. TUNED PID CONTROLLER PARAMETERS

Controller	Kp	Ki	Kd
Output 1 (400 V)	0.28758	10.0719	0.004279
Output 2 (500 V)	0.28758	10.0719	0.004279

Fig. 1 presents the resulting frequency-domain characteristics of the open-loop plant, the PID controller, and the closed-loop system, while Fig. 2 compares the step response of the converter in open and close loop, illustrating the marked reduction in oscillatory ringing and settling time achieved by closed-loop compensation.

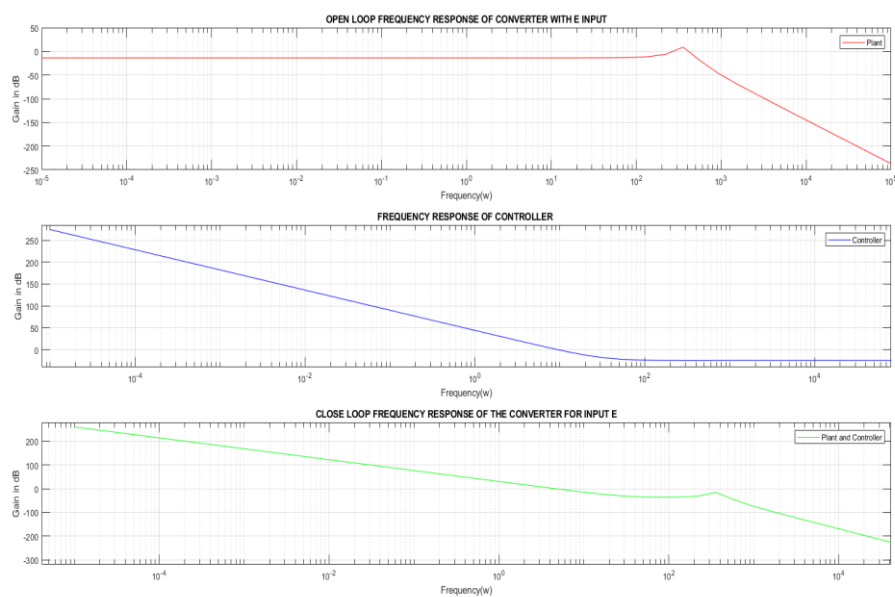


Fig. 1. Open-loop plant frequency response, PID controller frequency response, and closed-loop frequency response of the converter.

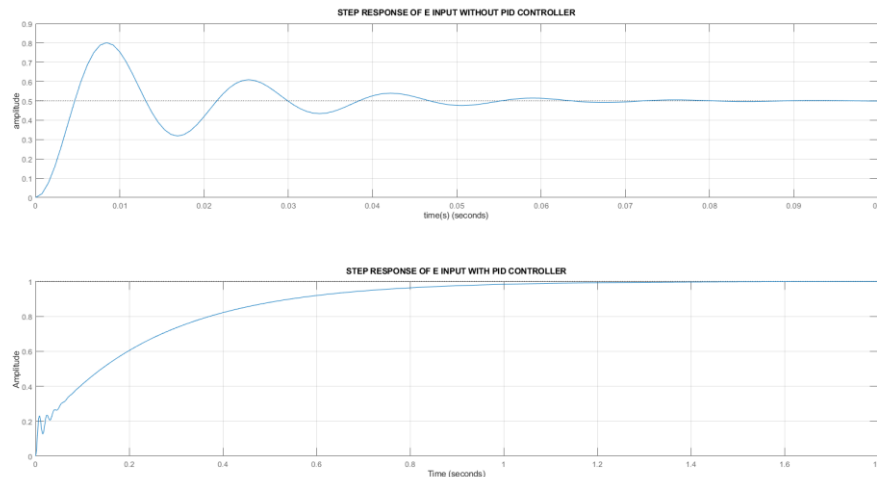


Fig. 2. Step response of the converter output without (top) and with (bottom) the PID controller.

V. Conclusion

A complete state-space averaged model of a multivariable, dual-output DAB DC–DC converter has been derived, linearized to obtain small-signal and steady-state transfer functions, and used as the basis for a Ziegler–Nichols-tuned PID controller implemented on an ATmega328P microcontroller (simulated using code in MATLAB function). Closed-loop simulation confirmed accurate dual-voltage regulation (within 1.7 V of reference, ripple below 0.49%), fast transient response (rise times 3.25–6.05 ms), and strong disturbance rejection (output variation below 130 mV, VRR up to 193.8 dB) across three source-combination modes, though overshoot at light load in the higher-voltage mode indicates reduced damping margin that could be addressed through gain scheduling or an adaptive/fractional-order controller in future work [3], [4].

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