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Design and Transient Analysis of a Low-Power High-Data-Activity Dual-Edge Triggered Flip-Flop Using GPDK 90 nm Technology

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ABSTRACT

Flip-flops are essential sequential elements in digital integrated circuits, where their power consumption, speed, and operational reliability significantly influence overall system performance. Dual-edge triggered flip-flops provide an alternative to conventional single-edge triggered designs by capturing input data at both rising and falling edges of the clock signal. This work presents the transistor-level implementation and transient analysis of a Low-Power High-Data-Activity Dual-Edge Triggered Flip-Flop (LPHD-DET FF) using GPDK 90 nm technology. The design is implemented using Cadence Virtuoso, following the latch-multiplexer-based True Single-Phase Clocking (TSPC) architecture. The circuit is evaluated through transient simulation by applying clock and data input signals and observing the corresponding output response. The simulation waveforms are analyzed to examine the functional behaviour of the flip-flop under the applied input conditions. This implementation study provides a basis for further evaluation of its power consumption, propagation delay, and energy efficiency in CMOS-based digital applications.

Keywords: Dual-Edge Triggered Flip-Flop, LPHD-DET, TSPC, GPDK 90 nm, Cadence Virtuoso, CMOS, Transient Analysis.

1.INTRODUCTION

Flip-flops are essential components of sequential digital circuits and are widely used in processors, registers, counters, and data storage systems. The power consumption, speed, and area of flip-flops have a considerable influence on the overall performance of digital integrated circuits. As modern VLSI systems demand higher performance with lower energy consumption, the development of efficient flip-flop architectures has become an important area of research.

Conventional Single-Edge Triggered (SET) flip-flops capture input data only at one transition of the clock signal, either the rising edge or the falling edge. In comparison, Dual-Edge Triggered (DET) flip-flops capture data at both rising and falling edges of the clock. Therefore, a DET flip-flop can achieve the same data throughput using half the clock frequency required by a conventional SET flip-flop. This characteristic can help reduce the power consumed by clock distribution networks.

True Single-Phase Clocking (TSPC) is an effective technique used in high-speed digital circuit design. It operates using a single clock signal to control the internal stages of a sequential circuit. This approach avoids the requirement for separate complementary clock signals and can simplify the clocking structure. Combining TSPC with dual-edge triggering provides an effective approach for designing high-performance sequential elements.

In the existing research, Yugal Kishore Maheshwari and Manoj Sachdev presented two low-power, low-energy, static and contention-free TSPC dual-edge triggered flip-flop architectures based on a latch-multiplexer methodology. These architectures are named Low-Power at Low Data Activity (LPLD-DET) and Low-Power at High Data Activity (LPHD-DET). The proposed architectures are designed to address different data activity conditions while reducing unnecessary internal switching activity [1].

The present work focuses on the transistor-level implementation and transient analysis of the LPHD-DET flip-flop architecture using GPDK 90 nm technology. The circuit is implemented and simulated using Cadence Virtuoso. Clock and data signals are applied to evaluate the output response of the designed flip-flop. The obtained transient waveforms are examined to verify the functional operation of the circuit. This implementation also provides a foundation for evaluating important performance parameters such as power consumption, propagation delay, and energy efficiency.

2.REVIEW OF EXISTING TSPC DUAL-EDGE TRIGGERED FLIP-FLOPS

Dual-edge triggered flip-flops have been developed using different circuit techniques to improve the performance of sequential digital systems. Some commonly studied approaches include pulsed-latch-based, C-element-based, and latch-multiplexer-based architectures. Each technique has different characteristics in terms of circuit complexity, power consumption, timing behaviour, and reliability.

2.1 Pulsed-Latch-Based Architecture

Pulsed-latch-based dual-edge triggered flip-flops use pulse-generating circuits to produce triggering pulses at both rising and falling clock edges. These pulses control the operation of the latches and allow data to be captured at both clock transitions. However, generating accurate pulse widths is challenging because pulse characteristics can vary with process, voltage, and temperature conditions. Additional pulse-generation circuitry can also increase power consumption and circuit area.

2.2 C-Element-Based Architecture

C-element-based flip-flops use C-elements to control data storage and state transitions. When the inputs of a C-element are identical, its output follows the corresponding input. When the inputs differ, the previous output state is maintained. Although this technique provides useful storage behaviour, contention between internal circuit paths can affect power consumption and reliability. Careful transistor-level design is therefore necessary.

2.3 Latch-Multiplexer-Based Architecture

The latch-multiplexer approach uses two level-sensitive latches controlled by opposite clock phases and a multiplexer at the output. One latch captures data while the other maintains its previous state. The output multiplexer selects the appropriate stored data according to the clock signal. This arrangement enables data capture at both clock edges and provides an alternative to pulse-generation-based architectures.

2.4 TSPC-Based Dual-Edge Triggered Architecture

True Single-Phase Clocking (TSPC) is used to simplify clock control by operating the internal circuit stages with a single clock signal. TSPC-based dual-edge triggered designs can avoid problems associated with overlapping complementary clock phases. However, their transistor count, internal switching activity, and voltage-level behaviour must be carefully considered when designing low-power circuits.

These existing approaches provide the background for the development of more efficient dual-edge triggered flip-flops. The LPHD-DET architecture considered in this work follows the latch-multiplexer-based TSPC approach and is implemented using GPDK 90 nm technology in Cadence Virtuoso [1].

3. LPHD-DET ARCHITECTURE AND CIRCUIT IMPLEMENTATION

The Low-Power High-Data-Activity Dual-Edge Triggered Flip-Flop (LPHD-DET) is a sequential circuit designed to capture input data at both rising and falling transitions of the clock signal. The architecture is based on a latch-multiplexer configuration using True Single-Phase Clocking (TSPC). It provides an approach for reducing unnecessary internal switching activity during circuit operation.

3.1 Architecture Overview

The LPHD-DET architecture consists of clock-controlled latch stages and an output selection network. The latch stages store input data during their respective clock phases, while the output selection network provides the appropriate stored data at the output. By using both clock transitions, the circuit performs dual-edge triggered operation.

The architecture is intended for applications involving higher data activity, where internal switching behaviour has an important influence on power consumption. The latch-multiplexer arrangement provides the required data transfer between internal storage nodes and the output.

3.2 Working Principle

The operation of the LPHD-DET flip-flop depends on the clock signal and the input data. During one clock phase, one latch captures the input data while the other maintains its previously stored value. During the opposite clock phase, the roles of the latch stages are exchanged.

The output selection network responds to the clock transition and selects the appropriate stored data. Consequently, the output can be updated at both rising and falling edges of the clock signal. This enables dual-edge triggered operation without requiring two independent clock inputs.

3.3 Circuit Implementation Using GPDK 90 nm Technology

The LPHD-DET flip-flop is implemented at the transistor level using Cadence Virtuoso with GPDK 90 nm technology. The design follows a latch-multiplexer-based True Single-Phase Clocking (TSPC) architecture, which enables data capture at both rising and falling transitions of the clock signal. The implementation consists of interconnected NMOS and PMOS transistors arranged to perform the required data storage, clock-controlled switching, and output selection operations.

The circuit is designed using multiple transistor networks that collectively perform the dual-edge triggered operation. The internal latch stages are responsible for temporarily storing the input data during their respective clock phases. These stages operate in coordination with the clock signal so that one stage captures the incoming data while the other maintains its previously stored state. This arrangement supports continuous data transfer between the internal storage nodes and the output stage.

The output selection network plays an important role in determining the final output of the flip-flop. Depending on the clock transition, the appropriate internal data is selected and transferred to the output. This enables the circuit to respond to both rising and falling edges of the clock signal. The use of a single-phase clocking approach simplifies the clock control requirements and avoids the need for separate external complementary clock inputs.

The transistor-level schematic is developed in the Cadence Virtuoso schematic editor by connecting the individual MOS transistor terminals according to the intended circuit architecture. The NMOS and PMOS devices are interconnected through their gate, source, drain, and bulk terminals to establish the required logic and storage functions. The internal nodes are connected through the respective transistor networks to achieve the desired signal propagation and output response.

After completing the schematic, clock and data input sources are connected to the circuit to establish the required simulation conditions. The clock signal controls the operation of the internal latch stages, while the data input provides the information to be captured and stored. The output terminal is monitored to examine the response of the designed flip-flop under different input conditions.

The implemented circuit is subsequently evaluated through transient analysis in Cadence Virtuoso. The resulting waveforms are used to examine the relationship between the clock, data, and output signals and to verify the functional behaviour of the LPHD-DET flip-flop. This transistor-level implementation using GPDK 90 nm technology provides a foundation for further investigation of important circuit characteristics, including power consumption, propagation delay, and energy efficiency.

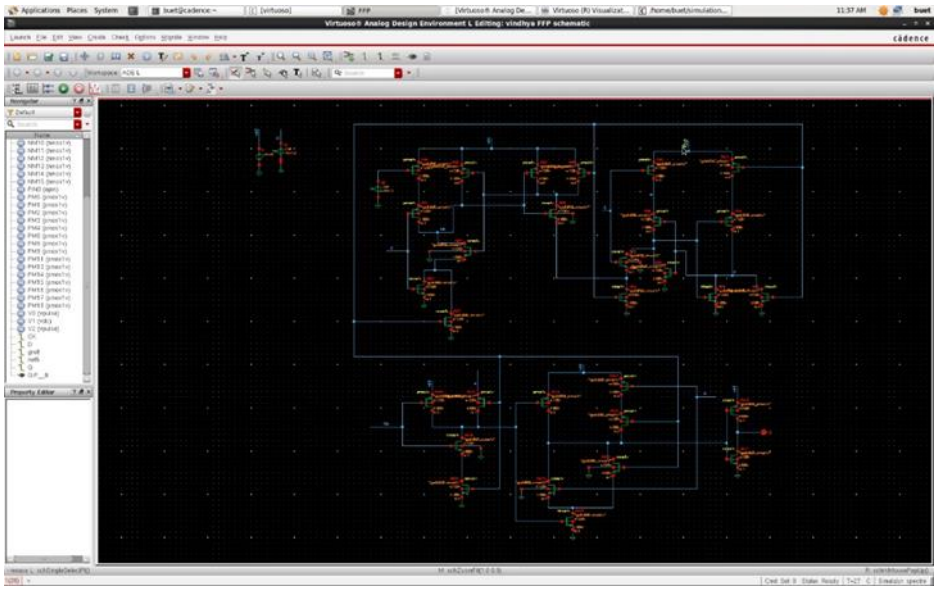


Figure 3.3: Transistor-level schematic of the implemented LPHD-DET flip-flop using GPDK 90 nm technology.

3.4 Simulation Setup

Transient analysis is performed in Cadence Virtuoso to examine the functional operation of the implemented flip-flop. A periodic clock signal and a varying data input signal are applied to the circuit. The output response is observed to determine whether the circuit captures data according to the applied clock transitions.

The clock, data, and output waveforms are used to study the relationship between the input signals and the resulting output behaviour. These simulation results form the basis for the functional verification and performance evaluation presented in the following section.

4. SIMULATION RESULTS AND ANALYSIS

The LPHD-DET flip-flop implemented using GPDK 90 nm technology is evaluated through transient analysis in Cadence Virtuoso. The simulation is performed to examine the functional response of the circuit under different clock and data input conditions. The clock signal (CK), data input (D), and output signal (Q) are observed to understand the relationship between the applied inputs and the resulting output response.

4.1 Transient Simulation

Transient analysis is carried out by applying periodic clock and data signals to the implemented circuit. The clock signal controls the switching operation of the internal latch stages, while the data input provides the information to be stored. The output waveform is monitored over the simulation period to examine the response of the flip-flop.

The simulation results are displayed as voltage waveforms with respect to time. These waveforms provide information about the switching behaviour of the input and output signals and help evaluate the functional operation of the designed circuit.

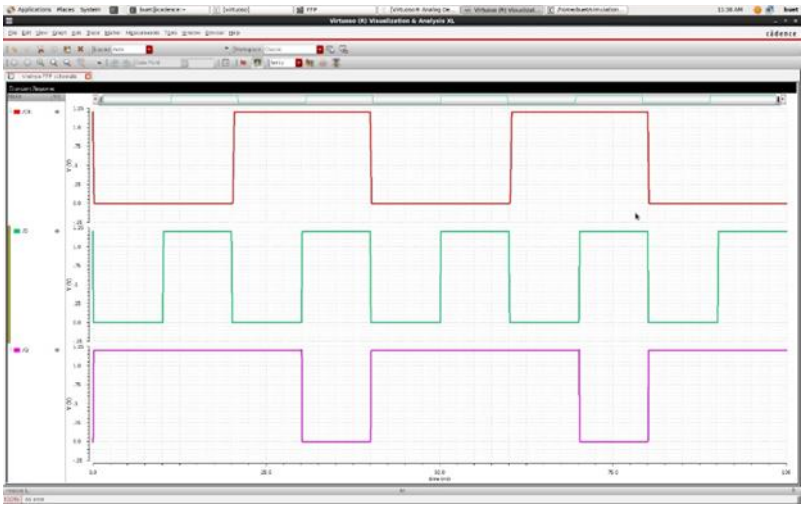


Figure4.1: Transient simulation waveforms of the LPHD-DET flip-flop showing clock (CK), data (D), and output (Q) signals.

4.2 Analysis of Clock, Data and Output Waveforms

The clock waveform represents the periodic control signal applied to the LPHD-DET flip-flop. The data waveform represents the input information supplied to the circuit. The output waveform indicates the stored data obtained from the flip-flop.

By observing the clock, data, and output waveforms together, the functional relationship between the signals can be examined. The output response is compared with the input data transitions and clock edges to verify the intended dual-edge triggered behaviour.

4.3 Functional Verification

The transient simulation results are used to examine whether the implemented LPHD-DET flip-flop responds to both rising and falling transitions of the clock signal. The output waveform is analyzed in relation to the applied clock and data inputs.

The observed waveforms provide an initial verification of the functional behaviour of the transistor-level implementation. Further characterization involving power consumption, propagation delay, and energy efficiency is required to quantify the performance of the circuit**.**

5. CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

This work presents the transistor-level design and transient analysis of a Low-Power High-Data-Activity Dual-Edge Triggered Flip-Flop (LPHD-DET) using GPDK 90 nm technology. The proposed circuit is implemented using Cadence Virtuoso, following a latch-multiplexer-based True Single-Phase Clocking (TSPC) architecture.

The designed flip-flop is evaluated by applying clock and data input signals and observing the corresponding output response through transient simulation. The obtained waveforms demonstrate the functional behaviour of the implemented circuit and provide an understanding of its response to the applied clock and data transitions.

The implementation establishes a foundation for further investigation of dual-edge triggered flip-flop designs for sequential digital applications. The study also highlights the importance of transistor-level circuit design and simulation in evaluating the behaviour of CMOS-based sequential circuits.

5.2 Future Scope

The proposed LPHD-DET flip-flop can be further investigated through detailed performance characterization. Future work may include measuring average power consumption, propagation delay, and power-delay product under different operating conditions.

Further optimization can be performed by examining transistor sizing and internal switching activity to improve the overall circuit performance. Post-layout simulation and process, voltage, and temperature (PVT) analysis can also be carried out to evaluate the robustness and reliability of the design.

The design may additionally be explored for integration into high-speed sequential digital systems, registers, and other applications requiring dual-edge data capture.

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