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Simulink Realization of a Communication-Free Fixed-Time Predictive Controller for a Fuel Cell/Battery/Supercapacitor Hybrid Storage System with Constant Power Load

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ABSTRACT—

Fuel cell/battery/supercapacitor hybrid energy storage systems (HESS) are expected to keep a dc bus at its set voltage, hand each source the share of the load power that suits its dynamics, and stay stable when the bus feeds constant power loads (CPLs). This work builds and tests, in MATLAB/Simulink, the communication-free controller published recently in IEEE Transactions on Smart Grid, which pairs autonomous fixed-time model predictive control (FxTMPC) and fixed-time disturbance observers (FxTDO) with decentralized hybrid droop control (DHDC). The simulated plant has a boost converter for the fuel cell and two bidirectional buck-boost converters for the battery and supercapacitor, all tied to a 200 V bus with a CPL; each converter is governed by a MATLAB-function controller that runs locally. Reading the simulated waveforms, the bus voltage overshoots by about 0.7 % at start-up, is within 0.05 V of 200 V after roughly 0.2 s, falls by only 0.25 V (0.125 %) when the disturbance arrives at 0.5 s, and is back in band within about 30 ms. The inductor and diode currents are then used to explain what happens to the stored energy during these transients. The findings are in line with the quick, well-damped response claimed by the original authors.

***Index Terms*—Constant power load, decentralized droop control, DC microgrid, fixed-time disturbance observer, hybrid energy storage system, model predictive control.**

I. Introduction

Because dc microgrids need no reactive-power, frequency or phase-synchronization control, they are well suited to connecting fuel cells, renewables, storage and power-electronic loads [1]. In these grids the storage must regulate the bus and take up power mismatches, but each technology covers only part of that job. The fuel cell has high energy density yet slow dynamics and cannot absorb power. The battery is moderately fast but degrades when cycled often. The supercapacitor offers very high power with little stored energy. A hybrid FC/BAT/SC system therefore gives the slowly varying, intermediate and fast components of the load power to the FC, BAT and SC, in that order [2].

When a converter is tightly regulated and feeds a load downstream, it behaves as a constant power load (CPL). Its negative incremental impedance lowers the damping of the source network and can destabilize controllers that were tuned on small-signal models [3]. PI loops have to trade stability margin for speed, and centralized or distributed coordination depends on communication links that limit reliability and scalability [2], [4].

Recently, Zhang *et al.* [1] recently proposed an autonomous fixed-time model predictive controller (FxTMPC). It has three elements: a fixed-time disturbance observer (FxTDO) that estimates the unknown source and load terms; a receding-horizon optimization, solved offline, whose reference trajectory receives fixed-time correction terms; and a decentralized hybrid droop control (DHDC) that gives the FC, BAT and SC terminals a virtual impedance, resistance and capacitance, respectively. Related finite-time and fixed-time controllers can be found in [5]–[9].

Here the architecture of [1] is implemented in MATLAB/Simulink and its bus-voltage, inductor-current and diode-current waveforms are analysed. The paper offers three things: a discrete-time Simulink model of a three-converter HESS in which every converter has its own MATLAB-function controller; numerical figures for voltage regulation during start-up and after a disturbance; and an explanation of the converter current waveforms in terms of the control action, set against the findings of [1].

II. Plant Description and Modeling

A. Power Stage

Three dc/dc converters are connected in parallel across one dc bus, as in Fig. 1 of [1]. A unidirectional boost converter interfaces the FC, and bidirectional buck-boost converters interface the BAT and SC. The bus feeds a resistive load and a CPL. If line impedance is ignored, the power balance of the bus is

$$P_{\mathrm{ofc}} + P_{\mathrm{obat}} + P_{\mathrm{osc}} = P_{\mathrm{load}} \tag{1}$$

where P_{ofc}, P_{obat} and P_{osc} are the output powers of the converters and P_{load} is the total load power, CPL included.

B. Averaged Converter Model

For converter $i \in \{\mathrm{fc}, \mathrm{bat}, \mathrm{sc}\}$, the averaged model reads

$$L_{\mathrm{i}}\, \mathrm{d}i_{\mathrm{Li}}/\mathrm{d}t = v_{\mathrm{si}} - (1 - \mu_i)v_{\mathrm{oi}} \tag{2}$$

$$C_i \, dv_{oi}/dt = (1 - \mu_i) i_{Li} - P_{oi}/v_{oi} \quad (3)$$

where L_i, C_i, μ_i, i_{Li}, v_{oi}, v_{si} and P_{oi} are, respectively, the inductance, capacitance, duty cycle, inductor current, output voltage, input voltage and output power. The term P_{oi}/v_{oi} makes the plant nonlinear and, with a CPL, non-minimum phase when the output voltage itself is the regulated variable. Following [1], the stored energy

$$x_{1i} = 0.5 \, L_i i^2_{Li} + 0.5 \, C_i v^2_{oi} \quad (4)$$

is used as the controlled state. Its time derivative, $\dot{x}_{1i} = v_{si} i_{Li} - P_{oi}$, is linear in the unknown power, so the plant becomes a chain of integrators driven by an intermediate control γ_i and an unmeasured disturbance $u_{1i} = -P_{oi}$. Forcing x_{1i} to its reference x^*_{1i} to its reference regulates the output voltage indirectly and keeps the non-minimum-phase dynamics out of the loop.

III. Controller Design

A. Fixed-Time Observer for Lumped Disturbances

The FxTDO of [1] follows the Brunovsky-system observer of [7] and estimates, for every converter, the output power u_{1i} and the input voltage u_{2i}, together with their derivatives. Its nonlinear terms have exponents $m_i \in (0.8, 1)$ and n_i so the estimation error converges within a time bound that is independent of the initial error. Since the estimates are fed forward to the controller, no dedicated sensors for output power or input voltage are needed.

B. Predictive Law with Fixed-Time Terms

With tracking errors $z_{1i} = x_{1i} - x^*_{1i}$ and $z_{2i} = \dot{z}_{1i}$, the receding-horizon cost over a horizon T_{si} is minimized offline by predicting the error with a third-order Taylor series, which yields the closed-form law

$$\gamma_i = -(15/T^2_{si}) z_{1i} - (6/T_{si}) z_{2i} \quad (5)$$

This law is globally asymptotically stable, although the convergence time is infinite. For fixed-time convergence, [1] appends power terms taken from the arbitrary-order integral system of [8]:

$$\gamma_i = -k_{1i} z_{1i} - k_{2i} z_{2i} - \Sigma_h [k_{hi} \mathrm{sig}^{\alpha hi}(z_{hi}) + k_{hi} \mathrm{sig}^{\beta hi}(z_{hi})] \quad (6)$$

where $\mathrm{sig}^a(z) = \mathrm{sign}(z)|z|^a$, $\alpha_{hi} = 2\alpha/(2-(h-1)(1-\alpha))$, $\beta_{hi} = 2\beta/(2-(h-1)(1-\beta))$, $\alpha \in (0.8, 1)$ and $\beta \in (1, 1.2)$. The closed loop is a second-order integral chain, so its settling time has an upper bound that is independent of the initial state.

C. Decentralized Hybrid Droop Layer

DHDC shifts each converter's voltage reference by an amount that depends only on that converter's own estimated output current:

$$v^*_{ofc} = v_{oref} - R_{vfc} \hat{\imath}_{ofc} + (R_{vfc}/L_{vfc}) \int (v_{oref} - v_{ofc}) d\tau \quad (7)$$

$$v^*_{obat} = v_{oref} - R_{vbat} \hat{\imath}_{obat} \quad (8)$$

$$v^*_{osc} = v_{oref} - (1/C_{vsc}) \int \hat{\imath}_{osc} d\tau \quad (9)$$

These references act as a virtual impedance at the FC, a virtual resistance at the BAT and a virtual capacitance at the SC. All units see the same bus voltage, so the load current is divided by a second-order low-pass filter $G_{fc}(s)$, a band-pass filter $G_{bat}(s)$ and a high-pass filter $G_{sc}(s)$. Consequently the steady-state load current comes only from the FC, the BAT supplies the middle frequency band and the SC absorbs fast transients. The droop parameters are those of [1], for cut-off frequencies of 0.5 Hz and 2.0 Hz and a damping ratio $\xi = 1.24$.

IV. Simulink Implementation

Fig. 1, adapted from Fig. 3 of [1], was realized in MATLAB/Simulink with Simscape Electrical components and simulated with the powergui discrete solver at a fixed 1 µs step. The model has three converter stages on one shared bus:

FC stage. A 100 V source E_1 feeds a boost converter with inductor resistance R_L, an IGBT switch, a series diode and an output capacitor. Inductor current i_{L1}, output voltage v_{C1}, diode current and switch current are sensed by measurement blocks and passed on through From/Goto tags.

BAT and SC stages. Two bidirectional buck-boost converters, each with a series inductor (R_{L1}, R_{L2}, R_{L3}, R_{L4} parasitics), a complementary IGBT pair driven via a NOT block, an output capacitor and a source labelled E_2 (220 V). The signals taken are v_{C2}, i_{L2} and v_{C3}, i_{L3}.

Controllers. Each converter has a dedicated MATLAB-function block, boost_controller for the FC and buckboost_controller for the BAT and SC. The block receives the sampled capacitor voltage V_c and inductor current i_L (via zero-order holds) and outputs the duty cycle d, which drives a PWM generator. Controllers do not communicate with each other, so the scheme remains decentralized.

Load and measurement. A constant power load block and a resistive branch are placed across the common bus. Measured output voltage and diode current pass through moving-average blocks before being logged to the workspace (out.Bus_voltage, out.V1, out.V2) and displayed on scopes.

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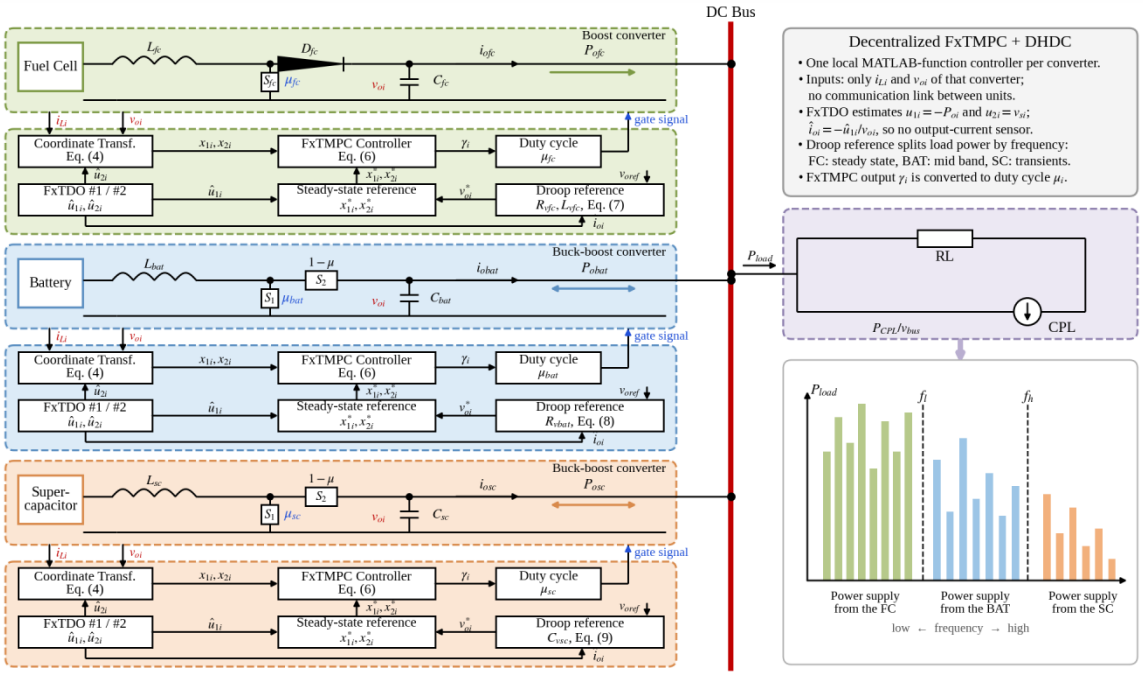


Fig. 1. Structure of the simulated FC/BAT/SC system: each converter (boost for the FC, buck-boost for the BAT and SC) has its own local FxTMPC + DHDC controller, and all three feed a common dc bus loaded by a resistor and a CPL. Adapted from Fig. 3 of [1].

Table I lists the controller and system parameters. Converter and controller values come from the baseline design in [1]; the load rating and disturbance profile are given in Section V.

TABLE I

Simulation and controller parameters

Parameter	Description	Value
E_1	FC source voltage	100 V
E_2	BAT/SC source voltage (as modelled)	220 V
v_{oref}	Reference bus voltage	200 V
L_i, C_i	Converter inductance / capacitance	1 mH / 940 µF
f_s	Switching frequency (ref. [1])	20 kHz
T_s	Prediction horizon	0.003 s
α, β	Fixed-time exponents	0.8, 1.2
m_i, n_i	Observer exponents	0.8, 1.2
ξ	Filter damping ratio	1.24
f_l, f_h	Boundary frequencies	0.5 Hz, 2.0 Hz
R_{vfc}, L_{vfc}	FC virtual resistance / inductance	1.4983 Ω, 0.1548 H
R_{vbat}, C_{vsc}	BAT virtual resistance / SC capacitance	0.5 Ω, 0.1791 F
Solver	Discrete, fixed step (powergui)	1 µs

V. Results and Discussion

The simulation lasts 1 s. The converter first goes through start-up from its initial condition, and a disturbance acts at $t = 0.5$ s ([state the load step, e.g. P_CPL from X W to Y W]). Figs. 2–4 are direct model outputs, and the values below are read from the plots, so they are approximate. In Fig. 2 the bus voltage rises from zero to a first peak near 201.4 V (+0.70 %) within about 5 ms, shows a smaller second peak near 200.5 V at roughly 17 ms, then decays monotonically toward 200 V and stays within about 0.05 V (0.025 %) of the reference from approximately 0.2 s on. The small overshoot and absence of sustained oscillation agree with the well-damped second-order integral dynamics set by (6). At $t = 0.5$ s the disturbance causes a single, quickly damped excursion: the voltage falls by about 0.25 V (−0.125 %) to 199.75 V, rises about 0.17 V above the reference to 200.17 V, and re-enters the steady band after 25–30 ms, so the peak-to-peak transient is below 0.5 V (0.25 %) on a 200 V bus. The feed-forward action of the FxTDO is the likely reason: it hands the estimated power change to the predictive law immediately, whereas a PI loop would have to wait for a voltage error to appear. After the transient,

high-frequency ripple on the bus voltage is visibly larger, about ±0.1 V (0.05 %), than before 0.5 s.

At start-up the inductor current in Fig. 3 shows a very large inrush, reaching the 5 A axis limit, which charges the output capacitor; it then holds a plateau of 0.2 A until 0.5 s. When the disturbance occurs the current peaks at about 1.55 A for a fraction of a millisecond, i.e. the controller pushes extra energy into the inductor to support the bus, and then alternates between about 0 and 0.4 A. No sustained current overshoot is needed to restore the bus. The levels of 0, 0.2 and 0.4 A suggest that the plotted quantity is sampled or averaged (zero-order holds and moving-average blocks are used) rather than the instantaneous switching current, and this coarse resolution probably accounts for the extra voltage ripple noted above. In Fig. 4 the diode current is a dense band from 0 to about 0.9 A, characteristic of high-frequency switching, and it looks the same before and after 0.5 s, which indicates an unchanged switching pattern. At 0.5 s there is one spike of about 1.9 A and then roughly 5 ms without visible diode conduction. A possible cause is duty-cycle saturation near its upper limit during the load increase: the switch stays on and charges the inductor with no diode conduction until the energy balance is restored and normal switching resumes.

A. Summary and Comparison with the Base Paper

TABLE II

Performance read from the simulation plots

Quantity	Value (approx.)
Start-up peak voltage	201.4 V (+0.70 %)
Time to within ±0.05 V	≈ 0.2 s
Voltage dip at disturbance	−0.25 V (−0.125 %)
Voltage overshoot at disturbance	+0.17 V (+0.085 %)
Recovery time after disturbance	≈ 25–30 ms
Steady-state voltage ripple (after 0.5 s)	≈ ±0.1 V (0.05 %)
Inductor current (before 0.5 s)	0.2 A
Inductor current spike at 0.5 s	≈ 1.55 A
Diode current band / spike	0–0.9 A / ≈ 1.9 A

Table III compares these observations with [1]. The authors of [1] report bus-voltage variations of about 1 V in their experiments and dips of a few volts for large CPL steps in their comparative tests, where the proposed controller gives the smallest dip among PI, FTBC and FxTMPC. A sub-volt excursion here is consistent with that, although load levels and converter setup are different, which rules out a direct numerical comparison.

TABLE III

QUALITATIVE COMPARISON WITH THE BASE PAPER [1]

Aspect	Base paper [1]	This work
Platform	PLECS and hardware	Simulink, discrete
Regulation target	200 V bus	200 V bus
Controller	FxTMPC + FxTDO + DHDC	Same structure
Voltage dip	≈1 V (experiment)	≈0.25 V
Settling	Set by DHDC cut-off	≈0.2 s start-up; ≈30 ms after step
Communication	None	None

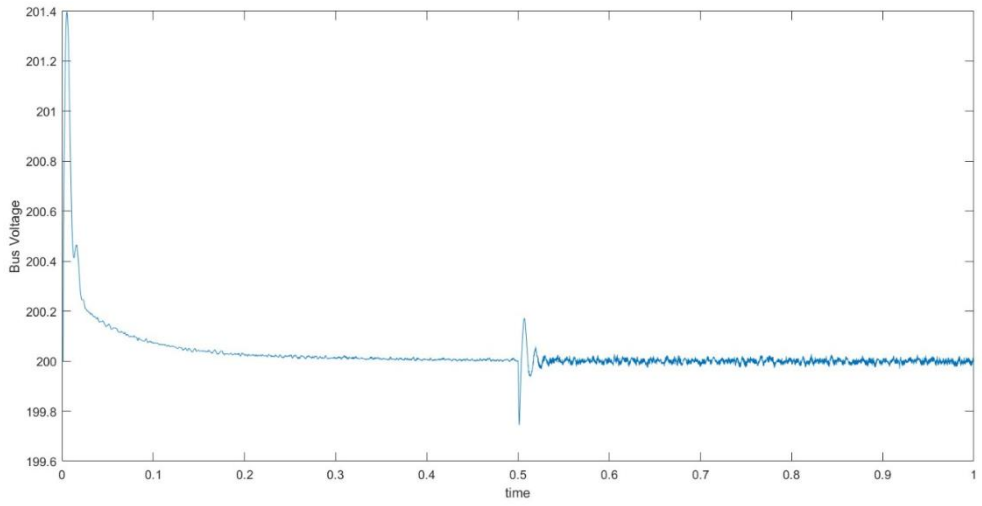


Fig. 2. DC-bus voltage (V) against time (s); reference 200 V, disturbance applied at 0.5 s.

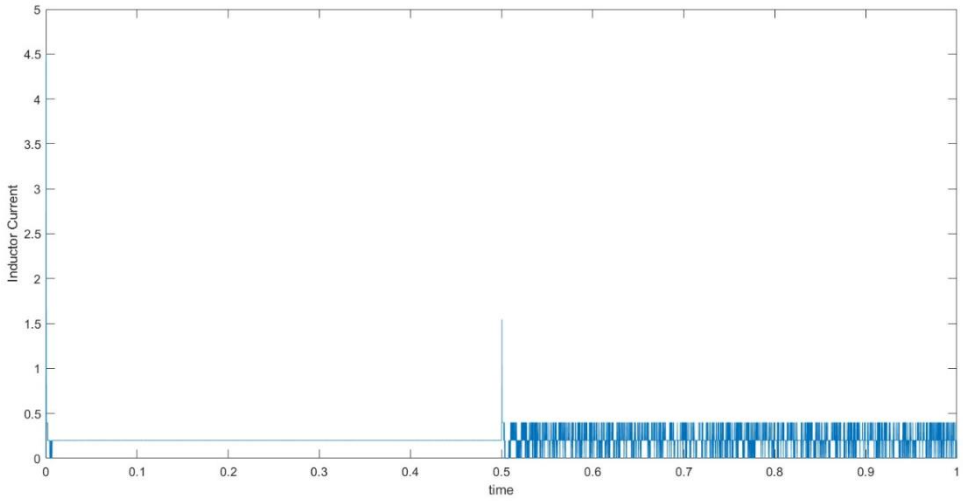


Fig. 3. Boost-converter inductor current (A) against time (s).

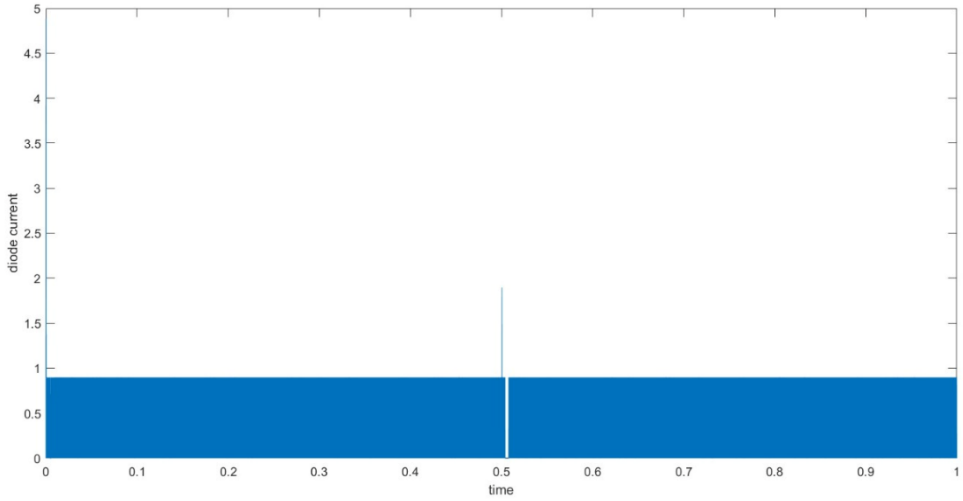


Fig. 4. Boost-converter diode current (A) against time (s).

B. Limitations

Only one operating-point change and one parameter set were simulated. The voltage ripple, the quantized inductor-current signal and the brief gap in diode current at 0.5 s need to be confirmed by logging the instantaneous inductor current at the switching step and by repeating the run with other load steps. Comparisons with PI and FTBC controllers, plug-and-play of single units and parameter-uncertainty tests, all of which appear in [1], were not repeated.

VI. Conclusion

A Simulink model of an FC/BAT/SC hybrid storage system supplying a CPL was built and run under the decentralized FxTMPC + FxTDO + DHDC strategy of [1]. The bus stays at 200 V, with about 0.7 % overshoot at start-up, comes within 0.05 V in roughly 0.2 s and, after a disturbance, deviates by only 0.125 % and recovers in about 30 ms, while the converter currents remain bounded. These results back up the fast, well-damped regulation claimed for the strategy. Planned extensions are the BAT and SC power-sharing waveforms, larger CPL steps, and comparisons with PI control and with unit-disconnection cases.

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