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Design and Analysis of a Telescopic OTA-Based Variable Gain Amplifier as a Adaptive Gain Controller

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A B S T R A C T :

This paper presents the design and simulation-based characterization of a variable gain amplifier (VGA) built around a fully differential telescopic operational transconductance amplifier (OTA) whose gain is set through the gate voltage of its tail transistor, together with an automatic gain control (AGC) loop formed by a MOSFET envelope detector and a differential error amplifier. The circuit is intended for the VGA-I and VGA-Q branches of a 28-GHz vector modulator. Gain-control relations are derived, and it is shown that the sign of the control characteristic must be evaluated at the carrier frequency rather than at DC for the loop to provide negative feedback. Cadence Virtuoso AC simulations of the OTA give a low-frequency differential gain of approximately 74 dB and a gain of 24.99 dB at 28 GHz. Process-corner sweeps (FF, FS, SS, SF) show a gain spread of 4.1 dB at low frequency that narrows to 1.6 dB at 28 GHz, whereas at the FF corner the gain depends strongly on temperature: the low-frequency gain is 2.0, 19.0 and 18.6 dB and the gain at 28 GHz is 1.0, 15.0 and 9.3 dB at −24, 27 and 55 °C. Transistor-width sweeps from 120 nm to 360 nm raise the gain monotonically. An open-loop gain-control sweep moves the 28-GHz gain between 20.1 dB and 31.9 dB over four control settings. The temperature sensitivity at the carrier motivates closed-loop regulation; closed-loop transient verification, the control-voltage-to-gain characteristic, power, noise and linearity are identified as remaining work.

Keywords: automatic gain control, envelope detector, operational transconductance amplifier, process corners, telescopic cascode, variable gain amplifier, 28 GHz.

Introduction

Receivers and transmitters must handle signal amplitudes that vary with propagation distance, interference and operating conditions. A fixed-gain stage cannot serve both weak and strong signals: too little gain under-drives the next block, while too much gain drives it toward compression. A variable gain amplifier (VGA) provides electronically adjustable gain, and an automatic gain control (AGC) loop adjusts that gain from a measurement of the output amplitude so that the signal delivered to the next stage stays within a target range [4], [5]. Such functions are needed in millimetre-wave 5G transmit and receive chains, in which gain and phase accuracy across several signal paths directly affect system performance [1].

This work considers a VGA based on a telescopic OTA, which obtains high gain and speed from a single current path at the cost of reduced output swing and input common-mode range [2]. The gain is controlled by the bias of the tail transistor (MN5, drawn as M13 in the schematic), and an AGC loop made of an amplitude detector and an error amplifier closes the control path. The VGA is the building block of the I and Q branches of a 28-GHz vector modulator (Fig. 1), where each branch is regulated by its own loop so that the amplitude of its component, and therefore the gain and phase accuracy of the combined output, is maintained when input level, supply, temperature or process corner changes.

The contributions of this paper are: (i) a loop-level analysis of the tail-current control scheme that shows why the control polarity must be checked at the carrier frequency; (ii) a description of the detector and error-amplifier circuits with the loop-gain and stability relations that govern them; and (iii) a Cadence characterization of the OTA gain and phase over process corners, transistor widths and temperature together with an open-loop gain-control sweep, with an explicit statement of what these open-loop results do and do not establish.

Background and related work

The telescopic OTA is attractive for high-frequency, low-power amplification because the same bias current flows through the input pair, the cascodes and the loads, but the stacked devices restrict headroom [2]. Choosing transistor operating points systematically, for instance with the gm/ID methodology, is particularly relevant when the bias current is intentionally varied, as it is here [6]. VGAs that exploit the bias dependence of OTA transconductance have been reported, with the caveat that bandwidth, swing and linearity change along with gain [3]. The design of AGC loops involves the interplay between the detector, the control amplifier and the VGA tuning characteristic, whose dynamics determine settling and ripple [4], and complete CMOS AGC amplifiers are evaluated by input dynamic range, output variation, settling time and power [5]. Process variation alters threshold voltage, mobility and parasitic capacitance, and therefore the gain and bandwidth of basic analog blocks, which makes corner analysis necessary even for a nominally well-centred design [7].

Circuit Architecture and Analysis

A. System and Signal Path

Within each VGA branch (Fig. 1) the signal and control path is V_{in} → telescopic OTA → V_{out} → amplitude detector → V_{ENV} → error amplifier (with V_{REF}) → V_{CTRL} → tail-transistor gate. The detector converts the amplitude of the differential output into a slowly varying DC voltage V_{ENV}; the error amplifier compares it with V_{REF}, and its output V_{CTRL} sets the OTA tail current and hence the gain, which closes the loop. The RF input is $v_{RF}(t) = A_{RF}\cos(2\pi f_{RF}t + \phi)$ with f_{RF} = 28 GHz; the detector extracts the amplitude and does not reproduce the carrier.

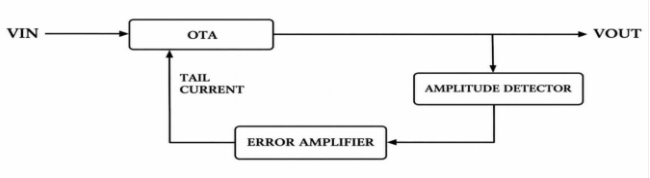


Fig. 1. Inside one VGA branch: telescopic OTA, amplitude detector, error amplifier and the tail-current control path. Each of the VGA-I and VGA-Q branches of the vector modulator contains one such loop.

B. Telescopic OTA Core

The OTA (Fig. 2) is a fully differential telescopic cascode. The input pair M1/M2 is stacked with NMOS cascodes M3/M4 (gate bias V_2), PMOS cascodes M5/M6 and PMOS current-source loads M7/M8 (gate bias V_1); the tail transistor M13 (MN5) is biased by V_3, which is V_{CTRL} in the AGC loop. In saturation, the square-law approximation gives

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D} \qquad (1)$$

which in a nanometre process is only a first-order estimate; the foundry model is the reference. The differential gain and output resistance are

$$A_v \approx g_{m1} R_{out} \qquad (2)$$

$$R_{out} \approx [g_{m3} r_{o3} r_{o1}] \parallel [g_{m5} r_{o5} r_{o7}] \qquad (3)$$

so that the cascodes multiply the output resistance of the input and load devices by their intrinsic gains. Five devices (M13, M1, M3, M5, M7) are stacked between the rails, so the supply must accommodate their saturation voltages plus the output swing, and the input common-mode level must be at least $V_{GS1} + V_{DS,sat13}$ to keep the tail device saturated.

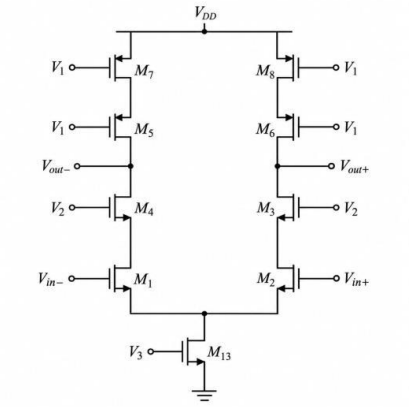


Fig. 2. Telescopic OTA: input pair M1/M2, cascodes M3–M6, loads M7/M8 and tail transistor M13 (MN5).

C. Gain Control Through the Tail Current

With its source grounded and gate at V_{CTRL}, the tail device carries

$$I_{tail} \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{13}(V_{CTRL} - V_{THn})^2 \qquad (4)$$

so V_{CTRL} sets I_{tail}, g_{m1} and the gain. The direction of the control characteristic depends on frequency. Above the dominant pole

$$f_p = \frac{1}{2\pi R_{out} C_L}$$

the gain behaves approximately as

$$|A_v(f)| \approx \frac{g_{m1}}{2\pi f C_L}$$

$$f \gg \frac{1}{2\pi R_{out} C_L} \qquad (5)$$

which increases with I_{tail}. At low frequency, in a square-law model with constant channel-length modulation, R_{out} falls faster with current than g_{m1} rises, so the DC gain decreases as I_{tail} increases. The polarity of the loop must therefore be verified at the carrier frequency and not only at DC. At the low end of V_{CTRL}, the tail device approaches V_{THn} and g_{m1} collapses, which defines the usable control range.

D. Amplitude Detector

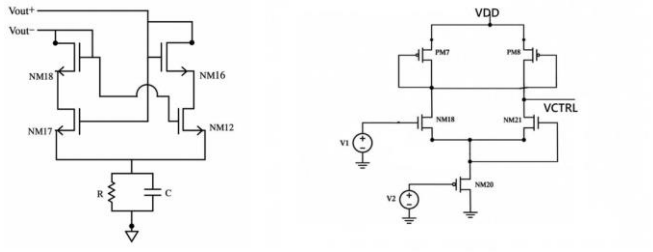
The detector (Fig. 3a) senses V_{out+} and V_{out-}. Two NMOS stacks, in which diode-connected devices NM18 and NM16 are in series with NM17 and NM12 respectively and each is driven by the opposite signal phase, share a source node returned to ground through a parallel R–C network. For a device with overdrive V_{OV} and a gate signal $a\cos(\omega t)$, the average drain current rises above its quiescent value by

$$\Delta I_D = \frac{ka^2}{4}$$

,

$$k = \mu_n C_{ox}\left(\frac{W}{L}\right) \qquad (6)$$

so the detector is square-law for small signals and approaches a peak-like linear response when the device is cut off during part of the cycle. The resistor converts the average current into $V_{ENV} \approx V_{ENV0} + R\Delta I_D$, and over a limited range $V_{ENV} \approx K_D A_{out} + V_{off}$, where K_D is the local slope of the simulated transfer curve and V_{off} is the offset with no RF input. V_{REF} must be chosen above this offset and inside the detector's usable range. The rectified current contains a component at $2f_{RF}$ that the R–C network attenuates by approximately $1/(2\pi \cdot 2f_{RF}RC)$; at 28 GHz this ripple is negligible, and the real constraint is that $\tau = RC$ adds a low-frequency pole to the AGC loop. The detector gate capacitances also load the OTA output and slightly reduce its bandwidth.



(a) (b)

Fig. 3. (a) Amplitude detector with R–C averaging network. (b) Error amplifier: PM7/PM8 load, NM18/NM21 differential pair, NM20 tail source, bias sources V1 and V2, output V_{CTRL}

E. Error Amplifier

The error amplifier (Fig. 3b) is a differential pair with a PMOS load and an NMOS tail source NM20. One input receives the reference V_{REF} and the other receives V_{ENV}; the output V_{CTRL} is taken at the drain of NM21. A rise of V_{ENV} raises the NM21 current and lowers V_{CTRL}, so the stage is inverting from V_{ENV} to V_{CTRL}:

$$V_{err} = V_{REF} - V_{ENV},$$
$$\Delta V_{CTRL} \approx -A_{EA}\Delta V_{ENV} \qquad (7)$$

The gain depends on the load. A diode-connected PMOS load, as drawn in Fig. 3b, gives $|A_{EA}| \approx \frac{g_{mN}}{g_{mP}}$, a low value set by a device ratio, whereas a current-mirror load gives$A_{EA} \approx g_{mN}(r_{oN} \parallel r_{oP})$. Because the residual regulation error is divided by (1 + loop gain), the diode-connected load limits regulation accuracy, and the mirror-load variant is the obvious refinement. The output swing of the stage must also cover the range of V_{CTRL} over which the tail transistor remains in its intended region.

F. Loop Gain, Polarity and Stability

Negative feedback requires the product of the signs of the three links, namely the detector (positive), the error amplifier (negative as above) and the control element $\frac{dA_{out}}{dV_{CTRL}}$, to be negative. The loop therefore regulates only if the OTA gain at the carrier frequency increases with V_{CTRL}, which (5) predicts and which is examined with an open-loop gain-control sweep in Section V-B. With $A_{out} = G(V_{CTRL})A_{in}$, the low-frequency loop gain and the compression of the output variation are

$$T_0 = A_{EA}K_D A_{in}\left|\frac{dG}{dV_{CTRL}}\right|,$$
$$\frac{dA_{out}}{dA_{in}} \approx \frac{G}{1+T_0} \qquad (8)$$

In steady state the loop drives V_{ENV} toward V_{REF}; this is a target, not a guarantee, because finite gain, offsets, detector nonlinearity and a limited control range leave a residual error. The compression is also lost at the extremes of the input range, where V_{CTRL} reaches the end of its usable range.

The loop contains two low-frequency poles: the detector R–C pole and the pole formed by the error-amplifier output resistance and the gate capacitance of M13. The OTA output pole is far higher and does not limit the loop. Two comparable low-frequency poles give a poor phase margin, so one should be made dominant, for example through τ or an added capacitor at V_{CTRL}, with the unity-gain frequency f_u placed well below the second pole. The phase margin is

$$PM = 180° + \angle T(j\omega_{gc}) \qquad (9)$$

evaluated at the loop-gain crossover ω_{gc}, and the closed-loop time constant is of the order of $1/(2\pi f_u)$. The loop bandwidth should lie well below the envelope-modulation bandwidth of the RF signal so that wanted amplitude information is not removed, and well above the rate at which the input level varies; residual detector ripple on V_{CTRL} modulates the tail current and appears as gain modulation.

Simulation Setup

The circuit was captured at transistor level and simulated in Cadence Virtuoso with the Analog Design Environment. The OTA gain was obtained from an AC analysis from 1 Hz to 100 GHz as $20\log_{10}\left|\frac{V_{out1}-V_{out2}}{V_{inn}-V_{inp}}\right|$ with the corresponding differential phase. Process-corner analysis used the FF, FS, SS and SF model sets; the width sweep used 120, 240 and 360 nm at the FF corner, and the temperature sweep used −24 °C, 27 °C and 55 °C at the FF corner. The technology is gpdk90, with VDD =1.8 V, channel length 100nm, bias voltages V1, V2, V3 = 1.2V, 800mV,Vctrl, load capacitance and detector R, C = 100kΩ, 10pF. The width sweep was applied to NM1, NM3.

The corner, width and temperature sweeps were extracted with a separate output-to-node transfer expression from the one used for the nominal differential gain of Fig. 4, and their absolute gain levels are therefore not directly comparable with it. They are interpreted here as relative sensitivities.

All results are open-loop AC data, and no closed-loop transient, power, noise or linearity data are reported. The gain-control sweep (Section V-B) steps the control input through four settings.

Results and Discussion

A. Nominal Gain and Phase

Fig. 4 shows the nominal differential gain. The low-frequency gain is approximately 74 dB (a reading from the plot), the dominant pole lies at roughly 70 MHz, the magnitude falls at about 20 dB/decade between 1 and 10 GHz, and the marker at 28 GHz reads 24.99 dB. This is consistent with the single-pole behaviour implied by (5) and with a dominant pole set by $R_{out}C_L$. The nominal phase is close to 0° at low frequency and becomes increasingly negative with a second phase transition above approximately 1 GHz, which indicates additional non-dominant poles or zeros.

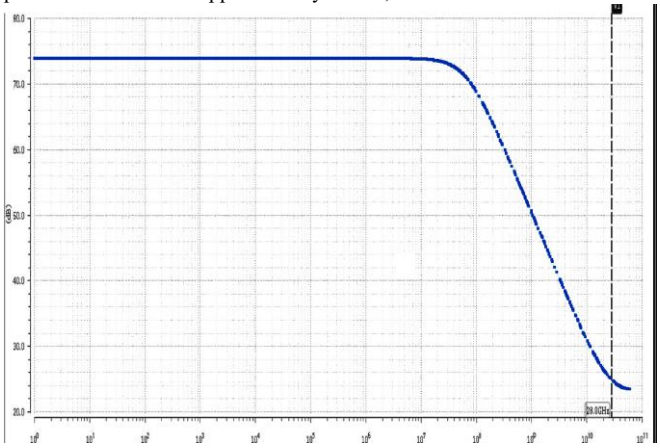


Fig. 4. Simulated nominal differential gain (dB) of the OTA versus frequency (1 Hz to 100 GHz); the marker V1 at 28 GHz reads 24.992 dB.

B. Gain-Control Sweep

Fig. 5 shows the open-loop gain for four settings of the control input. The low-frequency gain of the four traces lies between approximately 80 dB and 92 dB (readings from the plot), and the traces cross at roughly 5–30 MHz, so that the trace with the highest low-frequency gain has the lowest gain at higher frequency. At 28 GHz the markers read 31.91, 25.33, 22.14 and 20.10 dB, a range of 11.8 dB. Opposite orderings of the low-frequency and carrier-frequency gain are consistent with the frequency-dependent sign of the control characteristic discussed in Section III-C. The control voltages belonging to the four traces are not recorded with the plot, so the direction of the 28-GHz gain with V_{CTRL}, and hence the loop polarity, is not yet confirmed, and four settings do not establish the full gain-control range or its linearity.

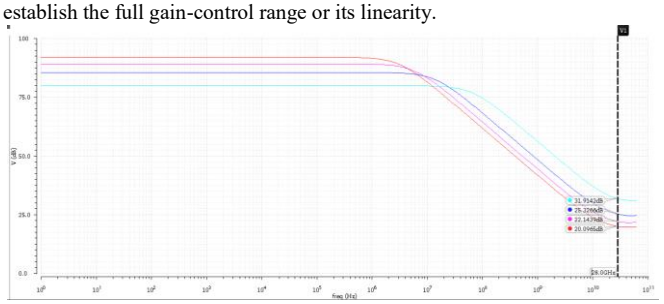


Fig. 5. Simulated open-loop gain (dB) of the OTA versus frequency (1 Hz to 100 GHz) for four settings of the control input; the markers at 28 GHz read 31.9142, 25.3266, 22.1439 and 20.0965 dB.

C. Process Corners

Table I lists the corner results. At low frequency the gain ranges from 16.7 dB (SS) to 20.8 dB (SF), a spread of 4.1 dB at 1 MHz and 4.0 dB at 1 GHz. At higher frequency the corners converge: the spread is 1.7 dB at 10 GHz and 1.6 dB at 28 GHz, where SF is highest (15.6 dB) and SS is lowest (14.0 dB). SF and SS are the highest- and lowest-gain corners at every tabulated frequency, whereas FF and FS exchange places between 1 GHz and 10 GHz. The corner-induced gain variation at the carrier is therefore small compared with the temperature variation of Section V-E, and process corners alone would require only a small control range at 28 GHz.

TABLE I: Gain Across Process Corners (DB)

Corner	1 MHz	100 MHz	1 GHz	10 GHz	28 GHz
FF	19.2	19.2	18.8	17.0	15.0
FS	18.8	18.8	18.5	17.3	15.3
SS	16.7	16.7	16.5	16.0	14.0
SF	20.8	20.8	20.5	17.7	15.6

D. Transistor Width

Table II shows that gain rises monotonically with width at the FF corner: by 1.0 dB at 1 MHz, 1.3 dB at 10 GHz and 1.8 dB at 28 GHz between 120 nm and 360 nm. A larger input pair delivers more transconductance for a given bias current, which is consistent with the low-frequency trend. Increasing width also increases input and output capacitance, area and bias requirements, which are not tabulated, so the 360-nm case is the highest-gain case of the sweep but is not claimed to be the best overall design.

TABLE II: Gain Versus Transistor Width at the FF Corner (dB)

Width (nm)	1 MHz	100 MHz	1 GHz	10 GHz	28 GHz
120	18.0	18.0	17.8	16.2	15.0
240	18.5	18.5	18.3	16.9	16.3
360	19.0	19.0	18.8	17.5	16.8

E. Temperature

Table III lists the temperature results at the FF corner. The low-frequency gain is 2.0 dB at −24 °C, 19.0 dB at 27 °C and 18.6 dB at 55 °C, and the gain at 28 GHz is 1.0 dB, 15.0 dB and 9.3 dB, respectively. The gain therefore depends strongly and non-monotonically on temperature: relative to 27 °C, the gain at −24 °C is lower by 17.0 dB at low frequency and 14.0 dB at 28 GHz, and at 55 °C the low-frequency gain falls by only 0.4 dB while the gain at 28 GHz falls by 5.7 dB. This is the largest gain variation among the process, width and temperature sweeps and is the main motivation for closed-loop regulation in these results. A possible cause is that the temperature dependence of mobility and threshold voltage shifts the operating point of the fixed-bias devices, in particular the tail transistor, which could explain the reduced gain at −24 °C; this is a hypothesis that was not tested and it should not be generalized to other bias conditions or corners. The phase at 28 GHz becomes less negative with temperature (Table IV).

TABLE III: Gain Versus Temperature at the FF Corner (dB)

Temperature (°C)	Low-frequency gain	Gain at 28 GHz
−24	2.0	1.0
27	19.0	15.0
55	18.6	9.3

F. Phase at the Carrier

Table IV lists the phase at 28 GHz for all ten cases, together with 180° + φ(28 GHz). This quantity measures the remaining phase budget at the carrier. It is not a stability margin, since 28 GHz is not the unity-gain frequency of the loop (Section III-F) and the OTA still has about 25 dB of gain there. The corner spread of the phase is 58.2° (FF −114.9°, SS −173.1°), and SS and SF show the largest lag. The 240-nm and 360-nm cases show positive phase excursions at intermediate frequencies in their traces; whether these arise from peaking, a left-half-plane zero or the probe expression has not been established, and the mid-band phase values are therefore not tabulated.

TABLE IV: Phase at 28 GHz and 180° + φ for All Sweeps

Sweep	Case	φ (28 GHz)	180° + φ
Corner	FF	−114.9°	65.1°
Corner	FS	−159.0°	21.0°
Corner	SS	−173.1°	6.9°
Corner	SF	−170.9°	9.1°
Width (FF)	120 nm	−154.3°	25.7°
Width (FF)	240 nm	−93.1°	86.9°
Width (FF)	360 nm	−45.1°	134.9°
Temp. (FF)	−24 °C	−157.6°	22.4°
Temp. (FF)	27 °C	−145.9°	34.1°
Temp. (FF)	55 °C	−135.4°	44.6°

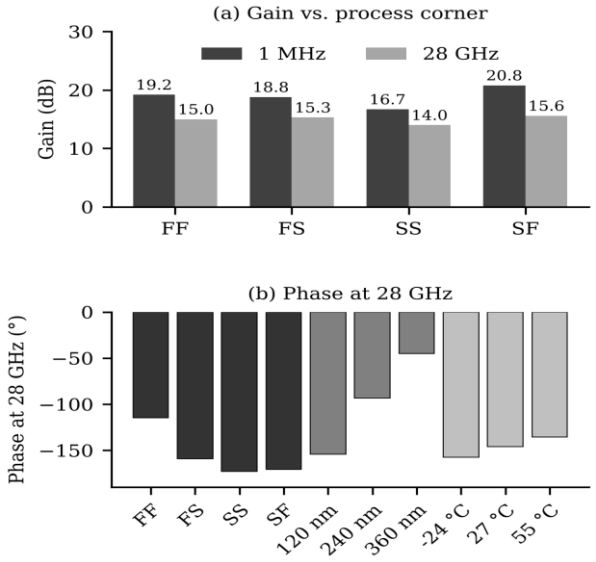


Fig. 6. Summary of the tabulated sweeps: (a) gain at 1 MHz and 28 GHz per process corner; (b) phase at 28 GHz for corners, widths and temperatures.

G. Scope and Limitations

The results characterize the open-loop OTA and establish trends under process, width and temperature variation, together with a four-setting open-loop gain-control sweep. They do not establish the closed-loop regulation accuracy, the full gain-control range and its dependence on the control voltage, the AGC settling time, the loop phase and gain margin, the output swing, the power consumption, the noise, the linearity, the suitability of the detector at 28 GHz over its input range, or post-layout performance. The finding that the gain at 28 GHz varies between 1.0 dB and 15.0 dB over the temperature range at the FF corner is a motivation for, not a demonstration of, the benefit of the AGC loop.

Conclusion and Future Work

A telescopic-OTA VGA with tail-current gain control and an envelope-detector/error-amplifier AGC loop was analysed and characterized by simulation. The analysis shows that the loop polarity must be evaluated at the carrier frequency, where the OTA gain increases with tail current, and that loop gain and the two low-frequency loop poles determine regulation accuracy and stability. Open-loop simulation gives about 74 dB low-frequency gain and 24.99 dB at 28 GHz; across corners the gain spread narrows from 4.1 dB at low frequency to 1.6 dB at 28 GHz, whereas at the FF corner the gain at 28 GHz varies between 1.0 dB and 15.0 dB over −24 °C to 55 °C, and an open-loop gain-control sweep moves the 28-GHz gain between 20.1 dB and 31.9 dB.

Future work comprises closed-loop transient simulation with input-amplitude steps; measurement of the V_{CTRL}-to-gain characteristic, with the control voltage of each trace recorded, and of the detector transfer curve at 28 GHz; loop phase and gain margin and settling time; a higher-gain current-mirror load for the error amplifier; consistent re-extraction of the PVT sweeps with the differential-gain expression; power, noise and linearity (compression point, IIP3) evaluation; post-layout simulation; and integration into the 28-GHz vector modulator to evaluate amplitude and phase accuracy.

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