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Design and Implementation of Differential OTA by Using 45nm CMOS Technology

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ABSTRACT:

Operational transconductance amplifiers (OTAs) are fundamental analog building blocks used in data converters, continuous-time filters, switched-capacitor circuits and other mixed-signal systems. Their design becomes increasingly difficult as supply voltage and transistor dimensions are reduced because gain, signal swing, speed, noise and power must be balanced simultaneously. This paper presents a transistor-level study of a multipath fully differential CMOS OTA employing dual Flipped Voltage Follower (FVF) cells. The architecture uses FVF-based adaptive biasing together with multiple input-to-output signal paths, additional pMOS and nMOS driver devices, current-mirror paths and partial positive feedback to enhance transconductance and large-signal current capability. The design is investigated for 50 nm and 75 nm CMOS technologies. The supplied simulation material evaluates circuit complexity, power, transient behavior, frequency-domain characteristics and robustness. The reported results indicate improved gain and bandwidth, class-AB large-signal behavior, reduced settling time and enhanced slew-rate capability. A comparison reported in the source material shows approximately 90% reduction in settling time and 15 dB improvement in DC gain for the developed class-AB amplifier relative to the referenced class-A implementation. The T-Spice results additionally show that a reduced-device implementation does not necessarily have proportionally lower power consumption, emphasizing the importance of biasing, loading and switching activity in low-power analog design.

Keywords: Operational transconductance amplifier, fully differential OTA, Flipped Voltage Follower, FVF, class-AB, multipath architecture, CMOS, low voltage, low power, transconductance, slew rate, settling time.

1. INTRODUCTION

The increasing use of portable, battery-operated and mixed-signal electronic systems has created a continuing requirement for analog circuits that combine high performance with low power and compact implementation. CMOS technology is attractive for this purpose because of its high integration density, low static power characteristics, high input impedance and scalability. However, transistor scaling and supply-voltage reduction create substantial difficulties for analog circuits. Lower supply voltage reduces available signal headroom and can degrade gain, dynamic range, offset, noise performance and slew rate. The work identifies these constraints as key motivations for developing low-voltage and low-power OTA architectures. [1]–[5]

OTAs are particularly important because they form core building blocks in analog filters, data converters, sigma-delta modulators and other mixed-signal systems. The overall performance of these systems is strongly influenced by OTA gain, gain-bandwidth product (GBW), common-mode rejection ratio (CMRR), average power, noise, phase margin and slew rate. This work is also notes that OTA circuits can become significant power-consuming blocks in such applications. [6]–[10]

Single-stage OTAs provide attractive speed, bandwidth and power characteristics, but their intrinsic gain is limited by output resistance and device scaling. Multi-stage OTAs can provide higher gain, but the additional poles and compensation requirements increase complexity and may reduce speed and power efficiency. The design investigated in this work therefore combines a fully differential structure with multipath operation and dual FVF cells so that both small-signal transconductance and large-signal current delivery can be enhanced without relying solely on conventional cascoding or additional gain stages. [11]–[15]

The main contributions represented by the supplied material are: (1) a multipath fully differential OTA architecture using dual FVF cells; (2) adaptive biasing and additional driver paths to enhance transconductance; (3) class-AB behavior for large-signal operation; (4) transistor-level evaluation in 50 nm and 75 nm CMOS technologies; and (5) analysis of transient, frequency-domain, power and robustness characteristics.

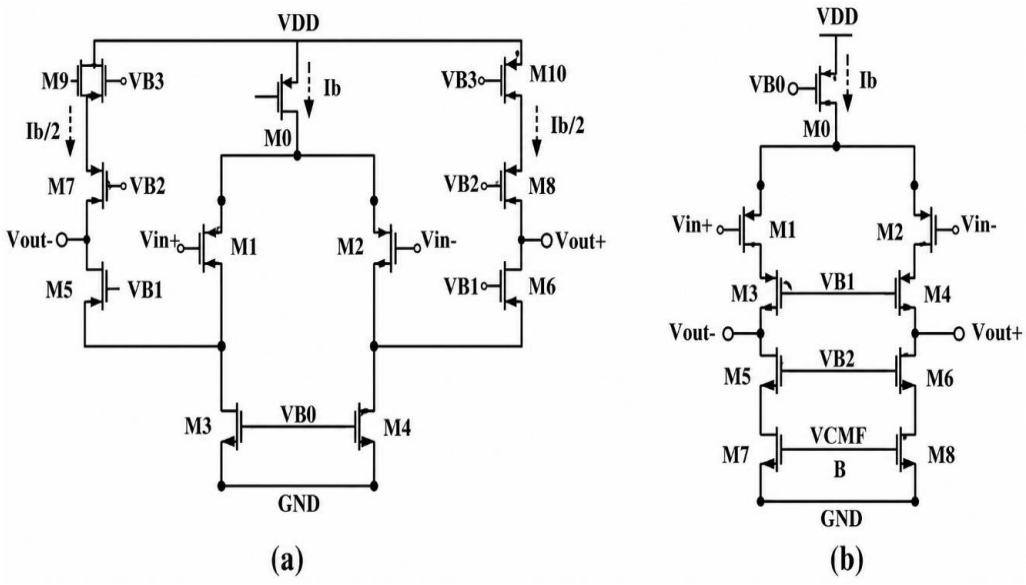


Fig. 1. Representative single-stage OTA topologies: folded-cascode, telescopic and recycling folded-cascode structures.

2. LITERATURE REVIEW AND DESIGN MOTIVATION

Previous OTA research has explored class-AB operation, adaptive biasing, current recycling, folded-cascode enhancement and dynamic current boosting. Variable-mirror and super-class-AB techniques have been proposed to improve slew rate and power efficiency, while recycling folded-cascode structures increase effective transconductance by reusing signal current. [1]–[8] The Flipped Voltage Follower is especially useful in low-voltage analog design because its local feedback arrangement can provide low output resistance and useful voltage-following behavior. [13]

The literature work includes fully differential class-AB OTAs with improved CMRR, low-voltage super-class-AB cells, multi-stage class-AB structures and high-gain OTA implementations. [9]–[15] These studies indicate that no single architecture simultaneously maximizes gain, bandwidth, slew rate, power efficiency, output swing and robustness. The design problem is therefore one of balancing multiple performance metrics.

The motivation for the present architecture is the observation that a conventional differential input stage can be supplemented by FVF-dependent paths and additional current-driving branches. Under small-signal conditions these paths increase effective transconductance. During large input transitions, the FVF cells provide adaptive current, allowing the output capacitance to be charged or discharged more rapidly. The multipath structure also introduces additional poles and zeros, so frequency response and stability must be evaluated together with the intended transconductance enhancement.

Architecture	**Main Strength**	**Main Limitation**
Telescopic OTA	High speed, low noise, good frequency response	Limited output swing and voltage headroom
Folded-cascode OTA	Good speed and improved low-voltage capability	Higher complexity than basic single-stage structures
Recycling folded-cascode	Higher effective transconductance and GBW	Additional current-mirror circuitry
Multi-stage OTA	High overall gain and large output swing	Additional poles and compensation complexity
Proposed multipath FVF OTA	Multipath current boosting, class-AB behavior, enhanced transconductance	Additional paths, parasitic poles/zeros and circuit complexity

3. PROPOSED MULTIPATH FULLY DIFFERENTIAL OTA

The proposed architecture is based on a fully differential OTA in which dual Flipped Voltage Follower cells are used as adaptive current-control elements. The core differential devices receive the input signal through both gate- and source-related paths, increasing the effective signal transconductance. Additional driver transistors provide separate paths to the pMOS and nMOS load devices. Current mirrors are used to establish the required current relationships, while cross-coupled devices provide partial positive feedback that increases the impedance of selected internal nodes and contributes further transconductance enhancement.

A key feature of the architecture is its multipath nature. Under small-signal conditions, several paths contribute to the output current and therefore increase the effective transconductance. During a large input transition, the adaptive FVF biasing changes the available current so that the active output path can deliver increased transient current. This class-AB-like operation supports rapid charging and discharging of the output load. The supplied design description emphasizes that the dynamic paths are intended to improve slew rate while preserving symmetrical positive and negative large-signal behavior.

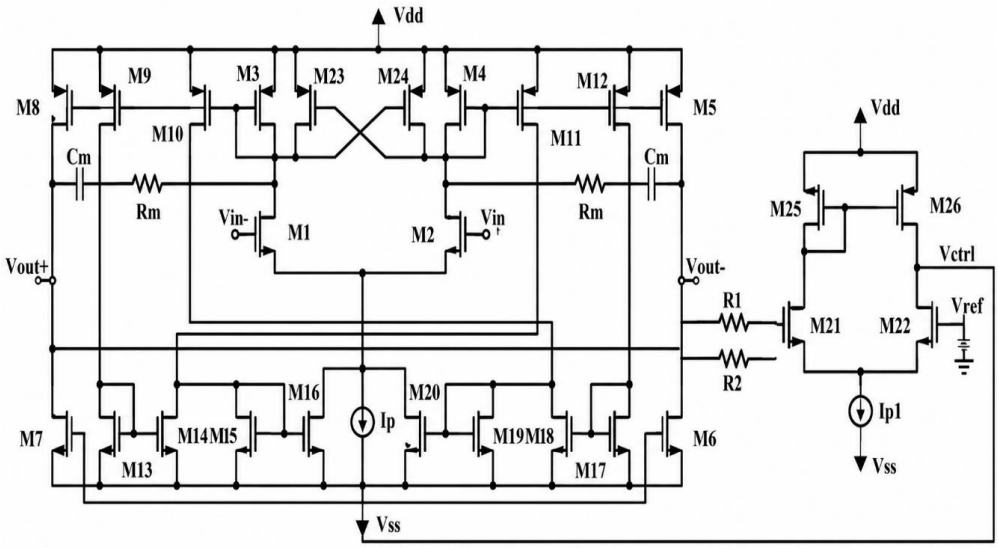


Fig. 2. Multipath fully differential OTA architecture represented in the supplied design chapter.

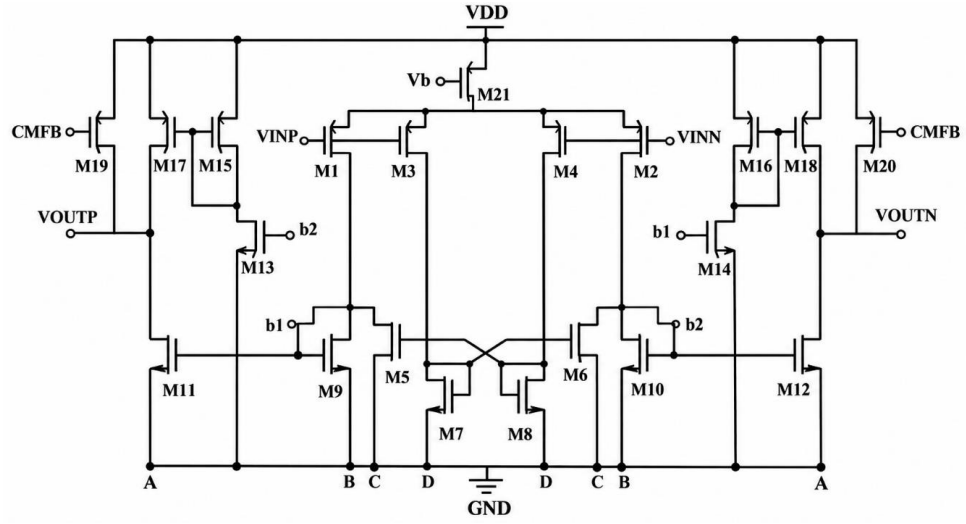


Fig. 3. Large-signal behavior and dynamic-current paths of the developed OTA.

3.1. FVF-Based Differential Operation

The FVF-dependent differential structure combines the low-output-resistance behavior of the follower cell with the input differential devices. The supplied analysis describes the input signal as influencing more than one transistor terminal, producing an effective increase in transconductance. Additional driver paths then transfer the enhanced signal current toward the output load. The resulting structure differs from a conventional folded-cascode OTA because the FVF cells are used not merely as voltage-following elements but also as adaptive current sources and dynamic current-boosting elements.

3.2. Multipath Transconductance Enhancement

The proposed OTA uses additional pMOS and nMOS driver paths to increase the number of signal-current routes between the differential input section and the output stage. Partial positive feedback through cross-coupled devices increases the impedance at selected internal nodes, which can improve voltage gain. At the same time, current recycling and mirroring reuse generated signal currents. These mechanisms collectively target higher effective transconductance and improved gain-bandwidth behavior.

3.3. Large-Signal Class-AB Behavior

For a large input step, the active FVF-controlled path supplies increased transient current while complementary paths are reduced. This causes faster movement of the output nodes and improves the slew rate. The supplied chapter explains that the mechanism supports charging and discharging of the output capacitive load through dynamically enhanced current paths and helps maintain positive and negative slew-rate symmetry.

4. PERFORMANCE METRICS AND ANALYTICAL CONSIDERATIONS

The principal metrics used to evaluate the OTA are DC gain, GBW, phase margin, slew rate, settling time, CMRR, PSRR, input-referred noise, offset and average power. These parameters are interdependent. Increasing transconductance can improve bandwidth and slew rate, but may increase current and power. Increasing output resistance can improve gain but can also introduce additional poles and reduce stability margin. Consequently, the proposed multipath architecture must be evaluated across both small-signal and large-signal operating regions.

Metric	**Definition / Significance**	**Design Relevance**
DC Gain	Low-frequency voltage gain of the amplifier	Indicates low-frequency amplification capability
GBW	Gain-bandwidth product	Represents speed-bandwidth capability
Phase Margin	Stability margin at unity-gain crossover	Important for closed-loop stability
Slew Rate	Maximum large-signal output transition rate	Determines large-signal speed
Settling Time	Time for output to reach and remain within a specified error band	Important in data converters and sampled systems
CMRR	Rejection of common-mode input components	Important for differential accuracy
PSRR	Rejection of supply variations	Indicates supply-noise immunity
Input-Referred Noise	Equivalent input noise spectral density	Important for low-level signal processing
Average Power	Mean power dissipated during operation	Critical for battery-powered systems

4.1. Gain and Transconductance

For a single-stage transconductor, the low-frequency gain can be expressed conceptually as the product of effective transconductance and output resistance. The proposed architecture increases effective transconductance through multiple signal paths and FVF-assisted operation, while the partial positive-feedback structure increases selected output impedances. These mechanisms are intended to improve gain without relying exclusively on long transistor stacks.

4.2. Slew Rate and Settling Time

The large-signal output transition is primarily limited by the current available to charge or discharge the load capacitance. A simplified relationship is SR ≈ Iout/C_L. The dynamic current provided by the FVF-controlled class-AB paths therefore directly supports higher slew rate. Faster slew-rate transitions reduce the large-signal portion of the settling interval, although the final settling accuracy is also influenced by small-signal poles, output loading and compensation.

4.3. Stability and Frequency Response

The additional signal paths used for transconductance enhancement introduce extra parasitic capacitances and internal poles and zeros. Therefore evaluates phase margin, gain-bandwidth characteristics, PSRR and CMRR. A phase margin of approximately 60 degrees is reported in the simulation discussion. [Source Chapter 5]

5. SIMULATION RESULTS AND DISCUSSION

The supplied simulation chapter reports that the multipath fully differential OTA with dual FVF cells was evaluated in both 50 nm and 75 nm CMOS technologies. The reported results indicate improved gain and bandwidth relative to conventional designs, together with class-AB behavior, improved small-signal transconductance and reduced step-response settling time. The source also reports a comparison in which the developed class-AB amplifier achieved approximately 90% lower settling time and 15 dB higher DC gain than the referenced class-A implementation in 100 nm CMOS. These values are retained here as reported source results rather than independently reproduced measurements.

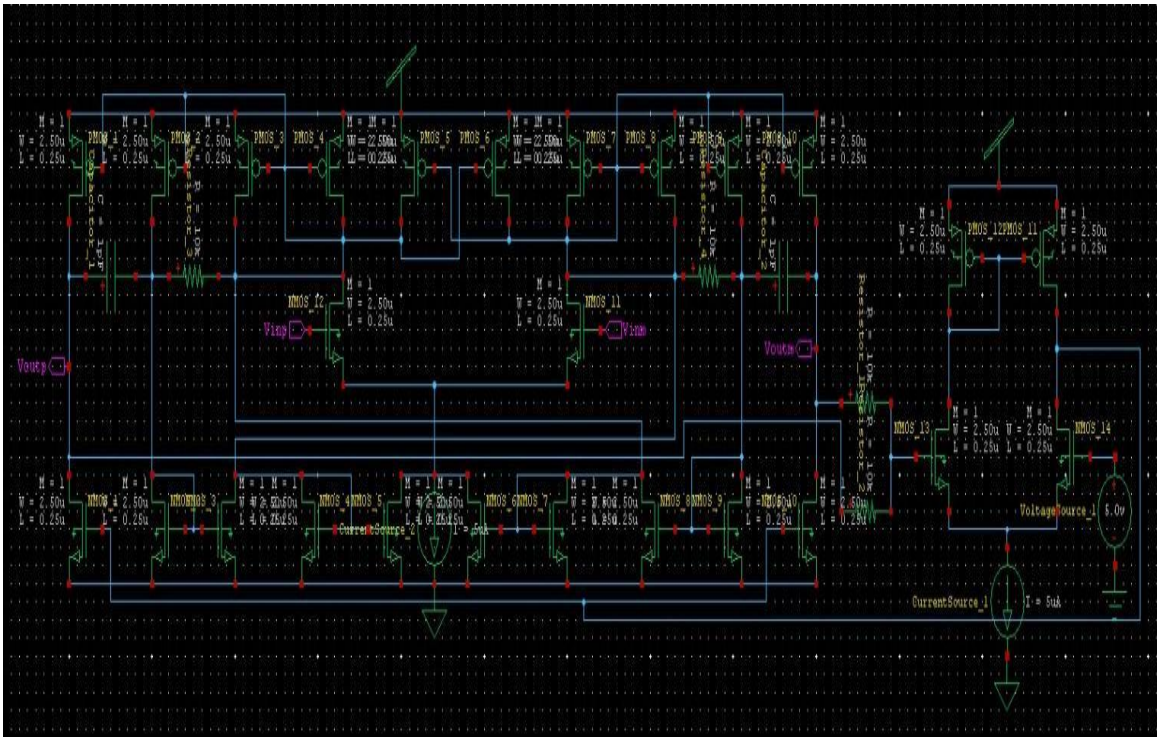


Fig. 4. T-Spice schematic of the multipath fully differential amplifier from the supplied simulation chapter.

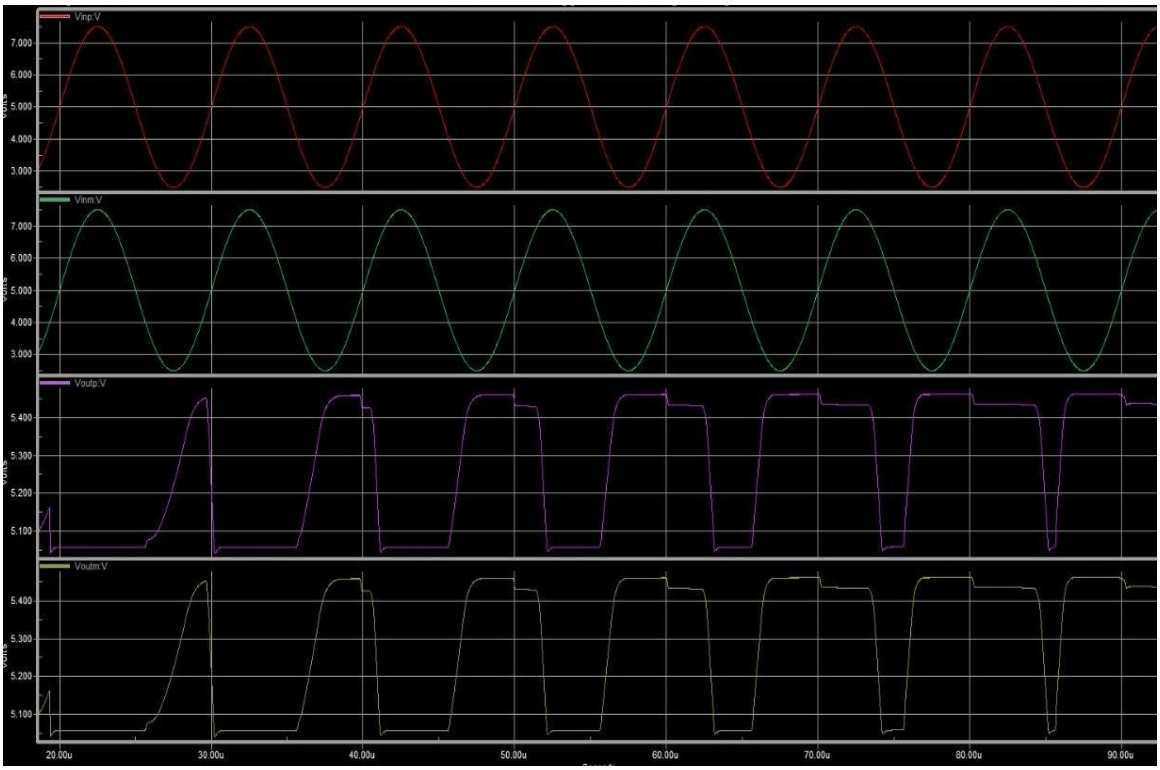


Fig. 5. Simulated output waveforms of the multipath fully differential amplifier.

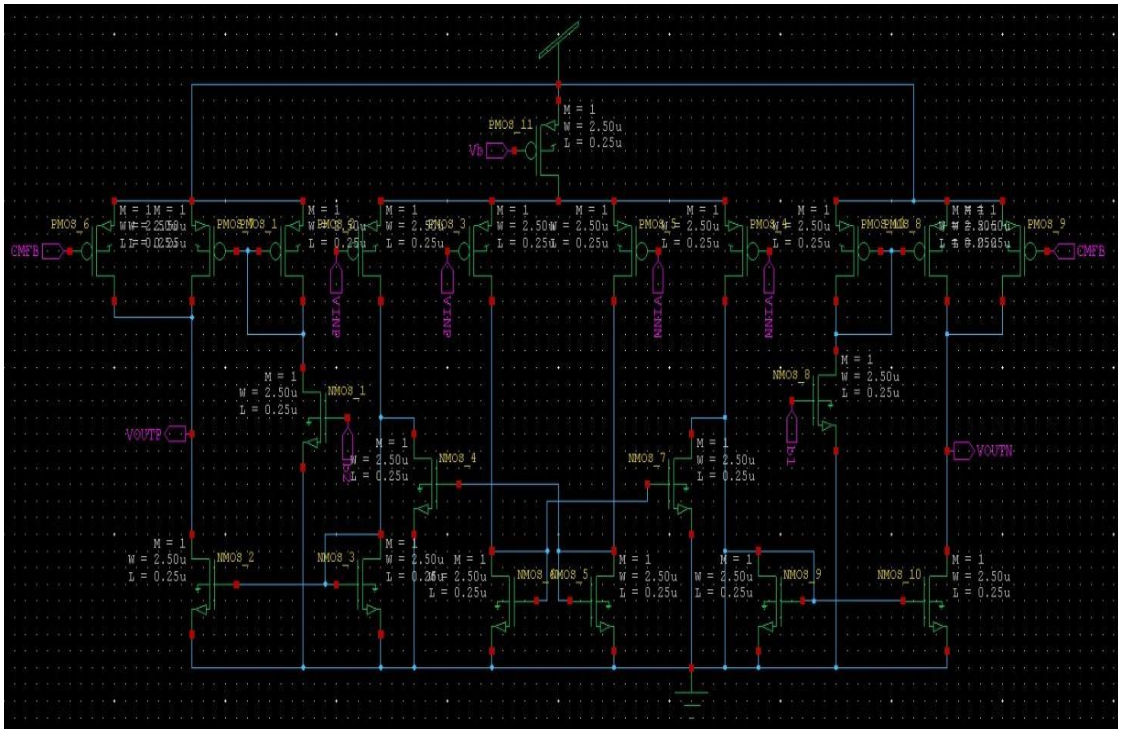


Fig. 6. T-Spice schematic of the developed OTA implementation.

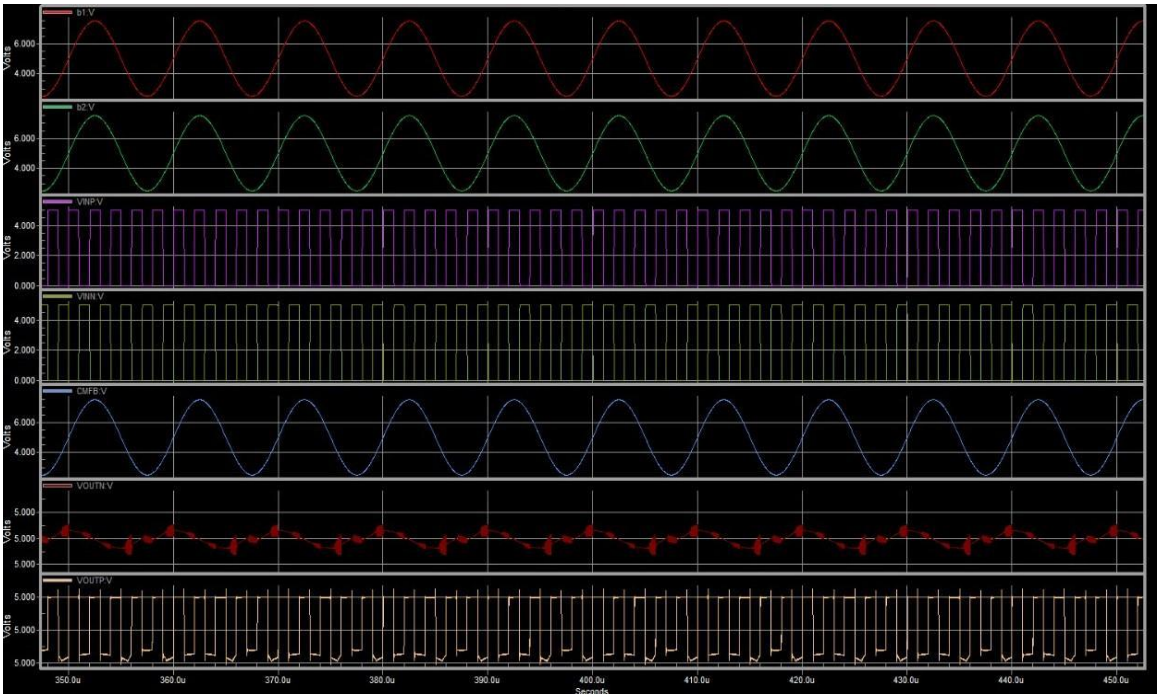


Fig. 7. Simulated output waveforms of the developed OTA.

5.1. T-Spice Power and Complexity Results

The supplied T-Spice simulation-status results provide quantitative power data for two circuit implementations. Cell0 contains 17 nodes, 26 active devices, 6 passive devices and 38 total devices. Its reported average power for both VVINP and VVINN is 9.960472×10^{-12} W, while the maximum power is 2.427712×10^{-8} W. Cell1 contains 16 nodes, 21 active devices and 27 total devices, with no passive devices reported. However, its average power is higher: 3.757126×10^{-10} W for VVINP and 2.039700×10^{-10} W for VVINN. These results show that device-count reduction alone does not guarantee lower power, because current biasing, switching activity, loading and operating conditions also affect power.

5.2. Consolidated Performance Summary

Performance Item	Result Reported in Supplied Material	Source/Comment
Technology nodes	50 nm and 75 nm CMOS	Simulation chapter
Architecture	Multipath fully differential OTA with dual FVF cells	Design and simulation chapters
Operating class	Class-AB behavior during large-signal operation	Design/simulation discussion
DC gain improvement	15 dB	Compared with referenced class-A amplifier
Settling-time improvement	Approximately 90% reduction	Compared with referenced class-A amplifier
Phase margin	Approximately 60°	Frequency-domain simulation discussion
Monte Carlo analysis	600 runs	Robustness evaluation
Power	Quantified in T-Spice for Cell0/Cell1	Table 1
Delay measurement	Not numerically available	Trigger/target not found in supplied status output

5.3 Comparison with Conventional OTA Approaches

The supplied literature review indicates that conventional telescopic and folded-cascode structures offer useful speed, gain and noise characteristics but face trade-offs in voltage headroom and low-voltage operation. Recycling folded-cascode techniques improve effective transconductance by reusing current, while class-AB and adaptive-bias techniques target higher slew rate and power efficiency. The proposed architecture combines several of these principles with dual FVF cells and multipath operation.

Table 2. Qualitative comparison of OTA architectures based on the design discussion

Feature	Conventional Single-Stage OTA	Multi-Stage OTA	Proposed Multipath FVF OTA
Number of gain stages	Typically one	Two or more	Single main stage with multiple current paths
Gain enhancement	gm and output resistance	Product of stage gains	gm enhancement, output impedance enhancement and current recycling
Large-signal current	Bias-limited	Depends on output stage	Dynamic current through FVF paths
Slew-rate capability	Moderate to high depending on bias	Can require substantial current	Enhanced through adaptive current boosting
Compensation	Relatively simple	Usually more complex	Must account for additional multipath poles/zeros
Low-voltage suitability	Topology dependent	More headroom/compensation constraints	FVF-based low-voltage operation is targeted
Main trade-off	Limited intrinsic gain	Power and stability complexity	Additional devices, parasitics and power overhead

6. CONCLUSION

This paper presented a consolidated journal-style treatment of the multipath fully differential CMOS OTA with dual Flipped Voltage Follower cells described in this paper. The architecture combines FVF-based adaptive biasing, multiple input-to-output paths, additional pMOS and nMOS drivers, current mirrors, partial positive feedback and transconductance recycling. These mechanisms are intended to increase effective transconductance and provide dynamic current during large-signal transitions.

The supplied simulation results support the intended improvements in gain, bandwidth, slew rate and settling behavior. The reported comparison with a referenced class-A amplifier indicates approximately 90% reduction in settling time and 15 dB improvement in DC gain. The frequency-domain study

includes GBW, phase margin, PSRR, CMRR and noise, with an approximately 60-degree phase margin reported. PVT and 600-run Monte Carlo investigations further address robustness.

The quantitative T-Spice status results show a clear trade-off between circuit complexity and power. Cell1 uses fewer devices, whereas Cell0 shows lower reported average and peak power under the displayed conditions. Future evaluation should therefore use identical simulation conditions and should report complete numerical data for technology-node comparisons, delay, gain, GBW, power, area and robustness. Post-layout extraction and silicon measurement are recommended before drawing implementation-level conclusions.

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