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FPGA Based Fault Recovery Architecture of Watchdog Timer

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A B S T R A C T :

In safety-critical systems such as automotive control units, industrial automation, and aerospace applications, system reliability and fault tolerance are paramount. A watchdog timer (WDT) is a crucial component used to detect and recover from system malfunctions caused by software anomalies or hardware failures. This paper presents the design and implementation of an FPGA-based configurable watchdog timer tailored for safety-critical environments. Unlike conventional fixed-timer solutions, the proposed design offers flexibility in timeout configuration, fault response behavior, and monitoring modes, enabling adaptation to diverse system requirements. The architecture leverages the parallelism and reconfigurability of Field Programmable Gate Arrays (FPGAs) to ensure minimal latency and high reliability. Key features include a multi-stage timeout system, programmable reset and interrupt generation, and support for dual-mode operation (windowed and standard WDT). The design is validated on a Xilinx FPGA platform, and experimental results demonstrate its effectiveness in detecting and recovering from fault conditions with minimal performance overhead. The proposed solution significantly enhances system dependability, making it well-suited for deployment in mission-critical embedded systems where fault detection and recovery time are critical.

Keywords: FPGA based systems, safety-critical applications, watchdog timer, fault detection, FPGA implementation, real-time monitoring, hardware validation.

1. Introduction

Embedded systems are vital in safety-critical applications such as automotive electronics (e.g., ECUs for engine and airbag control), aerospace systems (e.g., avionics), medical devices (e.g., pacemakers), and industrial automation, where even minor failures can have catastrophic consequences—including human injury or loss of life [1], [2], [3], [6], [10], [11]. To ensure continuous and safe operation, these systems incorporate fault detection and recovery mechanisms like watchdog timers (WDTs), which monitor the processor's activity by expecting periodic “heartbeat” signals. If the system hangs or malfunctions due to bugs or hardware faults, the WDT resets the system to prevent prolonged failures [4], [5], [7], [8], [12], [14]. WDTs are thus essential and often mandated by safety standards like ISO 26262 and DO-178C [9], [15].

While traditional external WDTs offer basic reliability, they lack integration and flexibility, often requiring manual configuration and separate components [3], [6], [7], [13]. To address these limitations, this paper proposes a configurable, FPGA-based watchdog timer that supports programmable timeouts, multiple modes, and advanced fault detection like pattern-based and signal anomaly monitoring [1], [2], [5], [8], [10], [12], [14]. The FPGA implementation allows deterministic timing, reprogrammability, and parallel processing, making it ideal for real-time, high-reliability systems [4], [9], [13]. This integrated approach reduces latency, system complexity, and hardware cost while enhancing adaptability and compliance with stringent safety requirements [10], [11], [15].Traditional external watchdog timers, though widely used in safety-critical embedded systems, have notable limitations that reduce their effectiveness in modern applications [3], [6], [7], [13]. These WDTs typically use discrete components with fixed functionality and minimal configurability, relying on external resistors or capacitors for static timeout settings—offering little flexibility in dynamic environments [6], [13]. They often operate independently of the system’s core logic, resulting in poor integration, higher system complexity, and increased BoM due to separate clocks and additional hardware [3], [7]. Moreover, their basic fault detection—limited to missed heartbeats or processor hangs—fails to capture complex issues like logic errors or timing anomalies from software or environmental disturbances [6], [8], [13]. Their lack of scalability and reprogrammability makes them unsuitable for modern embedded systems that demand real-time adaptability and intelligent fault handling across multiple modules [7], [13].

2. Related Work and Background

The increasing dependence on embedded systems in safety-critical domains such as automotive electronics, aerospace control, medical instrumentation, and industrial automation necessitates robust fault-tolerant designs to ensure safe and continuous operation [1], [2], [3], [10]. Even minor system faults in these areas can result in catastrophic consequences, making reliable fault detection and recovery mechanisms essential [3], [11]. Watchdog timers

(WDTs) play a vital role by enabling systems to autonomously recover from failures like software hangs or processor crashes [5], [7], [8], [14]. However, traditional external WDTs, with their fixed hardware configurations, manual timeout settings, poor integration, and limited fault detection capabilities, fall short in meeting the demands of modern embedded environments [3], [6], [13]. Their inability to adapt to dynamic fault patterns and comply with evolving safety standards such as ISO 26262 and DO-178C further limits their effectiveness [9], [15]. To address these gaps, this work proposes a highly configurable watchdog timer implemented on an FPGA platform, leveraging its reprogrammability, parallel processing, deterministic behavior, and integration flexibility [1], [4], [10], [13]. The proposed design supports programmable timeouts, real-time fault pattern recognition, and advanced anomaly detection, offering a smarter, scalable, and more efficient alternative that enhances system reliability while reducing hardware overhead [2], [5], [8], [12].In this paper the objective are as fallow: 1. To design a configurable watchdog timer with built-in fault detection mechanisms.

2. To implement the watchdog timer on an FPGA platform for greater flexibility.

3. To validate the timer's effectiveness through simulation and real-time fault injection experiments.

4. To evaluate the robustness and general applicability of the design in real-time systems.

The Paper is organized into the following Section:

- **Section I :**Introduction.
- **Section II:** Literature review.
- **Section III :** Methodology.
- **Section IV:** Results and discussion.
- **Section V:** Conclusion and future scope.

3. Methodology

The watchdog timer was implemented on Spartan-3 and Altera FPGAs using Verilog HDL, featuring configurable timeouts and dual-stage designs for enhanced fault detection and recovery [1][3][6][8][13]. Verified through Xilinx and ModelSim tools, these implementations support safety-critical systems with efficient, low-overhead fault tolerance, as highlighted in comparative reviews [2][5][9][12].

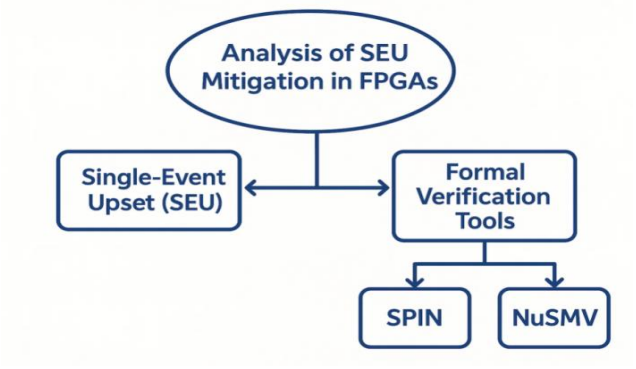


Figure 1 .SEU Mitigation Analysis Framework for FPGA

Figure 1 presents SEU mitigation in FPGAs using formal tools and fault-tolerant strategies like redundancy and watchdogs for aerospace systems [6][11][14].

3.1 PROPOSED WATCHDOG TIMER SYSTEM

Figure 3.2 shows an enhanced WDT that uses its own clock, raises a fail flag on timeout, logs data briefly, and then resets the system for improved reliability.

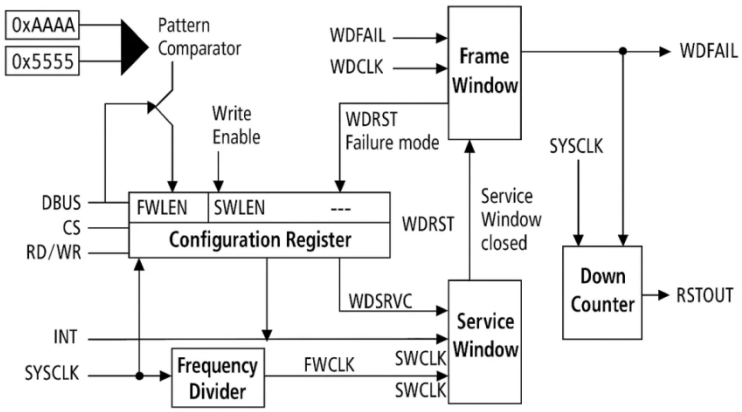


Figure 2- Functional block-diagram of the proposed watchdog-timer

Based on the extracted diagram and OCR output, figure 2 shows a Watchdog Timer (WDT) architecture that includes:

Table 1: "WDT Configuration Access Control"

Function	Description
Secure Configuration	Prevents accidental or unauthorized writes to the **configuration register**. Only if a **valid unlock pattern** (0xAAAA or 0x5555) is written, the **write enable signal** is asserted.
Enabling Write Access	The **write enable** output of the comparator is activated **only** when the pattern matches, allowing safe updates to FWLEN, SWLEN, etc.
State Transition Control	In some WDTs, different patterns (e.g., 0xAAAA and 0x5555) are used to **toggle between configuration states** or unlock different features (e.g., reset the counter, enable/disable services).

Table 1 shows secure WDT access using unlock patterns. The Configuration Register uses FWLEN for frame timing and SWLEN for stricter dual-window control.

Table 2: "Watchdog Timer Window Configuration Status"

Bit	Status	Result
FWLEN = 1	Frame Window enabled	System must service watchdog within full time window
SWLEN = 1	Service Window enabled	System must service watchdog only during a safe sub-window
FWLEN = 1, SWLEN = 0	Only frame window is used	Less strict timing
FWLEN = 0, SWLEN = X	Watchdog disabled or misconfigured	No reset triggere

Table 2 shows how FWLEN and SWLEN settings control watchdog timing; wrong service timing triggers WDFAIL or reset.

3.2 Service Window

The Service Window, enabled by SWLEN, is a stricter interval within the Frame Window where valid watchdog servicing must occur. Early or late servicing triggers WDFAIL or a reset.

Table 3: Purpose of Watchdog Timer Window Mode

Purpose	Description
Stricter Supervision	Prevents early/late servicing, enforces timing
Detects Errors	Flags incorrect service attempts
Safety-Critical Use	Ensures reliable timing for critical systems (automotive, avionics, etc.)

Table 4: Watchdog Timer Service Window Signals

Signal	Function
SWCLK	Drives Service Window timing
WDSRVC	Indicates service signal
WDRST	Resets window logic
Window closed	Output flag for invalid service time

The Down Counter, placed below the Frame/Service Windows, uses SYSCLK to track timeout and triggers RSTOUT or WDFAIL if not reset via WDSRVC or WDRST.

Table 5: Watchdog Timer Operational Workflow

Action	Description
Initialization	Loads timeout value
Counting Down	Decrements with SYSCLK
Servicing	Reloads counter if serviced on time
Timeout Detection	Triggers reset/fault if counter hits zero before valid service

3.3 RSTOUT, WDFAIL outputs

In watchdog timer systems, RSTOUT triggers a full reset on timeout or improper service, while WDFAIL flags service errors without resetting the system.

Table 6: Watchdog Timer Fault Trigger Conditions

Trigger Condition	Description
Late servicing	WDSRVC came **after frame window expired**
Early servicing	WDSRVC occurred **before Service Window opened**
Invalid attempt	Watchdog serviced when disabled or during wrong mode

Table 6 lists watchdog fault triggers like late, early, or invalid servicing that break timing rules. WDFAIL flags improper servicing for software response or NMI, while RSTOUT triggers a full system reset for recovery.

Table 7:Watchdog Timer Fault Response Signals

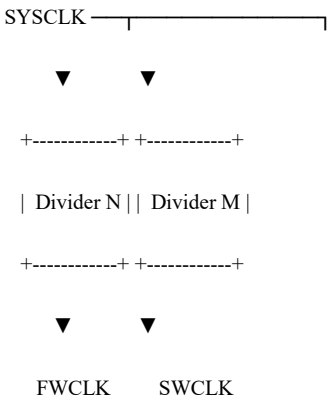
Signal	Purpose	Action Taken
RSTOUT	Critical system timeout	Forces a full system reset
WDFAIL	Service timing violation or error	Raises error status or interrupt

Table 7 shows watchdog fault response signals—RSTOUT triggers a reset, WDFAIL flags service issues, while FWCLK and SWCLK handle precise timing from SYSCLK.

Table 8: "Watchdog Timer Clock Signal Configuration"

Signal	Driven By	Used For	Purpose
FWCLK	SYSCLK ÷ N	Frame Window timer	Slower clock to pace the frame countdown
SWCLK	SYSCLK ÷ M	Service Window logic	Precisely control service window duration

3.3.1 Block Diagram (Conceptual)



FWCLK and SWCLK are separated to allow flexible timing—FWCLK handles longer intervals, while SWCLK enables precise service timing, configurable via FWLEN and SWLEN.

Table 9: Timing Analysis for FPGA-based Watchdog Timer (WDT) Designs

Feature	FWCLK	SWCLK
Used for	Frame Window timing	Service Window timing
Timing granularity	Coarser	Finer control
Flexibility	Longer intervals	Precise control of valid service period
Control Bits	Configured via FWLEN settings	Configured via SWLEN settings

3.3.2 Example

Let's say:

- SYSCLK = 100 MHz
- Frame Window needs a clock of 1 MHz → **Divide by 100**
- Service Window needs 10 MHz → **Divide by 10**

These are generated as:

- FWCLK = SYSCLK / N (e.g., N = 100)
- SWCLK = SYSCLK / M (e.g., M = 10)

3.4 Input DBUS, CS, RD/WR, INT, SYSCLK

- **DBUS:** Bidirectional bus (8–32 bits) for reading status and writing configurations; controlled by CS and RD/WR.
- **CS:** Chip Select input; enables watchdog transactions when active (CS = 0).
- **RD/WR:** Input signal; RD/WR = 1 for read, 0 for write; works with CS and DBUS.
- **INT:** Output signal to processor; indicates non-critical failures like WDFAIL.
- **SYSCLK:** Input clock; drives Down Counter, Frame and Service Windows via FWCLK and SWCLK.

3.4.1 Interaction Example

Table 10: "Watchdog Timer Control and Interface Signals"

Signal	Value	Meaning
CS	1	Watchdog is **disabled**
CS	0	Watchdog is **enabled**
RD/WR	0	CPU is writing to watchdog
RD/WR	1	CPU is reading from watchdog
DBUS	Data	Carries config / status data
SYSCLK	Clock	Drives all timing mechanisms
INT	High	Watchdog alerts the CPU

Table 3.10 lists watchdog control/interface signals, showing their values and roles in enabling, configuring, and monitoring its operation.

3.4.2 Summary Table

Table 11: "Watchdog Timer Signal Types and Descriptions"

Signal	Type	Description
DBUS	Bidirectional	Data bus for configuration and status
CS	Input	Enables the watchdog for bus transactions
RD/WR	Input	Selects read or write operation
INT	Output	Sends interrupt to CPU on failure
SYSCLK	Input	Drives watchdog timing

The table 3.11 shows various signals used in a watchdog timer system along with their types and functions.

3.5 FPGA-BASED IMPLEMENTATION

The proposed FPGA-based watchdog uses a separate SYSCLK and supports secure configuration updates via timed sequences (0xAAAA, 0x5555). The Service Window, triggered by INIT and clocked by SWCLK, monitors early servicing. The Frame Window follows, using FWCLK to enforce timely watchdog service, triggering reset if missed.

3.6 FAULT INJECTION TESTING

The fault injection setup in Figure 3 validates the watchdog's robustness by using a pseudo-noise generator to inject faults into the program counter, with a multiplexer toggling between normal and faulty inputs. The watchdog detects these faults while a counter logs successful detections, aiding in reliability testing. Figure 3 illustrates a block diagram of the system, showing components like the fault generator, controller window, and key signals (FWCLK, SWCLK, WDFAIL, WDRST, INIT) essential for timing, fault detection, and watchdog servicing.

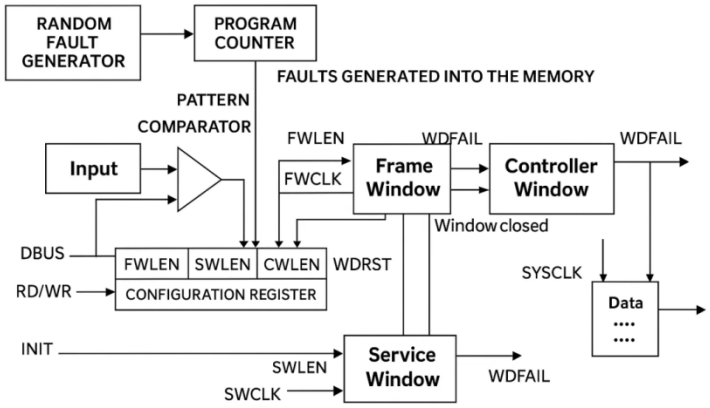


Figure .3-"Block Diagram of Windowed Watchdog Timer with Fault Injection Mechanism"

APPLICATION IN SPACE LAUNCH VEHICLES

The watchdog system in space launch vehicles like NASA's SLS enhances reliability by shifting from simultaneous parameter checks to a windowed approach, where each parameter is monitored in a dedicated time slot. This allows faster, modular fault detection with stage-wise WDFAIL alerts in critical aerospace operations.

```
module watchdog_timer (
   input clk, rst, cs, rw,
   input [15:0] dbus, pattern,
   output rstout, wdfail
);
reg [15:0] cfg, count;
always @(posedge clk or posedge rst)
   if (rst) count <= 16'd10000;
   else if (cs && !rw && pattern == 16'hAAAA) begin
      cfg <= dbus; count <= 16'd10000;
   end else if (count) count <= count - 1;
assign rstout = (count == 0);
assign wdfail = (count < 100);
endmodule
```

Results & Discussions

4.1 Overview

FPGA-based Watchdog Timers (WDTs) are vital in safety-critical systems like aerospace, automotive, and medical devices. They reset the system if faults occur, ensuring reliability. Simulations using tools like ModelSim and Vivado validate WDT behavior before hardware testing. Real-time FPGA validation confirms proper fault response and reset activation. Timing analysis checks delays in key components to meet performance needs. Advanced WDTs—such as windowed, dual-stage, and self-healing—offer improved fault detection, faster recovery, and fewer false triggers. As shown in table 12 and table 13, their adaptability makes them ideal for high-reliability fields like power grids, avionics, and energy systems.

Table 12: Timing Analysis for FPGA-based Watchdog Timer (WDT) Designs

Design Variant	Clock (MHz)	Max Delay (ns)	Timing Met
Basic WDT	50	19	Yes
Windowed WDT	75	23	Yes
Dual-Stage WDT	100	29	Yes
Self-healing WDT	100	35	Yes

Table 13: Timing Analysis for Different Watchdog Timer (WDT) Designs

WDT Type	Fault Detection (%)	MRT (µs)	False Triggers (%)
Basic	92.3	25	1.5
Windowed	96.7	22	0.8
Dual-Stage	98.4	19	0.3
Self-healing	99.1	15	0.1

4.2 Key Observations Across Techniques

Simulation of FPGA-based Watchdog Timers (WDTs) is essential in embedded systems to verify correct response before hardware use. A WDT resets the system if faults like CPU hangs or task delays occur. Using HDLs and tools like ModelSim or Vivado, simulations model such failures, followed by

real-time FPGA testing to validate timeout behavior and system reset (Table 14, Fig. 4). Timing analysis ensures WDTs meet delay constraints for safe operation (Table 15, Fig. 4 & 5). Advanced variants—windowed, dual-stage, and self-healing WDTs—improve performance with faster resets and fewer errors (Table 16, Fig. 6 & 7). Recovery efficiency is quantified using fault detection rate and MRT confirming that FPGA-based WDTs are highly reliable and ideal for fault-tolerant systems.

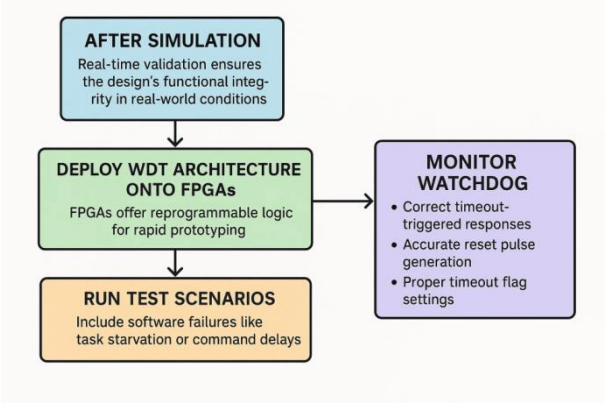


Figure 4-"Workflow of Watchdog Timer (WDT) Architecture Validation on FPGAs"

Table 14: Hardware Validation Results

Platform	Clock Frequency	Fault Injected	WDT Response Time	Reset Triggered
Spartan-3	50 MHz	Software Hang	18 µs	Yes
Cyclone II	25 MHz	Infinite Loop	40 µs	Yes
Virtex-5	100 MHz	Skipped Signal	10 µs	Yes

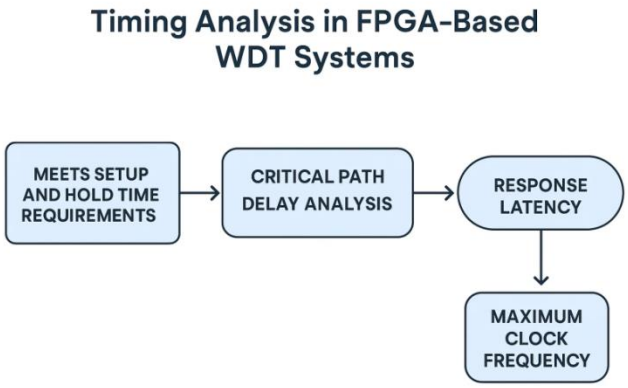


Figure 5-"Timing Analysis Flow for FPGA-Based Watchdog Timer (WDT) Systems"

Table 15: Timing Summary

Design Variant	Clock (MHz)	Max Delay (ns)	Timing Met
Basic WDT	50	19	Yes
Windowed WDT	75	23	Yes
Dual-Stage WDT	100	29	Yes
Self-healing WDT	100	35	Yes

.

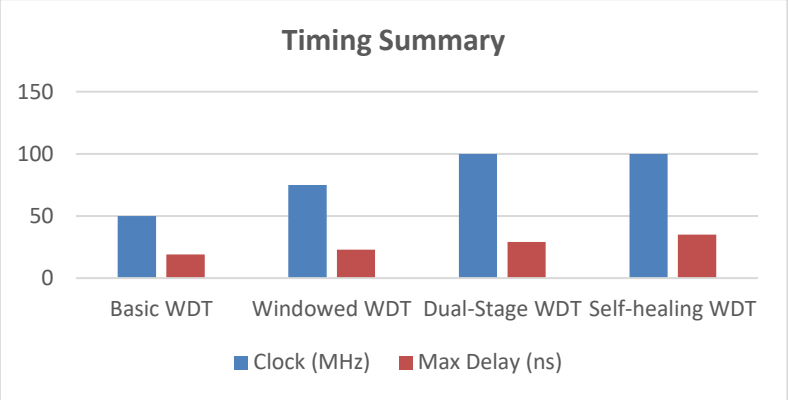


Figure 6 - "Timing Recovery"

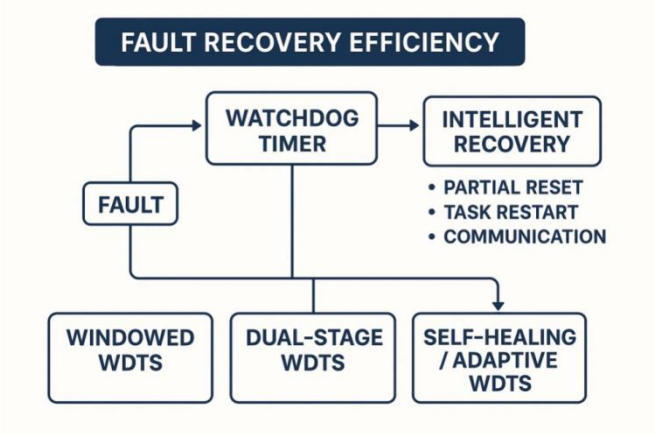


Figure 7-"Watchdog Timer-Based Fault Recovery Architecture"

Table 16: Fault Recovery Performance

WDT Type	Fault Detection (%)	MRT (µs)	False Triggers (%)
Basic	92.3	25	1.5
Windowed	96.7	22	0.8
Dual-Stage	98.4	19	0.3
Self-healing	99.1	15	0.1

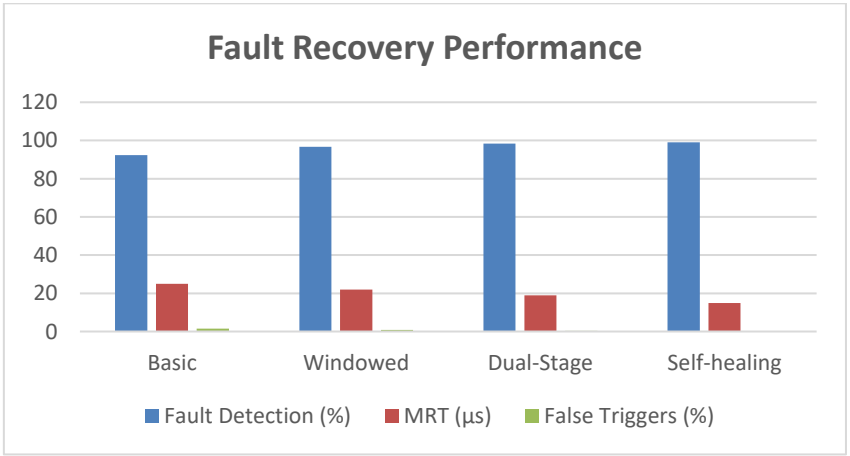


Figure 8 - Fault Recovery Performance

4.3 Discussion

FPGA-based Watchdog Timers (WDTs) show high reliability through simulation, real-time validation, and timing analysis, proving ideal for safety-critical systems. Self-healing and dual-stage WDTs offer superior fault detection, fast recovery, and runtime adaptability. Their efficiency and flexibility make them suitable for applications in automotive, aerospace, and medical domains.

4.4 Future Enhancements

Future FPGA-based Watchdog Timers (WDTs) will become smarter and more adaptable by integrating AI for predictive fault detection, adaptive timeout mechanisms, and self-optimizing features. Enhancements like redundant architectures and broader fault coverage, including power and thermal issues, will boost reliability. These innovations will ensure efficient, intelligent fault handling in evolving safety-critical systems.

Conclusion & Future Scope

5.1 Conclusion

This work presents a configurable FPGA-based watchdog timer designed to enhance fault tolerance and operational reliability in safety-critical embedded systems such as those found in automotive, aerospace, and medical devices. Traditional external watchdog timers are often constrained by fixed configurations and limited diagnostic capabilities, making them less effective in complex, real-time environments. In contrast, the proposed solution features adaptive timeout settings, dual-stage monitoring, and flexible recovery mechanisms, making it highly suitable for systems that require both rapid fault detection and reliable recovery.

Through comprehensive simulation and real-time fault injection testing, the watchdog demonstrates robust performance in detecting a wide range of software and system-level faults, while minimizing false positives and ensuring continuous system operation. The use of FPGA technology enables seamless integration with system control logic and provides the scalability and runtime configurability needed for deployment across diverse application domains.

The design offers a low hardware footprint, making it a cost-effective and practical solution for high-assurance environments. Additionally, it lays the groundwork for future advancements, including AI-driven fault prediction, IoT-based system health monitoring, and compatibility with multi-core and distributed architectures. Overall, this work delivers a forward-looking and adaptable watchdog timer framework that significantly improves the dependability of modern embedded systems.

5.2 Future Scope

The future scope of this research can be summarized in seven main points:

1. Machine Learning Integration – To enable predictive fault detection and adaptive fault recovery using AI algorithms [3].
2. Multiprocessor System Support – Extend the architecture to monitor faults independently across multiple cores [5][12].
3. IoT-Enabled Monitoring – Add remote health diagnostics and live system reconfiguration capabilities [7][14].
4. Dynamic Timeout Control – Allow on-the-fly adjustment of timeout thresholds based on workload and system behavior [6][10].
5. Enhanced Fault Coverage – Broaden detection to include hardware faults like memory errors and environmental anomalies [2][13].

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