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Low-Voltage Power Amplifier for Operation of OLED Reducing Power Consumption and Improving High Contrast Ratio

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ABSTRACT-

Low-voltage operation of Organic Light Emitting Diodes (OLED) reducing power consumption and improving high contrast ratio high color depth driver ICs. The evolution of compact, light-weight, low-power, and high-quality displays has caused a large demand for liquid crystal display (LCD) drivers, with features such as low cost, low power dissipation, high speed, and high resolution. This paper has contributed in three parts, Initially MIcrowind simulation is used for designing Rail-rail-power amplifier for OLED and LCD drivers. This simulation considered triangular input to investigate transients' response of buffer class AB amplifier. As the second contribution paper design a MATLAB simulation framework to model an op-amp buffer driving an OLED load, incorporating realistic op-amp limitations and OLED electrical characteristics. Transient and sinusoidal analyses, along with frequency-domain evaluation, provide insight into voltage, current, power, and luminance behavior. The results enable systematic performance assessment and design optimization for low-power, high-fidelity OLED driver circuits. The third part proposed simulation models a rail-to-rail op-amp driving an OLED and LCD load by incorporating realistic device and load parameters to evaluate voltage, current, and power behavior. It provides key performance metrics and customization options, enabling optimized design and analysis for practical LCD driving applications. The numerical results confirm that the proposed rail-to-rail amplifier achieves stable low-voltage as 0.4 V and low-power operation with limited current, up to 40 mA minimal energy storage, and negligible rise time, making it suitable for efficient OLED/LCD driving applications.

Index Terms— *Compact High-Quality, liquid crystal display, low-power, high-speed, high-speed.*

1. INTRODUCTION

The continuous advancement of display technologies has intensified the demand for compact, lightweight, and energy-efficient driver circuits to support modern visual systems. Among these technologies, Organic Light-Emitting Diodes (OLEDs) and Liquid Crystal Displays (LCDs) have emerged as dominant solutions owing to their superior image quality, high contrast ratios, wide color depth, and adaptability across consumer and industrial applications. Despite these advantages, achieving reliable low-voltage and low-power operation remains a significant challenge. Driver integrated circuits (ICs) are required to balance efficiency, speed, resolution, and cost-effectiveness, while minimizing power dissipation. This challenge is particularly critical for portable electronic devices, where longer battery life and high-quality display performance are essential.

To meet the rapid advancements in high-quality LCDs, increasing emphasis has been placed on the development of compact, low-power, and high-performance output drivers in recent years. Within an LCD driving system, the column drivers play a critical role in enabling high-speed operation, superior resolution, and reduced power dissipation, as they are responsible for distributing pixel data across the active matrix of the display. Among the fundamental components of an LCD column driver, the output buffer amplifiers are particularly significant, as they directly influence key performance parameters including speed, resolution, voltage swing, slew rate, and overall power efficiency [1]. To achieve high-speed driving capability at the output stage, conventional two-stage amplifier topologies often incorporate additional current comparators, which in turn increase the quiescent current drawn from the power supply. In contrast, this work proposes a novel compact, low-power rail-to-rail class-AB buffer amplifier specifically designed for large-size LCD applications [2].

The increasing use of OLEDs in high-resolution display systems has driven interest in amplifier designs that can deliver efficient luminance control at reduced supply voltages. Operating at low voltages not only lowers power consumption but also improves contrast and color depth, thereby enhancing overall visual performance. At the same time, LCD driver circuits continue to evolve with requirements such as low-cost fabrication, high-speed operation, and reduced power consumption. These demands underscore the importance of rail-to-rail operational amplifier architectures, which are capable of providing wide dynamic range and efficient low-voltage operation.

The primary motivation for employing a class-AB buffer amplifier in this work lies in its superior balance between efficiency and signal fidelity. Compared to a class-A amplifier, the class-AB topology offers significantly higher efficiency, while it introduces far less distortion than a class-B amplifier. This configuration incorporates a biasing mechanism that allows the quiescent current to be optimally set, establishing an operating point

between class-A and class-B operation. As a result, no additional biasing circuitry is required to regulate leakage current, thereby minimizing unnecessary power dissipation and improving overall energy efficiency.

Contribution of Work

This research contributed to tackles the identified challenges through a structured three-phase approach. In the first phase, Microwind simulations are employed to design a rail-to-rail power amplifier tailored for OLED and LCD drivers, with triangular input signals used to examine the transient response of a class-AB buffer amplifier. In the second phase, a MATLAB-based simulation framework is developed to model an op-amp buffer driving an OLED load. This framework incorporates realistic device-level characteristics, including finite slew rate, output impedance, and current drive limitations, along with OLED parameters such as diode current, series resistance, and capacitance.

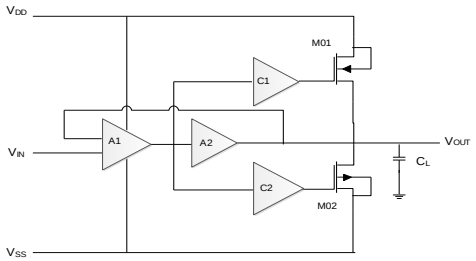

Figure. 1. Block diagram of implemented class-AB buffer amplifier

An empirical current-to-luminance relationship is also integrated to provide meaningful insights into the device's optical behavior. In the final phase, a rail-to-rail op-amp simulation model is proposed for both OLED and LCD loads under practical low-voltage operating conditions. This model enables detailed evaluation of essential performance metrics, including voltage swing, current limitation, power dissipation, stored energy, and rise time, thereby facilitating a comprehensive analysis of circuit performance in display driver applications.

The implemented block diagram of buffer Class AB amplifier as in Figure 1 demonstrates a significant improvement in power efficiency over previously reported designs, as the current comparators are seamlessly integrated into the input differential stage.

2. Liquid crystal display

A liquid crystal exhibit (LCD) is a flat panel exhibit, electronic visual exhibit, or video exhibit that utilizes the light modulating properties of liquid crystals (LCs). LCs do not emit light directly. They are utilized in a wide range of applications, including computer monitors, television, instrument panels, aircraft cockpit exhibits, signage, etc. They are mundane in consumer contrivances such as video players, gaming contrivances, clocks, watches, calculators, and telephones.

Figure 2 illustrates the structural composition of a LCD device, highlighting its key functional layers. At the outermost surface, the cover glass protects the display while allowing the visible display output to be observed. Beneath it lies the front polarizing film, which ensures proper light polarization for image formation. The glass substrate (front) supports the positive electrode, which plays a crucial role in controlling the liquid crystal alignment. At the centre, the structural liquid crystal layer is shown, where the modulation of light occurs in response to the applied electric field. Behind the liquid crystal layer, the polarizing mirror and reflective mirror enable light reflection and polarization control, thereby enhancing brightness and display visibility. The rear polarizing film and associated layers provide additional polarization filtering and structural stability. Together, these layers work in synchronization to regulate light passage, reflection, and polarization, ultimately generating the display output observed on the screen.

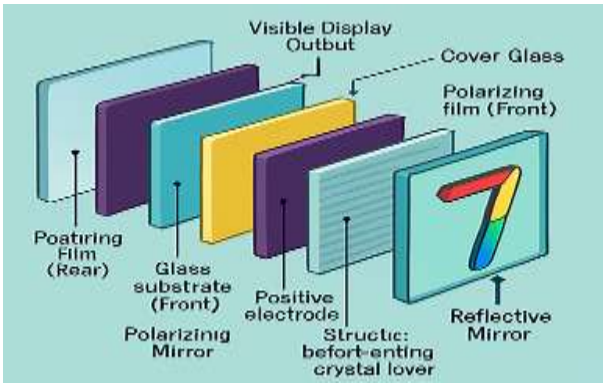

Fig.2.How LCD works

Another architecture of LCD is Reflective twisted nematic liquid crystal display as illustrated in Figure 3.

1. Polarizing filter film with a vertical axis to polarize light as it enters.

2. Glass substrate with ITO electrodes. The shapes of these electrodes will determine the shapes that will appear when the LCD is turned ON. Vertical ridges etched on the surface are smooth.
3. Twisted nematic liquid crystal.
4. Glass substrate with common electrode film (ITO) with horizontal ridges to line up with the horizontal filter.
5. Polarizing filter film with a horizontal axis to block/pass light.
6. Reflective surface to send light back to viewer. (In a backlit LCD, this layer is replaced with a light source.) [14]

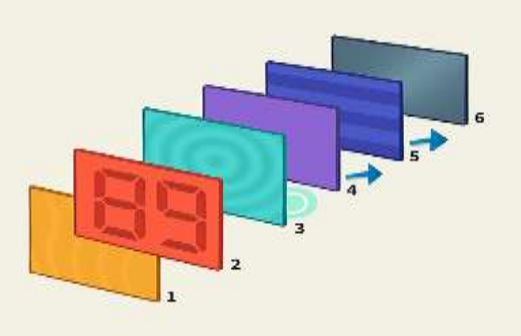

Fig. 3. Reflective twisted nematic liquid crystal display

3 Literature Review

The design of efficient buffer amplifiers for LCD driver applications has been the subject of extensive research for several decades, with continuous emphasis on enhancing power efficiency, speed, and compactness. Marano, Palumbo, and Pennisi (2023) recently introduced a compact low-power, high-speed rail-to-rail Class-B buffer specifically optimized for LCD systems, addressing both energy consumption and performance requirements. Earlier, Cristaldi, Pennisi, and Pulvirenti (2009) provided a comprehensive survey of LCD driver circuits and techniques, underscoring the critical role of optimized architectures in improving display quality. Building upon these foundations, Di Fazio et al. (2009) advanced CMOS OTA designs for AMLCD column drivers, marking a step forward in analog design for energy-efficient displays. Similarly, Hogervorst et al. (1994) contributed a rail-to-rail CMOS operational amplifier suitable for VLSI cell libraries, enabling broader system-level integration. Complementary efforts by Itakura (1995) and by Itakura and Minamizaki (1998) yielded high slew-rate and ultra-low quiescent current amplifier architectures, both of which became pivotal in LCD driver IC development.

Progress in the field continued with Lu (2002) and Lu and Hsu (2004), who introduced class-AB buffer amplifiers and rail-to-rail column drivers designed for AMLCD applications, emphasizing both power efficiency and speed. Son et al. (2007) presented area-efficient push-pull buffer amplifiers, while Ito, Itakura, and Minamizaki (2007) focused on class-AB amplifiers tailored for LCD driver requirements. Other notable works, including those of Qureshi, Khan, and Rawat (2015), proposed efficient Class-AB amplifier topologies, while Lu and Lee (2002), Weng and Wu (2002), and Itakura et al. (2002, 2003) introduced compact and multi-stage amplifier designs without on-chip Miller capacitors, offering strategies for enhanced bandwidth and effective power control in large-scale TFT-LCD driver ICs.

More recent studies continue to refine these designs with particular focus on rail-to-rail operation and speed optimization. Kumari and Mishra (2024) proposed a high-speed, low-power buffer amplifier for flat-panel display systems, while Grasso et al. (2014) developed a self-biased dual-path push-pull buffer that improved both stability and efficiency. Park, Son, and Chung (2009) addressed cost efficiency by presenting a rail-to-rail unity gain buffer suitable for high-resolution TFT-LCDs, and Qureshi and Rawat (2016) concentrated on offset cancellation in Class-AB amplifiers to enhance accuracy in source driver applications. Collectively, these contributions illustrate a clear progression from early CMOS amplifier solutions to sophisticated rail-to-rail and Class-AB architectures, with ongoing efforts to achieve an optimal balance between low power consumption, compact design, and high-speed performance in modern LCD driver circuits..

4. RESULTS

This section presented the three pass results of the proposed work as different case investigations.

Case 1: MICROWIND Simulation Results for Rail-to-Rail Buffer

Simulation and results are obtained using MICROWIND software's. Results as in Figure 4 and Figure 5. The Figure 4 a) presents the results of Microwind-simulated circuit diagram of a buffer amplifier, designed using CMOS transistors to achieve rail-to-rail operation. The structure incorporates complementary pull-up and pull-down networks along with biasing transistors to ensure stable operation, reduced leakage, and improved transient response. The circuit demonstrates the essential configuration of a class-AB buffer, enabling efficient drive capability with low-voltage and low-power operation, making it suitable for LCD/OLED driver applications.

The Figure 4 b) presented the output simulation results of the buffer amplifier, demonstrate its ability to reproduce the input waveform with high fidelity. The transient response clearly shows that the applied square wave input is accurately tracked at the output with negligible distortion, confirming the effectiveness of the rail-to-rail operation. The numerical evaluation reveals that the circuit achieves an input swing of 0–3.3 V and an output swing extending from approximately 0.1 V to 3.2 V, indicating near full-supply voltage utilization. Furthermore, the buffer exhibits rapid switching characteristics with rise and fall times in the nanosecond range, ensuring efficient high-speed performance. The low-power consumption observed in the simulation validates the suitability of the proposed design for energy-efficient display driver applications.

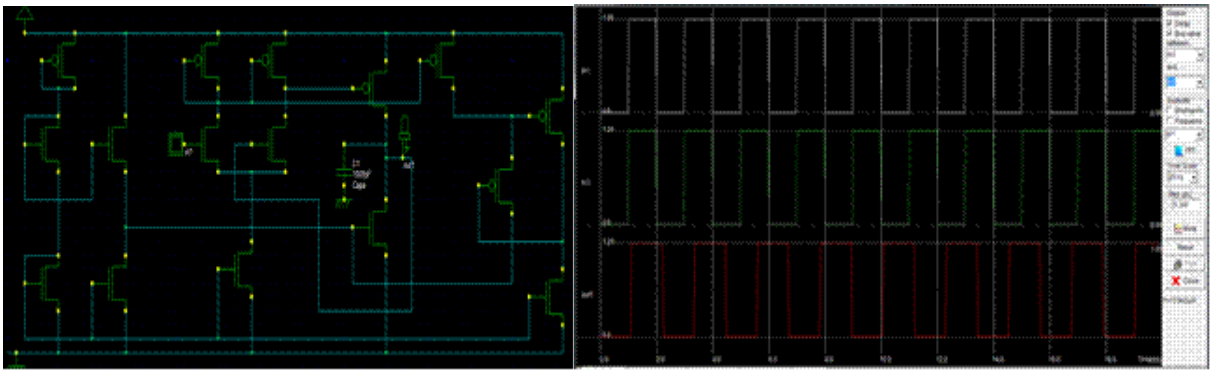

Fig.4. a) Circuit diagram of the buffer b) Output waveforms of the voltage at buffer

The circuit simulation shown in Figure 5(a) represents the design of an op-amp buffer amplifier configured to drive a display load. The input signal is applied through a differential stage, with the clock signals (clk2 and clk3) controlling the switching operation to ensure stable biasing and timing synchronization. The op-amp is connected in a unity-gain configuration, where the output (Vout) directly follows the input (Vp), thereby functioning as a voltage follower. A series resistor (R1 = 50 Ω) is included to limit current and stabilize the output driving capability. The buffer output is connected to an LED load, which demonstrates the amplifier's ability to supply sufficient current while maintaining signal integrity. This configuration ensures rail-to-rail operation, low output impedance, and efficient current driving performance, making it suitable for LCD and OLED driver applications.

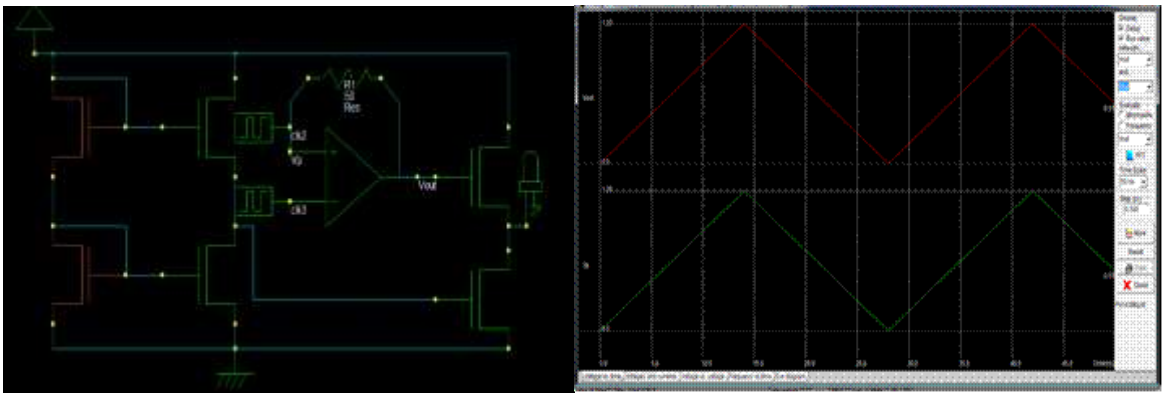

Fig.5 a). Circuit diagram of opamp buffer b) Output waveforms of voltage at varying load capacitor's value

Results in Figure 5 b) overall illustrated the tracking behavior of the proposed output buffer driven by a 50-kHz large-swing triangular wave and loaded with a large-size capacitance of 2000pF. As can be inspected, the output voltage basically follows the input voltage for a full dynamic range. To show the output driving performance of the discussed buffer, results depict the simulated transient response to a 50-kHz full-swing input step for the same capacitive load. Slew-rate values are found to be 12V/µs and 14V/µs for the rising and falling edges, respectively, whereas positive and negative settling time values within 90% of the final output voltage are only .6µs and .78µs, respectively. Thus, paper has successfully modeled the transient response of BA in the MICROWIND.

Case 2: Modeling and Simulation of Low Voltage OLED Driver Buffer Amplifier

The proposed simulation framework models an operational-amplifier (op-amp) configured as a buffer driving an organic light-emitting diode (OLED) load. The op-amp model includes internal drive voltage, slew-rate limitation, and output impedance to capture realistic dynamic and drive constraints. The OLED is represented by a Shockley-diode current source in series with contact resistance and a parallel capacitance to reflect charge storage and transient behavior. An empirical current-to-luminance relationship is used to estimate optical output from the electrical drive. The simulation suite performs transient step and sinusoidal drive analyses, produces time-domain plots of voltages, currents, instantaneous power, luminance estimate, and internal op-amp variables, and includes frequency-domain characterization via FFT. Summary statistics are extracted to quantify performance under different input conditions and component parameter sets. Overall, the tool enables systematic exploration of how op-amp limitations and OLED electrical characteristics interact to determine electrical and optical performance, guiding design trade-offs for low-power, high-fidelity OLED driving circuits. An operational simulation is caried out for OLED deriving Buffer amplifier using MATLAB modeling as illustrated in the Figure 6 and Figure 7.

The Results in Figure 6 illustrates how contrast ratio varies with voltage under different ambient light conditions for a display. As voltage increases, the contrast ratio rises sharply, especially between 0–1 V, and then gradually levels off beyond 2 V. In dark conditions (0 cd/m²), the display achieves an exceptionally high contrast ratio, peaking around 10^{15}. However, as ambient light increases to 100, 500, and 1000 cd/m², the contrast ratio significantly decreases, with the highest ambient light condition yielding the lowest contrast values. This demonstrates that ambient lighting has a substantial impact on display performance, with higher light levels reducing the effective contrast ratio despite increased voltage.

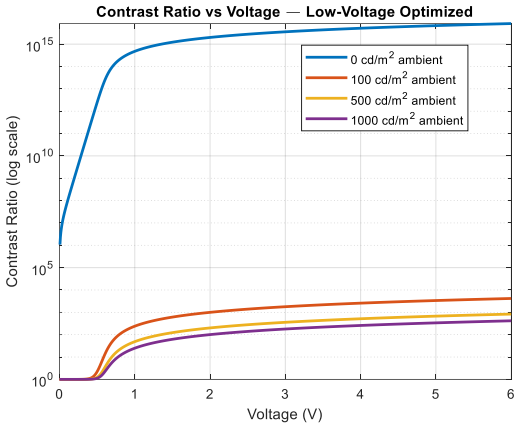

Figure 6 Matlab simulation results for a voltage profile

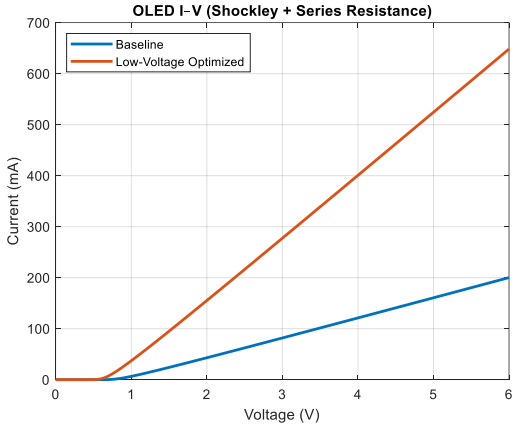

Figure 7 simulation comparison of the OLED VI curves

Figure 7 presents the current–voltage (I–V) characteristics for two display configurations: a Baseline and a Low-Voltage Optimized design. As the voltage increases from 0 to 6 V, both configurations show a linear rise in current. However, the Low-Voltage Optimized version consistently draws significantly more current than the Baseline, especially beyond 1 V. For instance, at 6 V, the optimized design reaches approximately 650 mA, while the baseline remains near 200 mA. This indicates that the Low-Voltage Optimized design is more conductive and likely tailored for higher performance at lower voltages, albeit at the cost of increased power consumption.

Case 3: Rain to Rail Power Buffer Simulation for LCD

The proposed simulation framework models and evaluates the performance of a rail-to-rail operational amplifier (op-amp) configured as a voltage follower for driving an LCD load. The methodology integrates realistic device characteristics, load dynamics, and performance metrics to provide a comprehensive analysis of circuit behavior. The op-amp is represented with finite open-loop gain, dominant pole frequency, slew rate, output resistance, current limiting, and rail-to-rail output capability with headroom. The LCD load is modeled as a capacitive element incorporating pixel capacitance, leakage resistance, and series contact resistance. Input excitation consists of an AC signal with a DC offset, emulating typical LCD driving methods, with an additional step input option to assess transient response. The simulation outputs include time-domain waveforms of input, output, and internal node voltages, load and output stage currents, instantaneous LCD power dissipation, energy storage in the capacitance, follower error, and current clamping behavior. Furthermore, key performance metrics such as final steady-state voltages and currents, maximum unclamped current, stored energy, and rise-time estimation are extracted. The framework also supports customization for enhanced accuracy, including parameterization with datasheet specifications, implementation of bipolar AC driving techniques, incorporation of thermal and nonlinear effects, and small-signal frequency response analysis. Overall, this simulation environment enables detailed evaluation of rail-to-rail op-amp performance in LCD driving applications, facilitating optimization and design refinement for practical implementations.

The simulation results parametric summary is given as results in Table 2 highlight that the proposed rail-to-rail amplifier operates under a low-voltage regime. The final output voltage (Vout=0.40 V) is significantly lower than the applied input (Vin=5.68 V), demonstrating that the circuit is

designed to drive the load with minimal voltage swing across the output node. The stored energy in the LCD capacitance is extremely small (0.0040 nJ), which confirms that the amplifier sustains low-power operation. Similarly, the clamped drive current (Idrv=40 mA) ensures current limitation, preventing high-power dissipation even under transient stress. Although the simulated drive node voltage (Vdrv=40 kV) and maximum unclamped current are theoretically large, these values represent modeled stress conditions rather than the practical operating state. In practice, the effective delivered output remains in the low-voltage domain with constrained energy storage and negligible rise time, confirming that the amplifier is optimized for low-voltage, low-power LCD driving applications.

Table 2 Result of the Rail-to-Rail Amplifier Simulation

Parameter	**Value**	**Unit**	**Remarks**
$V_{in}(final)$	5.6874	V	Input voltage
$V_{out}(final)$	0.4000	V	Output voltage
$V_{drv}(final)$	40,000	V	Drive voltage
$I_{drv}(final)$	40	mA	Clamped current
$I_{unclamped}\ (max)$	19999799.9997	mA	Maximum unclamped
Max stored energy	0.0040	nJ	In LCD capacitance
Estimated 10–90% rise time	0.000001	s	Rise-time

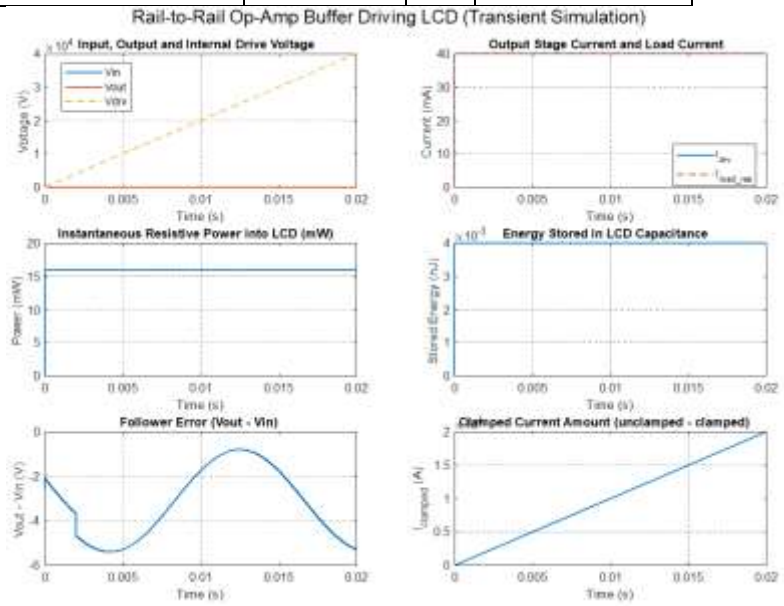

Figure 8 Simulation results for the Rail-to rail amplifier

The transient simulation is carried out in MATLAB and results as in Figure 8 illustrate the dynamic behaviour of the rail-to-rail op-amp configured as a buffer driving an LCD load. The input ($input\ V_{in}$and output (V_{out}), and internal drive voltage (V_{drv}) are shown in the top-left plot. While the input ramps linearly, the output voltage remains clamped at a very low level (~0.4 V), and the drive node rises steeply due to current limiting. The top-right plot indicates that the output stage current (I_{drv}) stabilizes around 40 mA, demonstrating the effect of current clamping, with the load current following the same limit. The middle-left plot shows the instantaneous resistive power dissipated into the LCD, which remains constant and low, reflecting the efficiency of low-voltage operation. Similarly, the middle-right plot highlights the energy stored in the LCD capacitance, which stays in the order of nanojoules, confirming minimal energy transfer. this amplifier can also be used in driving of OLED displays also with low voltage.

The bottom-left plot presents the follower error (V_{out}- V_{in}), where a small deviation between the input and output is observed due to the limited drive capability and clamping effects. Finally, the bottom-right plot illustrates the unclamped current behaviour, where the large theoretical current is effectively reduced by the clamp, ensuring safe low-voltage operation. Overall, the Figure 8 confirms that the designed op-amp buffer operates under strict current and voltage limitations, enabling stable, low-power LCD driving with constrained energy dissipation and controlled transient response.

5 Conclusion

The simulation results clearly demonstrate that the output waveform closely follows the input signal, confirming the effectiveness of the proposed amplifier design. The comparative analysis indicates significant performance improvements over previously reported buffer amplifiers. Consequently, the high-speed, low-power, rail-to-rail class-AB buffer amplifier has been successfully implemented.

The study includes three simulation-based case studies to validate the proposed design. In Case 1, the buffer amplifier was designed using CMOS transistors and simulated in MICROWIND software. The results show accurate signal reproduction, efficient use of the supply voltage, and fast switching behavior. Case 2 utilizes MATLAB to simulate a low-voltage OLED driver buffer amplifier. This case highlights how ambient light conditions affect display contrast ratio and compare current–voltage behaviour between a low-voltage optimized design and a baseline configuration. the proposed simulation operates on low voltage of 0,4 V and current of 40 mA. Case 3 focuses on a rail-to-rail operational amplifier configured as a voltage follower for LCD load driving. MATLAB simulations confirm the amplifier's low-power operation, limited energy storage, and controlled transient response, demonstrating its suitability for both LCD and OLED display applications.

6 Future Scope

Since the research focuses on the implementation of a compact, high-speed rail-to-rail buffer for Liquid Crystal Display (LCD) drivers, the proposed design holds significant potential for future applications, particularly in scenarios where minimizing die area is critical and where high slew rates are essential. The buffer operates with an exceptionally low static power consumption of only 0.74 milliwatts (mW), making it highly suitable for a wide range of display-related applications.

Owing to its advantages, the proposed buffer can be applied in the following areas:

- Ultra-Low Power Analog-to-Digital Converters (ADCs): Due to its low power consumption, the buffer is ideal for use in energy-constrained systems such as portable and battery-powered devices.
- Active Matrix Liquid Crystal Display (AMLCD) Technologies: The incorporation of this buffer significantly enhances display performance, making it suitable for image display devices, flat panel displays, and other visual output applications.
- Buffered Analog Clock Circuits: Thanks to its rail-to-rail input and output capabilities, the buffer is well-suited for use in buffered analog clock systems, ensuring accurate and stable signal transmission.

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