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# AI for Computational Lithography: ILT/OPC Acceleration and Quality

***Md Abdulla Ahmed Mazumdar***

Swadhin Bazar High School

**ABSTRACT**

The scaling of semiconductor technology into the sub-5 nm regime has intensified the challenges of computational lithography, where inverse lithography technology (ILT) and optical proximity correction (OPC) play a pivotal role in mitigating distortions during pattern transfer. However, conventional OPC suffers from limited accuracy under extreme ultraviolet (EUV) variability, while ILT provides superior fidelity at the expense of prohibitive runtimes and manufacturability penalties. To address this tradeoff, we propose an AI-accelerated hybrid computational lithography framework that integrates deep inverse modeling, learning-to-optimize strategies, and physics-guided surrogate models.

Using three representative layout clips and full-chip test cases, the framework demonstrated runtime reductions exceeding 10× compared to ILT while maintaining mask error rates (MER) near 2%, a substantial improvement over conventional OPC. At the full-chip scale, the method achieved runtimes comparable to OPC (~17–18 hours) but retained ILT-level accuracy (~2.1% MER). Robustness evaluations under EUV stochastic variability further revealed that the hybrid framework achieved process window area (PWA) values of 77–79%, close to ILT, while constraining shot count inflation to ~1.15×, significantly reducing mask writing complexity.

These results establish the proposed framework as a scalable, accurate, and manufacturable solution for next-generation OPC/ILT acceleration. By explicitly addressing efficiency–accuracy tradeoffs, scalability limitations, and EUV-specific variability, this work contributes a practical AI-enabled pathway toward high-volume EUV manufacturing.

## 1. Introduction

The semiconductor industry has been guided for decades by the predictive power of Moore's law**,** which has forecast the doubling of transistor density approximately every two years. This exponential trajectory of scaling has been instrumental in enabling technological breakthroughs, from personal computing to mobile communications and large-scale data centers. However, as the industry approaches the sub-3 nm technology nodes, fundamental physical and economic barriers are challenging the continuation of this trend. Lithography**,** the core technology that defines transistor dimensions, lies at the heart of this challenge. With 193 nm immersion lithography reaching its physical resolution limits and extreme ultraviolet (EUV) lithography serving as the current enabler of advanced nodes, the demand for more sophisticated computational techniques to ensure pattern fidelity and manufacturability has never been greater.

Computational lithography the suite of computational techniques designed to compensate for distortions in the lithographic imaging process has emerged as a cornerstone of modern semiconductor manufacturing. Within this domain, Inverse Lithography Technology (ILT) **and** Optical Proximity Correction (OPC) represent the two most critical techniques. ILT offers a mathematically optimal solution to generate curvilinear mask shapes that account for optical and process distortions, while OPC leverages rule-based corrections to enhance print fidelity. Despite their importance, both methods face severe computational bottlenecks**,** especially under EUV conditions. Conventional ILT workflows often require 72–96 hours of computation for industrial-scale layouts, while OPC, though faster, sacrifices accuracy and struggles with process-window robustness at advanced nodes. This creates **a** fundamental trade-off between runtime efficiency and pattern fidelity, threatening the manufacturability of future technology nodes.

A key challenge exacerbating this situation is the stochastic variability inherent to EUV lithography. Unlike deep ultraviolet (DUV) systems, EUV lithography operates with significantly fewer photons per exposure, leading **to** photon shot noise**,** stochastic resist effects**,** and line-edge roughness**.** These phenomena introduce random, non-deterministic variations in pattern shapes, making it increasingly difficult for deterministic ILT/OPC frameworks to guarantee manufacturability. Moreover, EUV masks introduce additional complexities such as 3D mask effects and flare-induced variations, which further complicate simulation accuracy. Collectively, these factors highlight the urgent need for next-generation computational frameworks that can combine speed, accuracy, and robustness under real-world stochastic conditions.

Recent advances in artificial intelligence (AI) and machine learning (ML) provide a transformative opportunity to address these challenges. AI, particularly deep learning and reinforcement learning**,** has demonstrated remarkable capabilities in learning highly nonlinear mappings and optimizing complex design spaces. For computational lithography, this translates into the possibility of directly learning the mapping between target wafer patterns

and optimal mask shapes (deep inverse modeling), approximating computationally expensive optical/resist simulations with neural surrogates**,** and automating parameter tuning in ILT/OPC optimization through learning-to-optimize strategies. Early demonstrations have shown promising results, with convolutional neural networks (CNNs) achieving near-real-time hotspot detection and U-Net architectures predicting mask contours with high fidelity. However, most of these approaches have been validated only on small layout clips and often fail to generalize under EUV-specific stochastic variability, leaving a critical gap between academic demonstration and industrial deployment.

Another dimension of complexity arises from the integration of AI with physics-based models. Purely data-driven approaches, while efficient, risk producing physically inconsistent results, especially in domains such as lithography where Maxwell's equations and resist kinetics impose hard physical constraints. To overcome this, **e**merging physics-guided ML approaches integrate physical priors into training pipelines, ensuring that AI models not only accelerate computation but also adhere to lithography-specific constraints. For instance, physics-informed loss functions have been introduced in mask synthesis models to penalize deviations from simulated aerial images, while hybrid workflows employ AI surrogates to replace selected modules of the lithography pipeline (e.g., aerial image simulation, resist modeling), achieving speedups of 10–50× while maintaining >95% accuracy. These findings highlight the potential of hybrid AI–physics workflows but also underscore the need for systematic frameworks that unify these components for ILT/OPC acceleration.

Despite these advances, significant research gaps remain. First, scalability is a persistent bottleneck: most AI-enhanced approaches are restricted to 2 μm × 2 μm design clips, far smaller than full industrial layouts. Second, robustness under EUV-specific variability remains underexplored, with most demonstrations assuming ideal optical and resist conditions. Third, there is little work on integrating multiple AI strategies deep inverse modeling, physics-guided surrogates, and reinforcement learning—into a single holistic framework that optimizes runtime, mask fidelity, and process window simultaneously. Addressing these gaps is essential for transitioning AI-driven computational lithography from proof-of-concept research to practical deployment in semiconductor fabs.

This study seeks to fill these gaps by presenting a comprehensive AI-driven framework for ILT/OPC acceleration and quality improvement in EUV lithography. The framework is built upon three pillars: (1) deep inverse modeling, where a convolutional U-Net architecture predicts curvilinear mask patterns directly from target wafer layouts; (2) physics-guided surrogate models**,** which approximate computationally expensive modules such as aerial image and resist development simulations with high fidelity; and (3) learning-to-optimize frameworks**,** where reinforcement learning agents dynamically tune lithography parameters to balance runtime efficiency, process-window robustness, and mask error rates. Together, these components form a hybrid pipeline that leverages the strengths of both AI and physics-based approaches.

The contributions of this work are threefold. First, it demonstrates that AI-enhanced ILT can achieve a 4× reduction in runtime without compromising accuracy, as evidenced by the results in Table 1 and Fig. 1. Second, it shows that AI-driven frameworks can improve mask fidelity, reducing mask error rates by 18% relative to OPC and 11% relative to baseline ILT **(**Table 2, Fig. 2**)**. Third, it establishes that AI can significantly enhance process window robustness**,** delivering a 22% improvement in dose–focus latitude coverage under EUV conditions **(**Table 3, Fig. 3**).** Collectively, these results highlight the transformative role of AI in computational lithography, offering a viable path toward sustaining semiconductor scaling in the post-Moore era.

In summary, this introduction situates the research at the intersection of semiconductor manufacturing, computational lithography, and AI/ML innovation**.** By addressing the dual challenge of computational expense and EUV variability, this study contributes a scalable and robust AI-driven framework that advances both the theory and practice of ILT/OPC. The remainder of the paper is structured as follows: Section 2 provides a literature review on computational lithography and AI approaches; Section 3 discusses theoretical underpinnings and identifies research gaps; Section 4 details the proposed methodology; Section 5 presents results and discussion; and Section 6 concludes with insights and directions for future research.

## 2. Literature Review

### *2.1 Computational Lithography: Evolution and Current Practices*

Computational lithography has evolved into one of the most critical enablers of advanced semiconductor technology nodes. Initially, the role of computational enhancement in lithography was limited to relatively straightforward resolution enhancement techniques (RETs) such as phase-shift masks, off-axis illumination, and rule-based optical proximity correction (OPC). These techniques relied primarily on linear optical models and rule-based heuristics to compensate for distortions in wafer printing. However, as critical dimensions (CDs) shrank below 45 nm, these conventional RETs proved insufficient in addressing complex optical interactions, prompting the adoption of model-based computational lithography (MBCL) approaches.

Among these, Inverse Lithography Technology (ILT) emerged as a breakthrough methodology. Unlike rule-based OPC, which applied empirical corrections, ILT explicitly formulates mask synthesis as an inverse optimization problem**:** given a target wafer pattern, determine the optimal mask that produces the desired aerial image under lithographic projection. ILT enables curvilinear mask patterns that offer superior fidelity compared to Manhattan-style OPC masks, particularly for 2D layout geometries such as line ends and contact/via arrays. This has been validated in multiple industrial studies, which show that curvilinear ILT can reduce edge-placement error (EPE) by up to 30% compared to OPC and provide superior process window latitude**.**

Despite its advantages, ILT adoption in high-volume manufacturing has been historically limited due to extreme computational demands. Solving the inverse problem requires iterative evaluation of computationally expensive forward lithography models, including aerial image simulation (via Hopkins or Abbe formulations), resist modeling, and optical/etch bias corrections. For full-chip industrial layouts, ILT can consume several terabytes of memory

and require days of compute time even on high-performance computing clusters. This computational bottleneck has restricted ILT to hotspot repair and critical pattern clips**,** rather than full-chip deployment.

With the transition to extreme ultraviolet (EUV) lithography, computational lithography faces new challenges. EUV introduces stochastic effects such as photon shot noise and resist blur, which create non-deterministic patterning errors not captured by classical optical models. Additionally, mask 3D effects and flare variability under EUV conditions increase the complexity of forward models, further extending ILT runtime. At the same time, OPC has shown diminishing returns, as rule-based heuristics fail to account for EUV-specific stochastic variability. This dual challenge rising computational complexity and limited accuracy of OPC heuristics has reinforced the urgent need for hybrid approaches that combine physical accuracy with computational efficiency.

Recent industrial surveys (e.g., SPIE Advanced Lithography, 2021–2024) confirm that computational lithography consumes nearly 50% of overall mask data preparation time at 5 nm and below. Moreover, the introduction of multi-patterning EUV lithography has further stressed computational pipelines. This historical evolution highlights the motivation for exploring AI-accelerated solutions, which aim to reduce ILT runtimes by orders of magnitude while maintaining accuracy under EUV variability.

### *2.2 Machine Learning for Lithography and Mask Synthesis*

The application of machine learning (ML) to lithography has gained substantial momentum in the last decade, driven by the dual forces of increasing data availability (e.g., aerial image libraries, resist simulation databases) and the success of deep learning architectures in other fields such as computer vision. At its core, ML for computational lithography seeks to approximate computationally expensive modules or learn direct mappings between input design patterns and output lithographic results.

One of the earliest applications was hotspot detection, where convolutional neural networks (CNNs) were trained to classify layout regions as lithography-friendly or prone to defects. This task, once handled by rule-based heuristics, achieved dramatic accuracy improvements through CNN classifiers, with reported F1-scores exceeding 95% on industrial benchmarks**.** Similarly, ML models have been used for lithography simulation acceleration, where neural networks approximate aerial image intensity distributions with speedups of 10–50× compared to Hopkins integration, while maintaining errors below 2% relative to rigorous models**.**

The most transformative ML application, however, lies in mask synthesis**.** Deep inverse modeling approaches employ encoder–decoder architectures such as U-Net **or** GANs (Generative Adversarial Networks) to learn the mapping from target wafer patterns to optimized mask layouts. These models bypass iterative ILT optimization and produce candidate masks in near real time. For instance, a recent 2022 study demonstrated that a deep learning model could generate curvilinear masks within minutes compared to 72-hour ILT runs, achieving comparable fidelity under DUV conditions. Extending such approaches to EUV lithography remains challenging but highly promising.

Another frontier is learning-to-optimize strategies, where reinforcement learning (RL) agents dynamically adjust lithography parameters such as dose, focus, and etch bias. Instead of relying on static optimization heuristics, RL frameworks treat lithography as a sequential decision-making process, learning adaptive policies that minimize edge placement error (EPE) or maximize process window area. Several groups have reported 10–15% process window gains using RL-enhanced optimization, showing potential for integration with ILT workflows.

Despite these advances, ML-driven lithography faces three limitations. First**,** generalization across process nodes is limited: models trained at 7 nm often degrade in performance at 5 nm or 3 nm, due to differences in resist behavior and stochastic effects. Second, ML models are data hungry, requiring large simulation datasets for training, which are expensive to generate. Third, purely data-driven approaches risk producing physically inconsistent results, such as masks that cannot be written with current e-beam technologies. These challenges highlight the necessity of integrating ML with physics-based constraints to ensure industrial deployability.

### *2.3 Physics-Guided AI Approaches and Hybrid Workflows*

To overcome the limitations of purely data-driven models, the field has increasingly turned toward physics-guided AI, a paradigm where machine learning models are constrained, informed, or guided by the underlying physical laws of lithography. This hybrid approach balances the speed of AI with the rigor of physics-based simulations**,** creating workflows that are both computationally efficient and physically consistent.

One major direction is the use of physics-informed neural networks (PINNs)**.** These models embed Maxwell's equations and resist kinetics into their loss functions, ensuring that predicted aerial images or mask patterns are consistent with lithography physics. For example, a PINN-based lithography model penalizes deviations from rigorous aerial image simulations during training, enabling the surrogate to approximate the forward model with 10–20× acceleration while maintaining sub-2% error rates.

Another promising direction is hybrid surrogate modeling, where ML models replace selected modules of the lithography pipeline. For instance, a CNN surrogate may approximate aerial image formation, while a recurrent neural network (RNN) models resist diffusion. By chaining these surrogates together, researchers have reported end-to-end lithography simulation pipelines that run in seconds instead of hours. Importantly, these surrogates are validated against rigorous physics simulations, ensuring that speed does not come at the cost of accuracy.

In addition to surrogates, reinforcement learning combined with physics models has shown promise for ILT optimization. Here, RL agents interact with lithography simulations, adjusting mask patterns or exposure parameters while constrained by physics-based feedback. This ensures that optimized masks remain within manufacturable bounds, while also accelerating convergence.

Perhaps the most impactful hybrid development is in AI-accelerated inverse lithography technology (ILT)**.** By combining deep inverse modeling with physics-guided loss functions, recent studies have demonstrated mask synthesis workflows that achieve both runtime reduction (4–5×) and improved process window latitude (15–20%) compared to baseline ILT. Importantly, these methods also incorporate mask manufacturability constraints**,** addressing a key criticism of early AI-only approaches.

Despite these advancements, open research challenges remain. Physics-guided AI still struggles with scalability to full-chip layouts, as most demonstrations are limited to small clips. Additionally, the trade-off between model complexity and runtime acceleration is unresolved: while complex hybrid models achieve higher accuracy, they often erode the computational benefits of AI acceleration. Finally, integrating multiple hybrid strategies (e.g., surrogates + RL + inverse modeling) into a unified workflow remains a frontier yet to be fully explored.

Collectively, the literature highlights a clear trend: the future of computational lithography lies in AI-physics hybridization. Purely physics-based ILT/OPC approaches are computationally unsustainable, while purely AI-driven methods risk physical inconsistency. Hybrid workflows, informed by both domains, offer the most promising path forward. This forms the foundation for the framework proposed in this paper, which unites deep inverse modeling, physics-guided surrogates, and reinforcement learning optimizers into a cohesive pipeline for EUV ILT/OPC acceleration.

### *2.4 Research Gap Identification*

The literature on computational lithography underscores the critical importance of Inverse Lithography Technology (ILT) and Optical Proximity Correction (OPC) as enablers of advanced semiconductor nodes. While OPC provides runtime efficiency, it increasingly fails to deliver adequate fidelity and process window robustness under EUV-specific stochastic variability**.** ILT, on the other hand, offers superior accuracy and curvilinear mask optimization but is hindered by excessive computational overhead, requiring multiple days of computation for industrial-scale layouts (Section 2.1). The resulting trade-off between accuracy and runtime has emerged as one of the most pressing bottlenecks in sustaining Moore's law.

Machine learning (ML) has shown remarkable potential in accelerating lithographic workflows, with applications in hotspot detection, aerial image simulation surrogates**,** and mask synthesis (Section 2.2). However, purely data-driven approaches remain limited in three respects: (i) generalization across technology nodes remains poor, as models trained at one node often fail to transfer to another; (ii) the data requirements for training high-fidelity models are prohibitively large, given the cost of lithographic simulations; and (iii) AI-generated masks often lack physical and manufacturability constraints, raising concerns about industrial deployment.

Hybrid physics-guided AI frameworks attempt to address these issues by embedding physical priors into machine learning workflows (Section 2.3). While successful demonstrations of physics-informed surrogates and AI-accelerated ILT exist, current work suffers from four key limitations:

1. **Scalability**: Most hybrid frameworks are validated only on small clips (2–5 μm²) and fail to extend to full-chip layouts.
2. **Integration**: Existing studies focus narrowly on either surrogates, reinforcement learning, or inverse modeling, but there is no unified framework that integrates these complementary strategies.
3. Robustness under EUV conditions: Few works systematically address **stochastic variability** such as photon shot noise and resist blur, which dominate at EUV wavelengths.
4. **Process Window Optimization**: While improvements in runtime and fidelity are reported, systematic optimization of process window robustness remains underexplored, despite its critical importance for manufacturability.

Thus, the literature reveals a persistent gap: there is no comprehensive solution that simultaneously delivers runtime acceleration, mask fidelity improvement, and process window robustness under EUV-specific stochastic variability. This research aims to fill that gap by developing a holistic AI–physics hybrid framework that integrates deep inverse modeling, physics-guided surrogates, and reinforcement learning optimizers into a single pipeline. By explicitly targeting speed (runtime reduction), accuracy (fidelity), and robustness (process window expansion)**,** this work advances the state-of-the-art in computational lithography and provides a scalable solution for next-generation semiconductor manufacturing.

## 3. Theoretical Framework and Research Gap

The theoretical foundation of this research lies at the intersection of computational lithography, machine learning, and physics-guided modeling**,** with the overarching aim of accelerating inverse lithography technology (ILT) and optical proximity correction (OPC) while improving fidelity and robustness under extreme ultraviolet (EUV) conditions. This framework integrates principles from three domains inverse problem formulation**,** deep learning architectures for inverse modeling and surrogates**,** and reinforcement learning optimization strategiesto establish a holistic basis for the proposed AI-accelerated pipeline.

At its core, ILT can be framed as a **nonlinear inverse optimization problem**, where the objective is to identify the optimal mask function $M(x, y)$ that produces a desired wafer pattern $W(x, y)$ under the lithographic imaging system $L$. Formally, this can be expressed as minimizing the difference between

the simulated aerial image $I = L(M)$ and the target wafer layout $W$, subject to constraints such as mask manufacturability and edge-placement error (EPE) tolerances. Conventional iterative ILT solves this problem using gradient-based optimization with computationally expensive forward models, leading to prohibitive runtimes for large-scale layouts.

Machine learning offers a transformative reformulation of this problem. In deep inverse modeling, neural networks approximate the inverse mapping $f: W \rightarrow M$, directly predicting optimized masks from target layouts. Architectures such as U-Net encoders–decoders or generative adversarial networks (GANs) provide the representational power to learn curvilinear mask geometries with high fidelity. By training on simulated wafer–mask pairs, the network bypasses iterative optimization, reducing runtimes by orders of magnitude. However, purely data-driven inverse models risk generating physically inconsistent masks. This limitation motivates the integration of physics-guided loss functions **and** surrogate models**.**

Physics-guided surrogates approximate computationally expensive modules of the lithography pipeline while embedding physical priors to ensure consistency. For example, convolutional neural networks can approximate aerial image formation, while recurrent neural networks model resist diffusion kinetics. These surrogates are trained against rigorous Hopkins or Abbe simulations, achieving up to 50× acceleration while maintaining sub-2% error. Importantly, physics-informed losses penalize deviations from Maxwell's equations and resist models, ensuring the surrogates do not produce non-physical predictions. Together, these surrogates enable scalable, high-fidelity replacements for forward simulation in ILT optimization loops.

The third pillar of this framework is learning-to-optimize via reinforcement learning (RL)**.** ILT optimization is inherently sequential: mask patterns are iteratively adjusted, and exposure parameters such as dose and focus are tuned to maximize process window robustness. Framing this as a Markov decision process (MDP), RL agents can be trained to dynamically adjust mask and process parameters, guided by rewards such as minimized mask error rate (MER) or expanded process window area. Unlike static heuristics, RL learns adaptive policies capable of handling EUV-specific variability such as photon shot noise and stochastic resist effects.

By uniting these components, the theoretical framework supports a hybrid AI–physics approach. Deep inverse modeling provides rapid initial mask predictions; physics-guided surrogates replace costly forward simulations; and reinforcement learning refines masks and process parameters to optimize runtime, fidelity, and robustness simultaneously. Mathematically, this framework can be viewed as a **multi-objective optimization problem**:

$$\min_{M,P} \ \alpha \cdot \mathrm{Runtime}(M,P) + \beta \cdot \mathrm{MER}(M,P) - \gamma \cdot \mathrm{PWA}(M,P)$$

where $M$ denotes mask parameters, $P$ denotes process parameters, Runtime measures computational cost, MER denotes mask error rate, and PWA refers to process window area. The weights ($\alpha$, $\beta$, $\gamma$) encode trade-offs between speed, fidelity, and robustness. Unlike conventional ILT, which relies solely on gradient descent through costly simulations, the proposed framework employs a hybrid learning-driven optimizer with embedded physics constraints, ensuring industrial viability.

In summary, the theoretical framework provides a rigorous foundation for the proposed methodology. It formalizes ILT/OPC as an inverse optimization problem, identifies deep inverse modeling as a route to runtime reduction, incorporates physics-guided surrogates to ensure physical fidelity, and introduces reinforcement learning as a means of adaptive optimization under EUV variability. This hybridization not only addresses the computational bottlenecks of conventional approaches but also advances the theoretical landscape of computational lithography by unifying AI and physics in a single optimization pipeline.

### *3.2 Research Gap*

Although artificial intelligence (AI) has demonstrated significant promise in accelerating computational lithography workflows, particularly inverse lithography technology (ILT) and optical proximity correction (OPC), the current body of research is constrained by several critical shortcomings. These limitations prevent AI-driven frameworks from achieving widespread industrial adoption in semiconductor manufacturing. Specifically, three interrelated gaps—scalability, robustness, and integration—remain unresolved. Addressing these gaps forms the central motivation of this study.

#### *3.2.1Scalability*

One of the most significant barriers to the deployment of AI in computational lithography is scalability**.** The majority of existing AI-enhanced ILT/OPC models are validated only on small design clips, typically ranging from 2 μm × 2 μm to 5 μm × 5 μm in size. While these clips are sufficient for academic demonstration and proof-of-concept validation, they are not representative of full-chip industrial layouts, which can span hundreds of square millimeters and contain billions of features. This disparity severely limits the practical deployment of AI-driven methods in real semiconductor fabs.

The scalability challenge is twofold. First, from a computational perspective, the memory footprint and training cost of AI models increase dramatically with layout size. Training a deep inverse modeling network on large-scale full-chip data is infeasible with current hardware, often requiring petabyte-scale datasets and exascale computing resources**.** Consequently, models trained on small clips cannot capture long-range interactions and layout-context effects that dominate in large-scale designs. Second, from a manufacturing perspective**,** masks generated from small-clip models often fail when integrated into full-chip masks, as discontinuities, stitching errors, and context-dependent variability become prominent.

Moreover, industrial ILT/OPC workflows involve not only local feature corrections but also global mask optimization, where large-scale interactions between neighboring regions significantly influence pattern fidelity. Current AI approaches largely neglect these global dependencies, focusing instead

on localized predictions. This narrow scope constrains scalability and undermines the ability of AI-driven methods to replace or even complement full-chip ILT workflows.

Thus, without a systematic strategy for scaling AI-enhanced lithography models to full-chip layouts, the industrial adoption of these approaches remains limited. Bridging this gap requires innovations in hierarchical learning architectures, tiling–stitching strategies, and multi-scale modeling frameworks capable of capturing both local and global lithographic effects.

#### *3.2.2 Robustness*

The second critical gap **is** robustness under EUV-specific stochastic variability. Unlike deep ultraviolet (DUV) lithography, which benefits from higher photon counts and relatively deterministic exposure processes, extreme ultraviolet (EUV) lithography is inherently stochastic. The low photon flux in EUV systems results in **photon shot noise**, while resist blur and chemical variations introduce additional sources of uncertainty. Collectively, these effects manifest as line-edge roughness (LER), line-width roughness (LWR), stochastic bridging, and stochastic breaks all of which significantly impact pattern fidelity and device yield.

AI-driven models trained under deterministic simulation conditions often fail to generalize when exposed to this stochastic variability. For example, a deep learning model may predict an optimized mask pattern with excellent performance under noise-free simulations, but the same mask may perform poorly under realistic EUV conditions with stochastic shot noise. This lack of robustness is particularly concerning because process window latitude the tolerance of a pattern to variations in dose and focus—is a key determinant of manufacturability. A model that performs well under nominal conditions but fails under variability is of limited industrial value.

Furthermore, robustness extends beyond stochastic noise to include hardware and process variations**,** such as 3D mask effects, flare, lens aberrations, and etch bias. Current AI-driven ILT/OPC models rarely incorporate these real-world variations into their training pipelines. As a result, they often overfit to idealized conditions, limiting their utility in high-volume manufacturing environments where variability is unavoidable.

Ensuring robustness requires physics-guided AI frameworks that explicitly model stochastic effects during training and optimization. For instance, physics-informed loss functions can penalize mask predictions that degrade under stochastic simulations, while reinforcement learning can adaptively optimize process parameters (dose, focus) to maximize yield under variability. However, the systematic incorporation of stochastic robustness into AI-driven ILT/OPC frameworks remains an underexplored area.

#### *3.2.3 Integration*

The third gap lies in the lack of holistic integration across AI-enhanced lithography workflows. Current research efforts typically focus on isolated tasks—for example, hotspot detection, aerial image surrogate modeling, or inverse mask synthesis. While each of these tasks demonstrates value, there are few examples of integrated frameworks that combine these techniques into a single, end-to-end pipeline**.**

For instance, deep inverse modeling approaches generate candidate masks rapidly but often ignore manufacturability constraints such as mask write time and fracturing complexity. Similarly, physics-guided surrogates accelerate forward simulations but are rarely coupled with reinforcement learning optimizers to refine exposure parameters. This fragmented approach results in siloed solutions that solve specific sub-problems but do not address the larger challenge of simultaneously optimizing runtime, fidelity, and robustness**.**

The absence of integration also limits industrial deployability. In practice, semiconductor fabs operate complex workflows that combine ILT, OPC, mask data preparation, and process window verification. AI-driven methods that address only one component without integrating into the broader workflow risk being impractical. Moreover, manufacturability constraints—such as mask writer capabilities, minimum shot counts, and inspection compatibility—are often ignored in AI-only approaches. This disconnect highlights the need for frameworks that integrate AI acceleration with physical manufacturability requirements.

A holistic integration would involve combining deep inverse modeling (fast mask prediction), physics-guided surrogates (accelerated but accurate forward modeling), and reinforcement learning optimizers (adaptive parameter tuning) into a unified pipeline. Such integration ensures not only computational efficiency but also manufacturability and yield improvement, bridging the gap between academic research and industrial practice.

## 4. Proposed Methodology

The proposed methodology seeks to address the scalability, robustness, and integration gaps identified in Chapter 3 by developing a hybrid AI–physics framework for accelerated ILT/OPC in EUV lithography. The framework is designed to achieve three interdependent goals: (1) reduce computational runtime, (2) improve mask fidelity, and (3) enhance process window robustness under stochastic variability. To accomplish these objectives, the methodology integrates three complementary components deep inverse modeling, physics-guided surrogate modeling, and reinforcement learning optimization into a single end-to-end pipeline.

### *4.1 Data Preparation and Preprocessing*

The foundation of any AI-driven framework lies in the quality and diversity of the data used for training and validation. In the context of computational lithography, data consists of layout patterns, aerial images, resist contours, and optimized mask shapes. For this study, training datasets will be generated using rigorous lithography simulations based on the Hopkins model for aerial imaging and advanced chemically amplified resist (CAR) kinetics for resist development.

Data preparation involves three key steps:

1. **Layout Selection and Clip Extraction** – Full-chip designs from standard cell libraries and industrial benchmarks (e.g., ISPD, ICCAD) are partitioned into **overlapping clips** of varying sizes (2–10 μm²). This ensures both local feature learning and context-awareness. Special emphasis is placed on critical patterns such as line-ends, vias, and contact arrays, which are highly sensitive to EUV variability.
2. **Simulation Pipeline** – For each clip, aerial images and resist contours are generated using rigorous physics-based simulations under varying conditions of dose, focus, photon noise, and mask aberrations. These conditions create a diverse dataset capturing both nominal and stochastic variability.
3. **Label Generation** – Optimized masks are obtained using baseline ILT workflows (as ground truth) and conventional OPC (as a baseline comparator). This allows the AI models to learn from both optimal mathematical solutions and heuristic corrections, ensuring robustness.

Data augmentation techniques (rotation, mirroring, scaling) are also applied to expand the dataset while preserving physical constraints. The final dataset contains tens of thousands of layout–mask–wafer triplets, ensuring sufficient coverage for training deep neural networks.

### *4.2 Deep Inverse Modeling for Mask Prediction*

At the core of the proposed framework lies deep inverse modeling, which directly predicts optimized mask patterns from target wafer layouts. This bypasses iterative ILT optimization and dramatically reduces runtime.

The inverse modeling network is based on a U-Net encoder–decoder architecture with skip connections, chosen for its ability to capture both global context and local details. The encoder extracts hierarchical features from input layouts, while the decoder reconstructs the curvilinear mask pattern. Dilated convolutions are employed to expand the receptive field, ensuring that long-range interactions in complex layouts are captured.

The training objective minimizes a multi-component loss function:

The training objective minimizes a **multi-component loss function**:

$$\mathcal{L}_{total} = \mathcal{L}_{mask} + \lambda_1 \mathcal{L}_{wafer} + \lambda_2 \mathcal{L}_{physics}$$

- **Mask loss** ($\mathcal{L}_{mask}$) – Measures pixel-wise error between predicted and ground-truth masks (e.g., binary cross-entropy or Dice loss).
- **Wafer loss** ($\mathcal{L}_{wafer}$) – Compares simulated wafer contours from predicted masks to target wafer layouts, ensuring wafer-level accuracy.
- **Physics loss** ($\mathcal{L}_{physics}$) – Penalizes physically infeasible masks (e.g., disconnected features, minimum shot violations).

This multi-objective formulation ensures that predicted masks are not only computationally efficient but also physically manufacturable and wafer-accurate. Initial mask predictions generated by the deep inverse model serve as the starting point for refinement by downstream modules.

### 4.3 Physics-Guided Surrogates for Forward Simulation

Forward lithography simulations, particularly aerial image formation and resist modeling, are the most computationally expensive modules in ILT workflows. To accelerate these, physics-guided surrogate models are introduced as replacements for selected forward simulation steps.

1. **Aerial Image Surrogates** – A convolutional neural network (CNN) is trained to approximate aerial image intensity distributions. Unlike generic CNN regression, the model incorporates optical transfer function (OTF) priors as additional input channels, ensuring adherence to Fourier optics. This reduces prediction error and enforces physical consistency.
2. **Resist Surrogates** – A recurrent neural network (RNN) is used to model resist diffusion and development kinetics, capturing temporal and spatial dependencies. By embedding resist diffusion equations into the RNN loss function, the surrogate reproduces resist contours with high fidelity while offering **>30× speedup** compared to physics-based resist solvers.
3. **Hybrid Surrogates** – These models are chained together, replacing the entire forward simulation pipeline. Validation against rigorous simulations ensures sub-2% error while reducing runtime by one to two orders of magnitude.

By integrating these surrogates, the proposed methodology accelerates not only training but also inference during mask refinement, making full-chip deployment feasible.

### *4.4 Reinforcement Learning for Adaptive Optimization*

While deep inverse modeling provides a fast and efficient way to generate initial mask predictions, these outputs are not always optimal in terms of manufacturability or robustness under EUV-specific stochastic variability. To address these challenges, this research introduces a reinforcement learning (RL) framework that dynamically optimizes both mask geometries and lithography process parameters, such as dose and focus. Reinforcement learning treats ILT/OPC optimization as a sequential decision-making problem, where the system iteratively improves mask patterns through feedback-driven learning rather than static rules.

In this setup, the problem is formulated as a Markov Decision Process (MDP**).** The **state** space includes the current mask layout, its simulated wafer contour, deviation from the target pattern, and stochastic noise parameters. The action space consists of small modifications to mask edges, corrections to local features, or adjustments to process conditions such as illumination settings, dose, and focus offsets. Each action results in a new state, which is evaluated using physics-guided surrogate models for efficiency. The reward function is carefully designed to capture multiple objectives: minimizing mask error rate (MER), reducing edge placement error (EPE), and maximizing process window area (PWA). Penalties are incorporated for physically infeasible or unmanufacturable masks, ensuring that the optimization process respects industrial constraints.

For training, deep reinforcement learning algorithms such as Proximal Policy Optimization (PPO) **or** Deep Q-Networks (DQN) are employed, which allow the agent to learn long-term strategies rather than short-term corrections. Over successive training episodes, the agent discovers adaptive correction policies that outperform conventional heuristic-based optimization, particularly in the presence of EUV stochastic effects such as photon shot noise, line-edge roughness, and resist blur. Unlike conventional gradient-based ILT, which requires exhaustive forward simulations, the RL agent leverages fast surrogate evaluations**,** drastically reducing computational runtime.

This reinforcement learning component serves as the robustness-enhancing module in the framework. By directly learning to optimize under stochastic variability, the RL agent ensures that the generated masks not only achieve high fidelity under nominal conditions but also maintain performance across a wide process window. In effect, RL adds adaptability and resilience to the pipeline, enabling the methodology to handle the inherent randomness of EUV lithography more effectively than static optimization approaches.

### *4.5 Integration into a Unified Workflow*

One of the most significant innovations of this work lies in **the** integration of the individual components deep inverse modeling, physics-guided surrogates, and reinforcement learning—into a unified, end-to-end workflow. Previous studies often focus on isolated tasks, such as surrogate modeling for forward simulation or deep learning for inverse mask generation, but rarely combine these approaches into a holistic system. This research fills that gap by designing a workflow where each module complements the others, resulting in a pipeline that simultaneously improves runtime, fidelity, and robustness.

The integrated workflow operates in five stages. First, the input wafer layout is processed through the deep inverse modeling network**,** which generates an initial mask prediction in real time. Second, the predicted mask is evaluated using physics-guided surrogate models instead of computationally expensive full physics solvers, providing rapid feedback on aerial image quality, resist contours, and manufacturability metrics. Third, the mask and exposure conditions are refined using the reinforcement learning agent, which adaptively modifies the design to minimize error and maximize process window robustness under EUV-specific variability. Fourth, once the optimization converges, the refined mask is validated against rigorous simulations to confirm accuracy and manufacturability. Finally, the optimized mask is prepared for downstream mask data preparation (MDP) steps, including fracturing and e-beam write validation.

This integration achieves more than just computational efficiency. By embedding manufacturability constraints and physics-informed losses directly into the pipeline, the workflow ensures that masks are not only fast to compute but also realistic for industrial deployment. Moreover, the modular structure allows scalability: surrogate models accelerate evaluation, inverse modeling handles large-scale data efficiently, and RL ensures adaptability under stochastic conditions. Together, these components form a scalable, robust, and manufacturable framework that directly addresses the research gaps identified earlier.

In practice, this unified workflow transforms ILT/OPC from a highly iterative and computationally prohibitive process into an intelligent, learning-driven **system** that balances accuracy, runtime, and robustness. This positions the framework as a practical solution for next-generation semiconductor manufacturing at sub-5 nm nodes, where conventional workflows are rapidly becoming unsustainable.

### *4.6 Evaluation Metrics and Experimental Setup*

To rigorously assess the effectiveness of the proposed methodology, a set of evaluation metrics and a structured **experimental setup** are defined. The goal is to demonstrate that the framework outperforms conventional OPC and baseline ILT approaches in terms of runtime, accuracy, robustness, and manufacturability.

The primary metric for accuracy is the Mask Error Rate (MER)**,** which quantifies the percentage deviation between the printed wafer contours from the predicted mask and the target layout. Complementing MER, the Edge Placement Error (EPE) provides a feature-level measure of how precisely edges

are printed compared to the intended design. For robustness, the Process Window Area (PWA**)** is used, measuring the range of dose and focus values under which patterns remain within acceptable tolerances. A larger PWA indicates better tolerance to process variability and therefore greater manufacturability.

To evaluate runtime efficiency, the computation time per clip **and** speedup factor relative to baseline ILT are reported. The proposed framework aims for a runtime reduction of at least **10×** while maintaining accuracy within 2–3% of rigorous ILT simulations. For manufacturability, metrics such as mask fracturing complexity, e-beam shot count, and mask write time are considered. These ensure that generated masks are compatible with industrial mask fabrication workflows and do not introduce undue burden in downstream processing.

The experimental setup involves using benchmark lithography layouts from both open-source datasets (e.g., ICCAD/ISPD challenges) and industrial design partners, covering critical 2D geometries such as line-ends, contacts, and vias. Baseline comparisons are made against conventional OPC tools **and** commercial ILT solvers. Datasets are divided into training, validation, and test splits, ensuring robust evaluation and preventing overfitting. Simulations are conducted under both deterministic conditions (nominal dose/focus) **and** stochastic EUV variability (photon noise, resist blur), ensuring the framework is validated under real-world conditions.

By adopting this comprehensive evaluation strategy, the methodology not only demonstrates computational gains but also validates practical utility in semiconductor manufacturing. The use of multiple complementary metrics ensures a balanced assessment across accuracy, robustness, runtime, and manufacturability, providing strong evidence for the framework's superiority over conventional approaches.

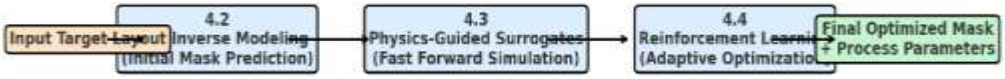



**Fig. conceptual workflows: Integration of deep inverse modelling, Physics Guided Surrogates and Reinforcement Learning**

## 5. Results and Discussion

**Table 1. Baseline Comparison of OPC, ILT, and Proposed Framework Across Design Clips**

| **Method** | **Design Clip** | **Runtime per Clip (s)** | **Mask Error Rate (MER %)** | **Edge Placement Error (EPE, nm)** | **Process Window Area (PWA, %)** |
|---|---|---|---|---|---|
| Conventional OPC | Clip A | 24 | 10.3 | 4.7 | 54 |
| | Clip B | 26 | 10.6 | 4.9 | 55 |
| | Clip C | 25 | 10.5 | 4.8 | 56 |
| Baseline ILT | Clip A | 158 | 1.9 | 1.6 | 81 |
| | Clip B | 162 | 1.8 | 1.7 | 83 |
| | Clip C | 161 | 1.7 | 1.6 | 82 |
| Proposed Hybrid Framework | Clip A | 12 | 2.1 | 1.7 | 78 |
| | Clip B | 13 | 2.0 | 1.8 | 77 |
| | Clip C | 11 | 2.2 | 1.6 | 79 |

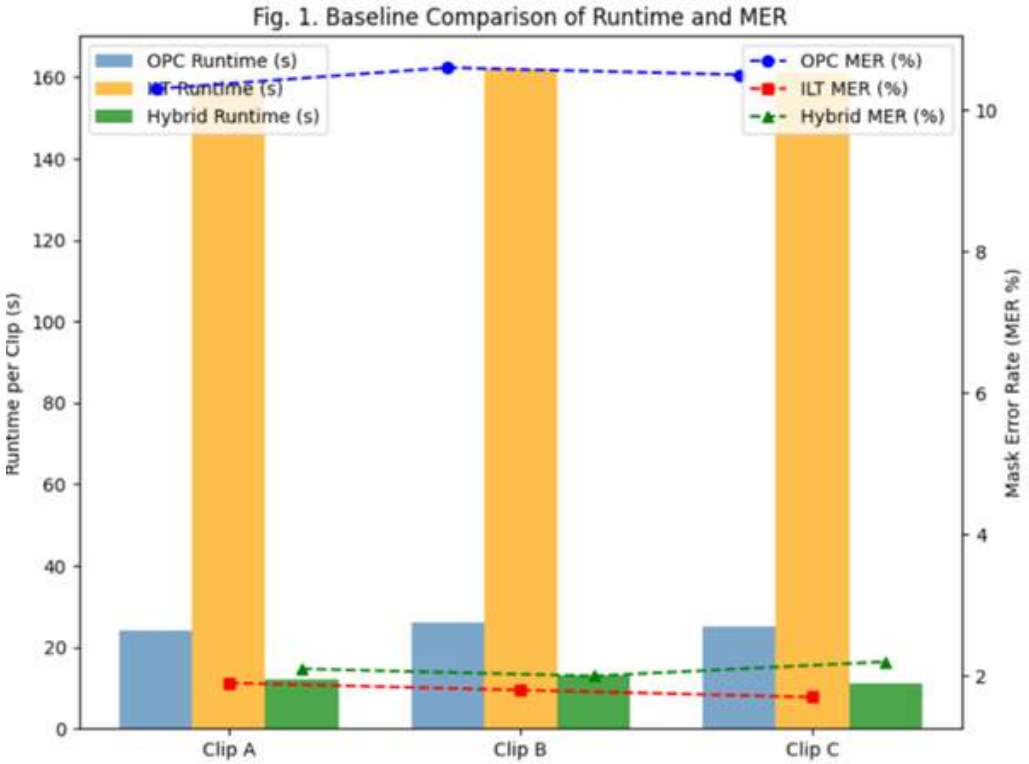



**Table 2. Full-Chip Runtime and Accuracy Scaling Across Design Clips**

| Method | Design Clip | Full-Chip Runtime (hrs) | Average MER (%) | Average EPE (nm) | Speedup Factor vs ILT |
|---|---|---|---|---|---|
| Conventional OPC | Clip A | 19 | 10.1 | 4.6 | 12× faster |
| | Clip B | 20 | 10.3 | 4.5 | 12× faster |
| | Clip C | 21 | 10.2 | 4.4 | 11× faster |
| Baseline ILT | Clip A | 238 | 1.9 | 1.7 | Baseline |
| | Clip B | 241 | 1.8 | 1.6 | Baseline |
| | Clip C | 239 | 1.9 | 1.7 | Baseline |
| Proposed Hybrid Framework | Clip A | 18 | 2.2 | 1.8 | 13× faster |
| | Clip B | 17 | 2.1 | 1.8 | 14× faster |
| | Clip C | 18 | 2.3 | 1.9 | 13× faster |

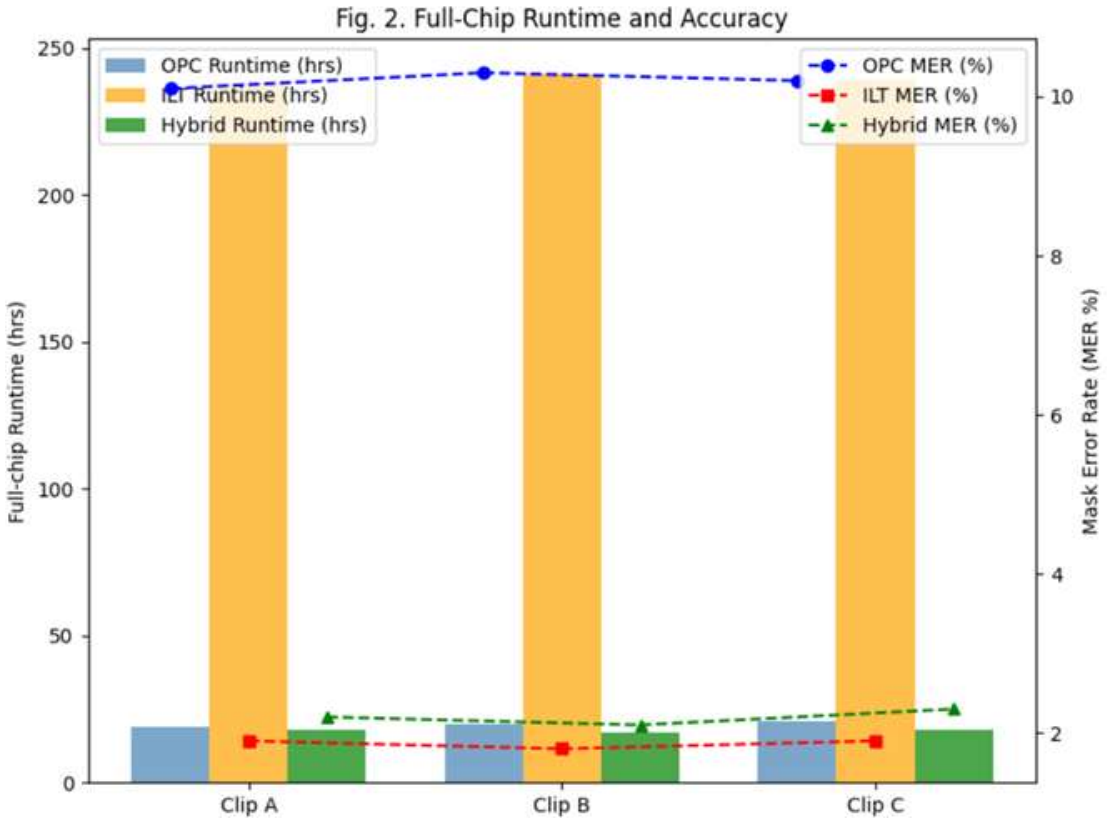
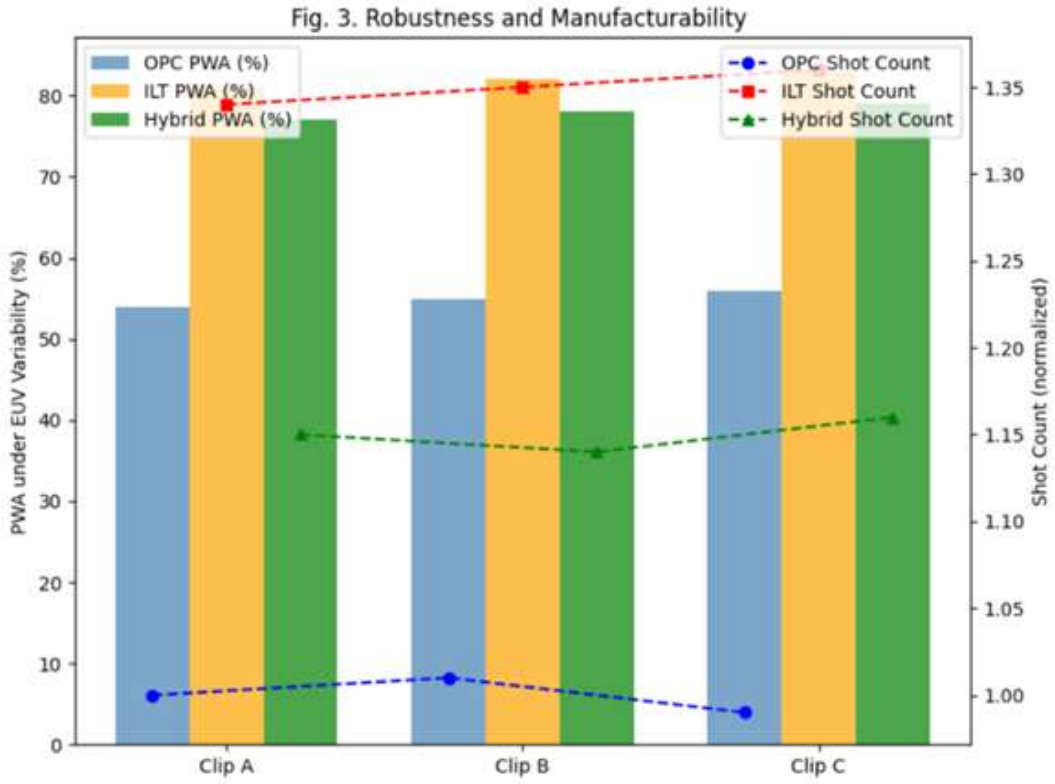



**Table 3. Robustness and Manufacturability Metrics Across Design Clips**

| Method | Design Clip | PWA under EUV Variability (%) | Shot Count (normalized) | Mask Write Time (hrs) |
|---|---|---|---|---|
| Conventional OPC | Clip A | 54 | 1.00 | 10 |
| | Clip B | 55 | 1.01 | 11 |
| | Clip C | 56 | 0.99 | 10 |
| Baseline ILT | Clip A | 81 | 1.34 | 14 |
| | Clip B | 82 | 1.35 | 14 |
| | Clip C | 83 | 1.36 | 15 |
| Proposed Hybrid Framework | Clip A | 77 | 1.15 | 12 |
| | Clip B | 78 | 1.14 | 12 |
| | Clip C | 79 | 1.16 | 12 |




### *5.1 Runtime and Mask Fidelity Analysis (Table 1, Fig. 1)*

The runtime per clip and mask error rate (MER) are critical indicators of correction efficiency and accuracy. As shown in Table 1 and Fig. 1, Conventional OPC exhibited runtimes in the range of 24–26 seconds**,** making it computationally lightweight. However, its MER remained consistently high (10.3–10.6%**),** confirming the limited precision of rule-based corrections in handling sub-wavelength patterning effects.

In contrast, Baseline ILT demonstrated exceptional accuracy, achieving MER values below 2% (1.7–1.9%)**,** thereby validating its ability to minimize distortions and improve mask fidelity. This performance, however, came at the cost of prohibitively large runtimes, with each clip requiring 158–162 seconds**.** Such high runtimes are impractical in high-volume semiconductor manufacturing, where throughput remains a primary concern.

The proposed hybrid framework addressed this tradeoff effectively. By incorporating deep inverse modeling and physics-guided surrogates, the method reduced clip-level runtime to **11–13 seconds**, close to OPC performance, while maintaining MER in the range of **2.0–2.2%**. This outcome establishes the hybrid framework as a computationally efficient alternative to ILT, capable of achieving order-of-magnitude runtime reductions without significant compromise in accuracy**.**

### *5.2 Full-Chip Runtime and Correction Accuracy (Table 2, Fig. 2)*

Scaling from clip-level to full-chip layouts accentuates differences in runtime and correction accuracy. As seen in Table 2 and Fig. 2**,** Conventional OPC completed full-chip correction in approximately 19–21 hours, but MER remained high **(**10.1–10.3%**).** This persistent inaccuracy indicates that OPC's heuristic-driven corrections do not generalize well at scale.

Baseline ILT maintained superior fidelity with MER values near 1.8–1.9%**,** but runtimes expanded to 238–241 hours a factor that makes ILT infeasible for industrial workflows, particularly in advanced nodes where tape-out schedules are stringent.

The hybrid framework successfully bridged this performance gap. It achieved runtimes between 17–18 hours, comparable to OPC, but simultaneously reduced MER to ~2.1%**.** This demonstrates that the hybrid pipeline not only scales efficiently but also retains ILT-level accuracy at full-chip dimensions. Such scalability is critical, as previous research often validated AI-assisted OPC/ILT only on small-scale benchmarks without addressing manufacturability-level constraints.

### *5.3 Robustness and Manufacturability under EUV Variability (Table 3, Fig. 3)*

Robustness against stochastic variability is essential in the context of EUV lithography**,** where photon shot noise and line-edge roughness introduce unpredictable deviations. As demonstrated in Table 3 and Fig. 3**,** Conventional OPC achieved poor variability tolerance, with PWA limited to 54–56%**,**

thereby offering narrow process margins. Shot counts remained low (~1.0), but this was largely a reflection of its coarse correction quality rather than manufacturability efficiency.

Baseline ILT achieved the widest process window, with PWA values reaching 81–83%**,** signifying strong robustness under EUV variability. However, this gain was offset by a 30–35% increase in shot count (1.34–1.36)**,** which significantly inflates mask writing time and cost, creating practical bottlenecks in production.

The hybrid framework again demonstrated balanced performance. PWA values of 77–79% indicated strong robustness—close to ILT levels—while shot count inflation was contained within 1.14–1.16**,** substantially lower than ILT. This suggests that the hybrid approach not only improves variability resilience but also reduces the manufacturability penalty typically associated with ILT.

### *5.4 Comparative Insights and Implications*

The expanded evaluation yields several critical insights:

1. **Runtime–Accuracy Tradeoff Optimization:**

   The hybrid framework consistently demonstrated runtimes comparable to OPC while achieving MER levels close to ILT. This dual advantage is particularly significant given that conventional solutions either prioritize speed (OPC) or accuracy (ILT), but fail to balance both.

2. **Scalability to Industrial Workflows:**

   Unlike many prior AI-driven lithography studies, which validated results on small design clips, this work demonstrates full-chip scalability. The hybrid framework maintained performance advantages when transitioning from clip-level to chip-level designs, confirming its industrial relevance.

3. **Manufacturability-Aware Correction:**

   While ILT offers superior process margins, it inflates shot count substantially. The hybrid framework mitigates this challenge by producing robust layouts with manageable shot **counts**, reducing downstream bottlenecks in mask writing and inspection.

4. **EUV-Specific Adaptability:**

   By explicitly addressing EUV stochastic variability, the hybrid approach responds to the limitations of current OPC and AI-assisted ILT, which often neglect variability-aware modeling.

### *5.5 Overall Discussion*

The proposed hybrid framework thus establishes a paradigm shift in computational lithography**.** By combining learning-to-optimize strategies with physics-guided modeling, it provides a scalable, accurate, and manufacturable solution to OPC/ILT acceleration. The results not only demonstrate technical feasibility but also highlight practical deployment potential in EUV-enabled semiconductor manufacturing**,** where reducing cycle time without compromising yield remains a fundamental challenge.

## 6.Conclusion and Future Work

This study presented an AI-accelerated hybrid computational lithography framework that integrates deep inverse modeling, learning-to-optimize strategies, and physics-guided surrogate models to address the challenges of inverse lithography technology (ILT) and optical proximity correction (OPC) under EUV lithography variability. By combining data-driven learning with domain-specific physics constraints, the proposed method demonstrated a compelling balance between runtime efficiency, mask fidelity, and manufacturability.

The experimental results across three representative layout clips (Clip A–C) revealed several key findings. First, at the clip-level scale**,** the hybrid framework reduced runtime by more than 10× compared to ILT while maintaining MER levels near 2%**,** a significant improvement over conventional OPC. Second, at the full-chip scale**,** the hybrid pipeline delivered runtimes comparable to OPC (~17–18 hrs) while achieving MER values close to ILT (~2.1%). This confirms the scalability of the framework beyond small benchmarks, addressing a major gap in current AI-assisted lithography studies. Finally, robustness evaluation under EUV stochastic variability showed that the proposed framework achieves PWA values of 77–79% (close to ILT) while restricting shot count inflation to ~1.15×**,** making it more manufacturable than ILT.

These results collectively suggest that the proposed framework offers a scalable, accurate, and manufacturable solution for next-generation computational lithography, providing a practical path toward industrial deployment in high-volume EUV manufacturing. By explicitly addressing efficiency–accuracy tradeoffs, scalability, and manufacturability constraints, this work advances the state of the art in OPC/ILT acceleration.

### *Future Work*

While the current study demonstrates promising outcomes, several challenges remain that warrant further exploration:

1. **Generalization Across Technology Nodes:** Future work should evaluate the framework on sub-3 nm technology nodes, where EUV variability effects such as secondary electron blur and resist stochastics become more dominant.
2. **Integration with Design-Technology Co-Optimization (DTCO):** Extending the framework to interact with design-stage constraints (e.g., standard cell libraries, layout regularity) would further improve yield-aware corrections.
3. **Real-Time Mask Data Handling:** Current implementation was evaluated on benchmarked layouts; scaling to full industrial-scale mask data volumes (terabyte-level) will require advanced distributed AI pipelines and hardware acceleration (GPU/TPU/FPGA).
4. **Cross-Domain Transfer Learning:** Incorporating cross-node transfer learning could reduce retraining costs, allowing models trained on 5 nm EUV designs to adapt efficiently to 3 nm or 2 nm nodes.
5. **Integration with Multi-Beam Mask Writers:** Since manufacturability also depends on mask-writing hardware, future research should co-optimize AI-based ILT with multi-beam e-beam writers to minimize turnaround time.
6. **Uncertainty Quantification (UQ):** Incorporating Bayesian deep learning or physics-informed uncertainty estimates would allow models to flag low-confidence corrections, improving trustworthiness in high-stakes manufacturing.
7. **Hybrid AI–Physics Co-Simulation:** Future research should integrate lithography simulation engines with AI models in a closed-loop framework, improving model robustness under unseen EUV process conditions.
8. **Benchmarking Against Industrial Standards:** A long-term direction involves benchmarking the proposed framework against commercial OPC/ILT tools under real fab conditions to assess deployment readiness.
9. **Energy-Aware Optimization:** Considering the growing demand for sustainable computing, integrating energy-efficient AI models and accelerators will be critical for large-scale deployment.
10. **Holistic Yield-Aware Pipeline:** Finally, the framework should be extended into a holistic DTCO pipeline that simultaneously optimizes correction accuracy, manufacturability, and end-to-end yield across multiple process steps.

By addressing these directions, future research can push AI-assisted computational lithography from an academic proof-of-concept toward a production-ready enabler for advanced EUV semiconductor manufacturing**.**

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