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Performance of Benchmarking of the Embedded SRAM and DRAM for Cryo-CMOS Applications in 40-nmTechnology

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Abstract:

Cryogenic CMOS (cryo-CMOS) embedded digital memories with diverse specifications are essential for interfacing electronics in quantum processors. To determine the most suitable architecture for each use case, this study benchmarks custom SRAM and DRAM designs across temperatures ranging from room temperature (RT) down to 4.2 K, all fabricated using a 40-nm CMOS process. Due to the notable shifts in device behavior at cryogenic temperatures—such as elevated threshold voltages, decreased sub threshold leakage, and greater variability—the viability of various memory types is evaluated, and key design considerations for cryogenic operation are proposed. Remarkably, at 4.2 K, a 2T low-threshold-voltage (LVT) DRAM demonstrates up to twice the power efficiency of SRAMs at access rates above 75 kHz. This efficiency gain is primarily due to a 40,000× increase in retention time, enabled by reduced leakage, which substantially lowers refresh power. These findings highlight the promising role of cryo-CMOS DRAMs in ultra-low-temperature applications.

Key Words: Cryogenic CMOS (cryo-CMOS), SRAM,DRAM, eDRAM, memory, quantum computing,.

I. INTRODUCTION

Quantum computers (QCs) are capable of achieving exponential acceleration for a variety of computational tasks [1]–[6]. However, scaling up quantum systems to support thousands or even millions of qubits presents significant hardware challenges—particularly the impracticality of routing an extensive number of wires from cryogenically cooled qubits to room-temperature (RT) control systems. To address this interconnect limitation, the use of cryogenic CMOS (cryo-CMOS)—CMOS-based electronics that operate reliably at cryogenic temperatures—has been proposed [7], [8].

Since the available cooling power in quantum computing systems is limited, designing cryo-CMOS circuits with ultra-low power consumption is of paramount importance. These control circuits typically include analog/RF interfaces for qubit manipulation and measurement, alongside a digital system-on-chip (SoC) responsible for quantum algorithm scheduling [9] and processing large volumes of measurement data, particularly for tasks such as quantum error correction [10]–[14].

In contemporary digital architectures, embedded memory consumes a substantial portion of both power and silicon area. Consequently, optimizing cryo-CMOS embedded memory becomes a key design objective. However, predicting memory power consumption under cryogenic conditions remains difficult due to the absence of robust cryogenic device models.

II. Cryo-CMOS Device Behavior

Lowering the temperature to cryogenic levels significantly impacts the behavior of short-channel NMOS and PMOS transistors. Specifically, it leads to an increase in threshold voltage (Vth) by approximately 100–200 mV, a subthreshold slope that becomes nearly three times steeper, and a doubling of the low-field carrier mobility. At cryogenic temperatures, device mismatch tends to increase, as observed in 40-nm and 28-nm bulk CMOS technologies [62], [63]. Additionally, interconnect resistance reduces by approximately 30% [64], and the capacitance of source/drain junctions decreases due to the expansion of depletion regions caused by carrier freeze-out effects [19]. These changes have beneficial implications for analog circuits, including improved bandwidth and lower power consumption. In digital circuits operating at full voltage swing, the enhanced carrier mobility at cryogenic temperatures offsets the impact of elevated threshold voltage (Vth). Combined with the reduced resistance and capacitance, this results in performance gains ranging from 10% to 20% in 40-nm bulk CMOS technologies [65]–[67]. However, in more advanced nodes, this performance improvement from room temperature (RT) to 4.2 K diminishes. This is primarily due to the greater relative impact of interconnect capacitance and lower supply voltages, which amplify the effect of increased Vth [65].

Nevertheless, FinFET technologies offer the potential to recover this performance loss by scaling Vth appropriately [40]. Moreover, the higher Vth and sharper subthreshold slope at cryogenic temperatures drastically reduce subthreshold leakage, while gate leakage remains nearly unchanged (within a factor of 2) [68]. For digital systems, this leads to significantly lower leakage power, while dynamic power consumption remains largely unaffected.

III. EXISTINGMETHOD

In the existing system technique with configurable multiple boost planes to implement low-power 6T SRAM. Experimental results reveal that the proposed 6T SRAM cell maintains stable operation across a temperature range from room temperature down to 6 K, achieving notably low minimum operating voltages—0.23 V at room temperature and 0.31 V at 6 K. While efforts have been made to optimize power consumption, recent research has increasingly shifted focus toward enhancing memory density. This study includes an analysis of the 6T SRAM cell across different CMOS technology nodes, specifically to evaluate its static noise margin (SNM).

To mitigate read disturbances, the read path is isolated from the actual storage nodes, and a write-assist mechanism is employed to perform write operations in a pseudo-differential manner using a dedicated write bit line and control signal [1]. The design and modeling of 6T SRAM cells for both 90nm and 180nm technologies were conducted using the Cadence Virtuoso platform. Static noise margins were extracted for SRAM cells built with nmos1V and nmos2V transistors in both technology nodes. As anticipated, SNM values decline with technology scaling, and results show that CMOS 1V transistors offer superior SNM performance compared to their CMOS 2V counterparts [1].

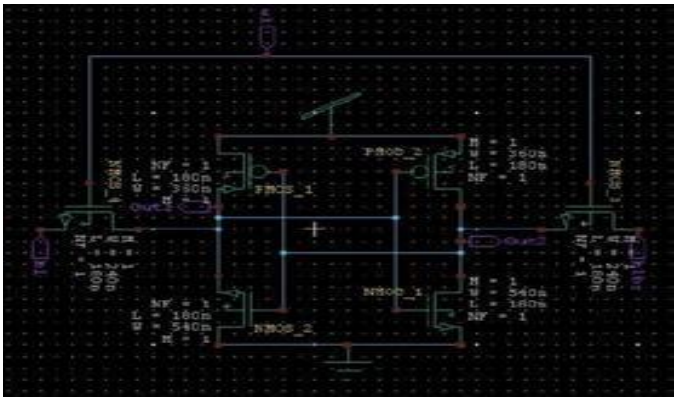


Figure: Existing System

IV. DESIGN METHODLOGY

In the proposed system Memory Circuits Volatile and non-volatile memories are two majorcategories of CMOS-basedmemory.Volatile memories, such as static random-access memory (SRAM) and dynamic RAM (DRAM), exhibit improved performance metrics at cryogenic temperatures due to reduced leakage currents and enhanced carrier mobility. Additionally, the high compatibility of volatile memory with silicon- based CMOS processes facilitates achieving high levels of integration. Due to its data stability and high-speed advantages, SRAM has become the most widely used memory topology. proposed a 4T SRAM structure optimized for operation at 77 K by eliminating two pMOS transistors from the pull-up network. The 4TSRAM achieved a reduction of cell area by20.3%, compared to the standard 6T SRAM structure. Moreover, it also provided faster read and write operations. Compared to SRAM, DRAM can achieve higher density due to its compact bitcell layout. However, DRAM requires frequent refresh operationstomaintain datacorrectness,resultingin extra area and power overhead. The additional costs associated with DRAM makeit less attractive for memory implementation at room temperature. Benefiting from the optimized leakage current and carrier mobility at cryogenic temperature, the data retention time and read/write operations of DRAM can be further improved. Recent research works have explored various DRAM topologies for cryogenic operations. Chakrabortyet al. [44]proposed a pseudo-static 1T capacitorless (1T0C) DRAM using 22 nm fully depleted silicon-on-insulator (FDSOI) technologyat 4.8 K, named Cryo-DRAM.

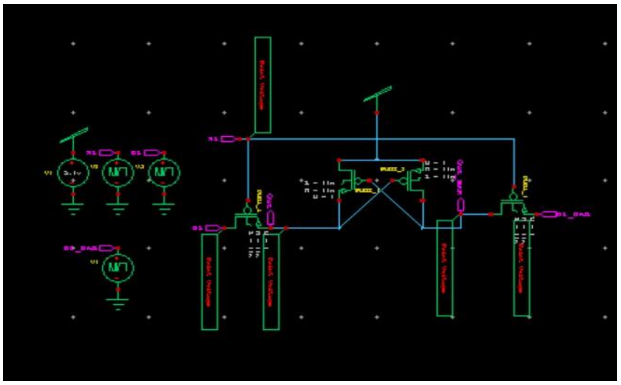


Figure: Proposed System

proposed a 4T CSDB-eDRAM design with dual- port read topologies and ensure disturb-free read operations. The 4T CSDB-eDRAM achieved an impressivedataretentiontimeof16.67sat4.2K,
with a maximum frequency of 1.41GHz. The studies above have demonstrated significant improvements in the performance of variousSRAM and DRAM cells at cryogenic temperatures a comprehensive benchmark from room temperature down to 4.2 K of custom memorycells, including 6T SRAM, 2T NWPR (nMOS for write and pMOS for read), 3T NWPR, and 3T NRPW(nMOSforreadandpMOSfor write)inthe same 40 nm CMOS process. Measurement results showed that the 2T low-threshold-voltage (LVT) DRAM operating at 4.2 Kis up to twice as energy- efficient as SRAM for access rates exceeding 75 kHz. These findings underscore the potential of cryogenic DRAMs for cryogenic applications.

V. SIMULATIONRESULTS

The entire simulation and result obtaining usingtest vectors are done with the help of Tanner 16.1 software.

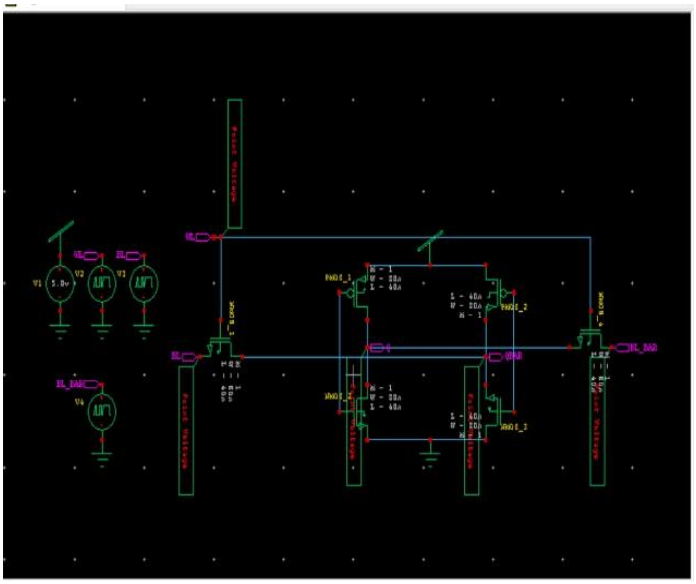
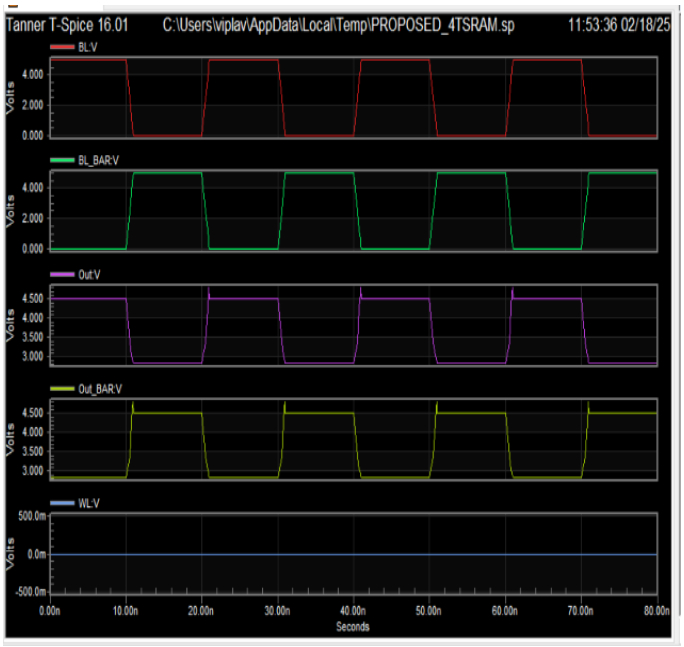


Figure: 6TSARM Existing System Diagram



Figure–8:6TSARM Existing System Simulation Outputs

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Power Results

VV2 from time 0 to 1e-008
Average power consumed -> 1.475947e+001 watts
Max power 1.475947e+001 at time 0
Min power 1.475947e+001 at time 0

VV3 from time 0 to 1e-008
Average power consumed -> 1.812614e-003 watts
Max power 1.812614e-003 at time 0
Min power 1.812614e-003 at time 0

VV4 from time 0 to 1e-008
Average power consumed -> 0.000000e+000 watts
Max power 0.000000e+000 at time 0
Min power 0.000000e+000 at time 0
```

Figure: 6TSRAM Existing System Power Results

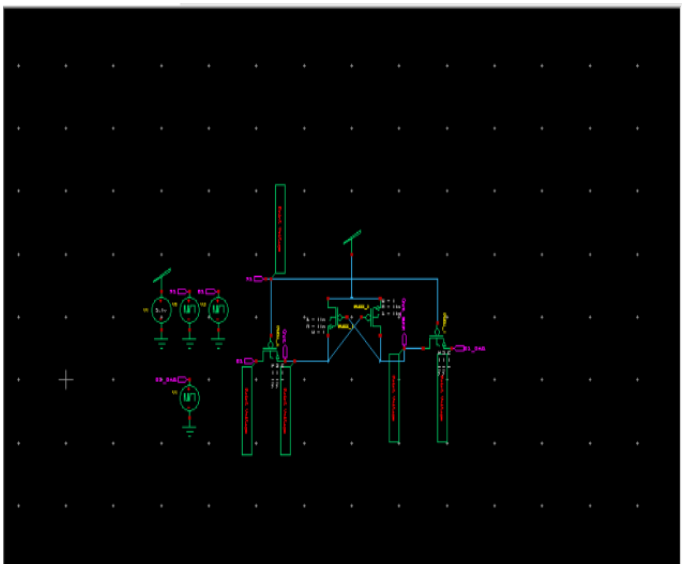

Figure: 4TSRAM Proposed system Circuit

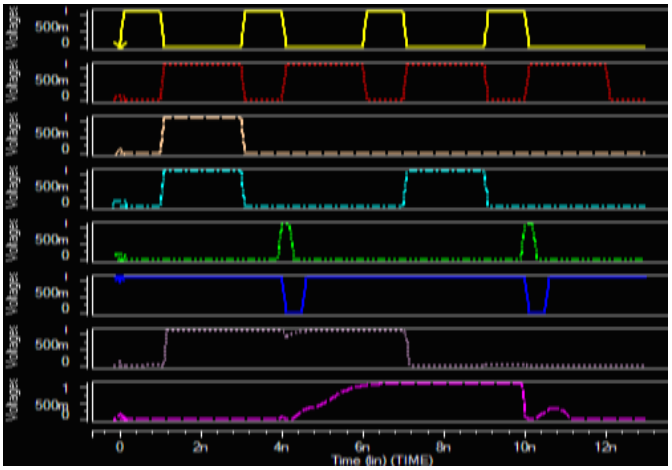

Figure: 4TSRAM Wave forms

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Min power 0.000000e+000 at time 0

VV3 from time 0 to 8e-008
Average power consumed -> 9.968859e-002 watts
Max power 2.094245e-001 at time 3e-008
Min power 0.000000e+000 at time 1.1e-008

VV4 from time 0 to 8e-008
Average power consumed -> 9.649796e-002 watts
Max power 2.094245e-001 at time 4e-008
Min power 0.000000e+000 at time 0


Parsing                    0.01 seconds
Setup                      0.01 seconds
DC operating point         0.05 seconds
Transient Analysis         0.04 seconds
Overhead                   0.64 seconds
```

Figure:4TSRAM Power Results

VI. CONCLUSION

Bycomparingsingle-bankstaticanddynamic memoriesatcryogenictemperature,thisarticle
shows that well-designed dynamic memories can outperform static memories for middle-to-high frequency applications in terms of area and power. While the subthreshold leakage reduces substantially from RT to 4.2 K, gate leakage stays approximately constant, thus still limiting the retention time. Still, adopting dynamic cells with enhanced resistance to gate leakage and cryogenic Vth shifts can significantly increase retention time, thus lowering the refresh power. The increased variability in both cells and peripherals may increase the number of outlier cells, while thelower noise reduces the read error rate. Embracing the design guidelines outlined here for cryogenic embedded memories will facilitate the adoption of dynamic-memory cells for high-density low-power cryogenic memories, there by enabling the complex cryo-CMOS SoCs needed in future QCs.

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