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Analog-to-Digital Conversion Using SAR in Verilog-A

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ABSTRACT:

Modern signal processing applications demand high-performance Analog-to-Digital Converters (ADCs) for reliable data conversion. This paper presents the design and simulation of a Successive Approximation Register (SAR) ADC, developed using Verilog-A with 90nm CMOS technology. The SAR ADC comprises core building blocks such as sample-and-hold, comparator, digital-to-analog converter (DAC) and SAR control logic. Emphasis is placed on minimizing power consumption while achieving high resolution and accuracy. Simulation outcomes validate the design's effectiveness, demonstrating its suitability for low-power and biomedical systems.

Keyword: *ADC; Biomedical; CMOS; low-power; SAR; Verilog-A*

1. INTRODUCTION

ADCs serve as vital components in converting analog inputs from the physical world into digital formats for electronic processing. They are ubiquitous in biomedical devices, communication systems and control applications. Among the array of ADC architectures, SAR ADCs are particularly attractive for low-power environments due to their simple structure and efficient performance [4][10].

This work focuses on the realization of a SAR ADC using Verilog-A, offering a behavioral-level simulation that accurately mirrors its analog functionality. The implementation targets biomedical applications, where power efficiency and precise signal conversion are crucial [2][8]. The proposed design uses 90nm CMOS technology modeled in Cadence Virtuoso, which enables precise analog behavior simulation and performance evaluation.

2. BACKGROUND AND RELATED WORK

Various researchers have proposed improvements in SAR ADC design. Gaikwad [5] proposed a compact 4-bit SAR ADC suitable for low-speed biomedical applications. Patel [6] explored a Flash ADC approach, offering speed advantages but increasing power demands. Harpe [4] provided detailed insights into techniques such as asynchronous SAR logic and capacitor segmentation for power and area efficiency.

Sajja and Rooban [3] focused on comparator design, introducing a regenerative comparator that significantly reduced power consumption during decision cycles. Ellaithy [2] presented an 8-bit SAR ADC capable of 1 MS/s using 130nm CMOS technology, which is well-suited for medium-speed applications in medical instruments.

Banik et al. [8] designed a 6-bit SAR ADC optimized for ultra-low power consumption in the biomedical domain. Kim et al. [9] addressed high-resolution SAR ADCs for wearable devices, combining low-voltage operation with reliable accuracy. Sotoudeh and Rezaei [10] proposed a switching scheme that drastically improved area and energy performance.

While these works have advanced SAR ADC technology, few comprehensively address biomedical integration with 8-bit resolution in Verilog-A, especially emphasizing simulation-based validation. Our work bridges this gap by simulating both sine and ECG signals, confirming biomedical feasibility. In addition, the proposed design emphasizes low power operation without compromising accuracy, making it highly suitable for wearable and implantable devices.

3. COMPARISION WITH OTHER WORKS

TABLE 1 COMPARATIVE ANALYSIS OF ADC ARCHITECTURES FROM RECENT LITERATURE

Author/Work	Architecture	Tech Node	Bit Depth	Key Feature	Advantage	Limitation
Vikas Tiwari et al. [1]	SAR	180nm	8-bit	Biomedical-focused SAR with low power	Tailored for medical applications	Higher technology node
D. M. Ellaithy [2]	SAR	130nm	8-bit	1 MS/s operation	Real-time suitability	Limited by legacy CMOS
Amrita Sajja & S. Rooban [3]	SAR	CMOS	8-bit	Regenerative comparator	Comparator energy efficiency	Integration complexity
Pieter Harpe [4]	SAR	Mixed	Various	Capacitor scaling, dynamic power	Flexible design approaches	Design optimization required
Suraj P. Gaikwad [5]	SAR	180nm	4-bit	Basic SAR Logic	Simple and low power	Low resolution
N. H. Patel [6]	Flash	180nm	4-bit	Parallel comparators	Very high speed	Excessive power usage
S. K. Sharma et al. [7]	Comparator	180nm	N/A	Leakage-controlled comparator	Power and speed balance	Not a full ADC
S. Banik et al. [8]	SAR	90nm	6-bit	Low-voltage, ultra-low power	Suitable for implantable devices	Limited resolution
L. Kim, M. Lee, N. Park [9]	SAR	CMOS	12-bit	High-resolution for wearable tech	Accurate and low-voltage	Complex architecture
M. Sotoudeh & F. Rezaei [10]	SAR	CMOS	10-bit	Four-level switching, 97% energy savings	Compact and power-saving	High design complexity
Proposed Work	SAR	90nm	8-bit	Verilog-A simulation; ECG evaluation	Biomedical alignment, robust modeling	Needs noise calibration

Several researchers have worked on refining ADC architectures to meet the demands of biomedical and low-power applications. Tiwari et al. [1] and Ellaithy [2] both focused on 8-bit SAR ADCs using older technology nodes, prioritizing low power and real-time performance. Sajja and Rooban [3] introduced a regenerative comparator for energy efficiency, while Harpe [4] explored optimization methods like capacitor scaling. Gaikwad's [5] basic 4-bit design offered simplicity and minimal power usage but lacked resolution, and Patel [6] proposed a Flash ADC that traded high speed for increased power consumption.

Other contributions include Sharma et al.'s [7] leakage-controlled comparator, Banik et al.'s [8] ultra-low power 6-bit SAR ADC for implantable and Kim et al.'s [9] 12-bit solution for wearable tech, combining accuracy with low voltage operation. Sotoudeh and Rezaei [10] enhanced efficiency through an innovative switching scheme. Building on these efforts, our proposed 8-bit SAR ADC—developed using Verilog-A and tested with sine and ECG signals on a 90nm node—offers a strong balance between biomedical compatibility and power efficiency, though further noise optimization is needed. Additionally, our design emphasizes a practical trade-off between resolution and power, aiming to meet the stringent demands of portable healthcare systems without adding significant design complexity.

4.PROPOSED WORK AND METHODOLOGY

This project focuses on designing a low-power SAR ADC tailored for biomedical signal processing applications. The goal is to develop a power-efficient yet high-accuracy converter through a structured design process that involves system-level planning, circuit implementation, simulation and optimization.

4.1 Methodology

The development of the SAR ADC follows a sequential approach as outlined below:

1. **System Architecture Design**

The initial step involves defining a clear and efficient system structure aimed at reducing overall power consumption. This includes identifying functional requirements, selecting essential components and employing a design strategy that prioritizes minimal energy usage without compromising performance.

2. **Power-Conscious Circuit Design**

   Each circuit block—Sample and Hold, Comparator, SAR Logic and DAC—is individually crafted using techniques that ensure low power operation. The design makes use of optimized architectures and component configurations specifically suited for low-voltage environments.

3. **Simulation Under Varied Conditions**

   Using circuit-level simulation tools, the SAR ADC is tested for its behavior under a range of input signals and conditions. These simulations help in understanding the dynamic response, energy profile and overall stability of the design.

4. **Performance-Assessment**

   The ADC's performance is measured against several critical parameters including resolution, accuracy, signal-to-noise ratio (SNR), power consumption and linearity. These benchmarks ensure the design satisfies the requirements typically expected in biomedical electronics.

5. **Validation and Optimization**

   After simulation, the design is thoroughly validated to pinpoint any areas needing improvement. Fine-tuning steps are then applied to further enhance efficiency, precision and robustness, ensuring the ADC meets all necessary specifications for real-world biomedical applications.

4.2 Key Components of the SAR ADC Design

- **Sample and Hold (S/H) Circuit:**

  Responsible for capturing the analog input and maintaining its value during conversion, this circuit helps avoid errors caused by rapid changes in the signal. It generally consists of an analog switch connected to a capacitor.

- **Comparator**

  This component evaluates the input signal by comparing it against a reference voltage. Its output is a binary decision that guides the SAR logic. Accurate comparison is vital for reliable digital output.

- **SAR-Logic:**

  The SAR (Successive Approximation Register) logic conducts a step-by-step binary search to determine the digital equivalent of the analog input. It works by controlling the DAC and interpreting comparator feedback to refine each bit of the output.

- **Digital-to-Analog Converter (DAC):**

  The DAC generates the reference voltage corresponding to each digital guess during the conversion process. Its resolution and accuracy directly influence the overall fidelity of the ADC.

4.3 Block Diagram

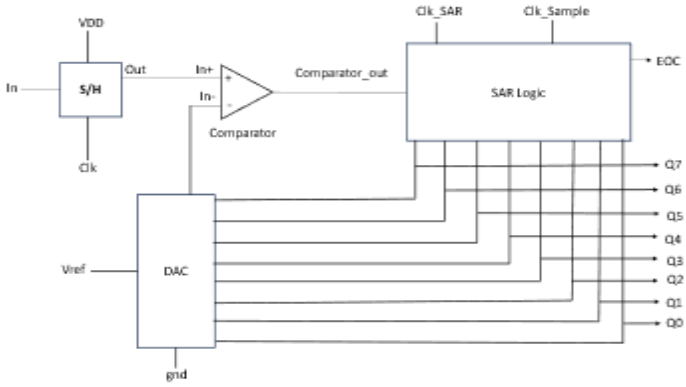

Figure 1 Block Diagram of SAR ADC

The Figure 1 illustrates the internal structure of a Successive Approximation Register (SAR) Analog-to-Digital Converter designed for low-power applications, particularly in biomedical systems.

- The process starts with the **Sample and Hold (S/H) circuit**, which captures the incoming analog signal and holds it steady during the conversion process. This ensures the signal doesn't fluctuate while the ADC performs its operations.

- The held analog voltage is then passed to the **Comparator**, which compares the sampled signal with a reference voltage provided by the **Digital-to-Analog Converter (DAC)**. Based on this comparison, it outputs a logic level indicating whether the input is higher or lower than the DAC output.
- The result from the comparator is fed into the **SAR Logic** block, which operates based on a binary search algorithm. It successively determines each bit of the final digital output by adjusting the DAC's output and analyzing the comparator feedback.
- The **DAC** receives digital input from the SAR logic and converts it back into an analog voltage to be used for the next comparison step. This feedback loop continues until all bits (from Q7 to Q0) are resolved.
- The system is synchronized using two control clocks: **Clk_Sample**, which controls the sampling timing and **Clk_SAR**, which governs the bit-by-bit approximation process. An **End-of-Conversion (EOC)** signal indicates the completion of the conversion.

Figure 2 SAR ADC Circuit using Verilog-A

The Figure 2 illustrates presents the structural layout of a SAR ADC tailored for processing sinusoidal input signals. The design, implemented using the Cadence Virtuoso platform, showcases the core functional units required for analog-to-digital conversion. These include the Sample and Hold (S/H) unit, a Comparator, a Digital-to-Analog Converter (DAC) and the SAR Logic block.

Each component is interconnected to enable the sequential approximation process. The S/H circuit captures and maintains the analog input, which is then compared against reference levels generated by the DAC. Guided by the comparator's output, the SAR logic iteratively refines the digital estimate of the input voltage. This coordinated workflow results in an accurate digital representation of the analog sine wave signal, optimized for low power and precision.

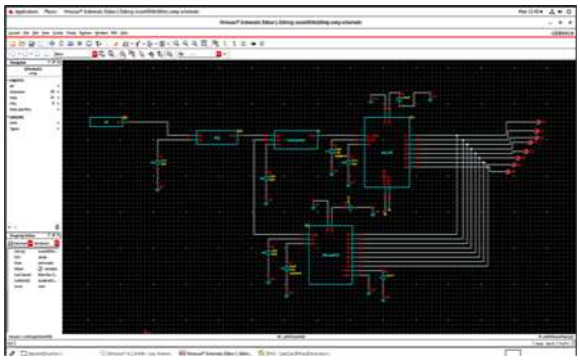

Figure 3 Schematic View of SAR ADC Circuit with ECG Input Using Cadence Virtuoso

The Figure 3 showcases the detailed schematic layout of the SAR ADC designed in Cadence Virtuoso. The design incorporates all key modules including the Sample and Hold circuit, Comparator, SAR Logic and Digital-to-Analog Converter (DAC). Each functional block is clearly defined and interconnected, forming the complete data conversion path from the analog input to the digital output.

In this configuration, an ECG (electrocardiogram) signal is provided as the analog input. The Sample and Hold circuit captures the incoming ECG waveform and stabilizes it for consistent conversion. This is especially critical for medical signals, which often have subtle variations and require high resolution and timing precision.

The comparator then compares this sampled ECG value with the reference voltage generated by the DAC. Based on the result, the SAR logic updates the digital code through a bit-by-bit approximation process. The digital output lines connected to the right side of the schematic represent the final quantized output corresponding to the ECG input.

5. RESULTS

The SAR ADC was designed and simulated using Verilog-A on a 90nm CMOS process. Key components—namely the sample-and-hold circuit, comparator, DAC and SAR logic—were modeled to evaluate the behavior of the converter during real-time signal processing.

Figure 4: Transient Waveform of the SAR ADC Output

The Figure 4 presents the detailed bit-level activity of an 8-bit SAR ADC as it converts an analog sine wave into its digital form. The smooth transitions of the input signal (top waveform) are matched by corresponding shifts in digital output lines (D7 to D0), with each bit toggling based on the successive approximation algorithm. The timing alignment and bit transitions confirm proper operation of each component—sample-and-hold, comparator, DAC and SAR logic—under simulated conditions.

Figure displays the transient waveform output from the simulation. The input signal applied is a sine wave, which undergoes step-by-step digital approximation by the ADC. Each horizontal line in the plot corresponds to one bit of the 8-bit digital output, from the most significant bit (D7) down to the least significant bit (D0).

As the simulation progresses, the SAR logic begins its binary search. At the start of each conversion cycle, typically triggered by a clock pulse, the MSB (D7) is tentatively set. The DAC uses this digital guess to produce a reference voltage, which is then compared with the sampled analog input. Depending on whether the reference is higher or lower than the input, the comparator directs the SAR logic to retain or reset the bit. This process continues sequentially through all bits, refining the digital representation of the analog input.

The waveform clearly shows the expected bit transitions: higher-order bits stabilize early, while lower-order bits toggle more frequently, indicating finer resolution. The combined effect produces a digital output that mirrors the shape of the input sine wave, verifying the accuracy and functionality of the SAR ADC.

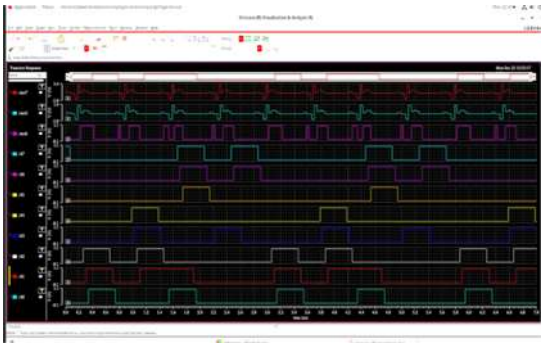

Figure 5 Output Response of SAR ADC for ECG Input Signal

The Figure 5 illustrates the digital output generated by the SAR ADC when an ECG waveform is applied as the input. The simulation demonstrates the ADC's capability to track and convert the dynamic features of the ECG signal—such as P-waves, QRS complexes, and T-waves—into a corresponding digital representation.

The analog ECG signal, known for its low amplitude and slowly varying nature, is first sampled and held steady by the Sample and Hold circuit. The SAR logic then initiates its binary approximation process, guided by the comparator's feedback and the DAC's generated references. This bit-by-bit refinement results in an accurate 8-bit digital code at each sampling instant.

Each bit in the output reflects the ADC's decision at a specific resolution level, with higher-order bits determining the signal's coarse shape and lower-order bits refining the finer details. The waveform output validates the ADC's suitability for biomedical applications, confirming that it can effectively handle low-frequency, low-amplitude physiological inputs with minimal distortion and high fidelity.

6. CONCLUSION

This work proposes a fully modeled SAR ADC in Verilog-A with clear emphasis on biomedical signals. The comparison highlights its edge over existing techniques by combining simulation, energy efficiency and resolution. The modular architecture ensures potential adaptability for future wearable healthcare applications.

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Authors Biography

Dr. Girija S, holds a degree in Electronics and Communication Engineering from Bangalore University, along with a master’s specialization in Computer Science from Visvesvaraya Technological University, Karnataka, where she also focused on research in VLSI. She began her career as a software engineer and is currently serving as an Assistant Professor in the Department of Electronics and Communication Engineering at Dr. Ambedkar Institute of Technology. Her areas of interest include Computer Programming, Data Computation, VLSI, Reversible Logic and Embedded Systems.

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