WWW.IJRPR.COM

International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

Improvement of on current in MOSFET with Hetero Structure (Si-Ge)

Aniruddha Ghosh[a*], Anirban Patra[a], Atanu Biswas[a], Ripan Ghosh[a], Akash Koner[a]

[a]Dept. Of ECE, JIS College of Engineering, Kalyani, West Bengal, India
*aniruddha.ghosh@jiscollege.ac.in

A B S T R A C T :

Recent advances in group-IV alloy heterostructures have generated significant excitement and optimism, reinforcing the idea that Si-Ge-based technologies could revolutionize the next generation of VLSI/ULSI systems. One of the major technical hurdles lies in the deposition of ultrathin dielectric films on strained group-IV alloy layers. As metal-oxide-semiconductor devices continue to shrink in size, there is growing interest in high-permittivity (high-K) materials as potential replacements for traditional gate dielectrics. Source is made with Si and channel is made by Ge. Here, Si-Ge hetero structure is created by proposed structure. Due to hetero structure, on current of MOSFET is improved. Improvement of on current mainly focused in this paper. The proposed device delivers an increased on-current and exhibits a sharper switching characteristic.

Keywords: MOSFET, Double Gate, Hetero Structure (Si-Ge), Hetero Dielectric High -K Oxide material, Subthreshold slope, On-state current

1. INTRODUCTION

CMOS technology remains one of the most widely adopted platforms in the semiconductor industry due to its seamless integration with integrated circuits (ICs). As MOSFET dimensions continue to shrink—leading to a doubling of transistor count approximately every two years—challenges such as short-channel effects and increased leakage currents arise due to reduced channel lengths. To address these issues, innovative device architectures and technologies have been introduced. Among them, double-gate MOSFETs have demonstrated superior performance, particularly in amplifier applications, compared to conventional single-gate designs. Additionally, silicon-based MOSFETs are known for their robustness in extreme environments and have been employed in diverse fields, including biomolecular sensing. Increasing the number of gates enhances the transistor's current driving capability, contributing to overall device efficiency.

Si-Ge hetero structure is essential to increase the on current in MOSFET. Double gate enhancing the controllability over channel, hence improves the device performance. If the on current improves that's mean on-off current ratio improves. As a result, Subthreshold slope (SS) reflects more improvement and switching speed enhanced.

2. METHODOLOGY

Enhancing the on-current of a MOSFET is critical for improving its performance, particularly in digital and analog circuits. Several strategies are commonly employed to achieve this:

Channel Engineering

- Use high-mobility materials: Replace or alloy silicon with materials like strained silicon, Si-Ge [1], or pure germanium (Ge) to improve carrier mobility. Here, Si-Ge structure is implemented in proposed structure.
- Strain engineering: Applying tensile strain for NMOS or compressive strain for PMOS can enhance carrier mobility, thereby boosting on-current [2].

Gate Engineering

- High-k dielectrics and metal gates: These reduce gate leakage and allow for a thinner equivalent oxide thickness (EOT), improving gate control over the channel [3].
- Work function tuning: Adjusting the gate work function can help optimize threshold voltage and improve drive current.

Device Architecture

- Multi-gate structures (e.g., Double-Gate MOSFETs): These improve electrostatic control over the channel and allow higher drive currents by reducing short-channel effects [4].

Doping and Source/Drain Engineering

- Heavily doped source/drain regions: Reduce series resistance, which helps improve on-current [5].
- Shallow junctions: Minimize parasitic resistances and improve carrier injection into the channel.

Scaling Supply Voltage and Threshold Voltage

- Lower threshold voltage can increase on-current but may raise off-state leakage; hence it must be carefully balanced [6].

Channel Length Scaling

- Reducing the channel length increases electric field strength and carrier velocity, thus enhancing on-current—though it must be controlled to prevent short-channel effects [7].

In this paper, Proposed structure with Si-Ge hetero region, hetero dielectric high K oxide layer and double gate, is displayed in Fig.-1. Silver – Chromium combination also play an important role in proposed structure.

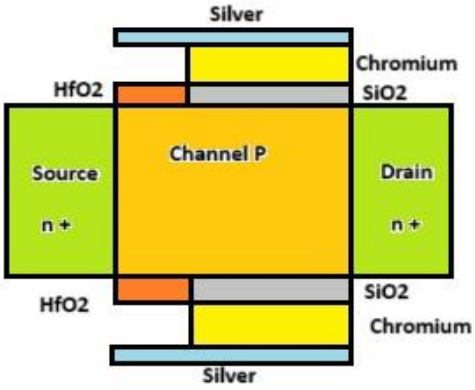

Fig. 1 – Structure of MOSFET

The above hetero structure introduces high band gap material silicon (Si) and low band gap material germanium (Ge) in same structure. Due to this hetero structure, drain current is improved. The hetero dielectric oxide layer, composed of SiO_2 and HfO_2, plays a crucial role in minimizing hot carrier tunnelling into the gate and suppressing gate-induced drain leakage (GIDL) [8]. Additionally, double-gate structures offer improved control over the channel potential. The dimension of the following structure and doping concentration as follows:

- Gate length: 50 nm
- SiO_2 layer length: 10 nm
- HfO_2 layer length: 40 nm
- Gate oxide thickness: 3 nm
- Body thickness: 30 nm
- Chromium thickness: 15 nm
- Silver thickness: 2 nm
- Source doping: $1.5*10^{21}/cm^3$
- Drain doping: $5*10^{20}/cm^3$
- Channel doping: $1*10^{17}/cm^3$
- Total device length: 100 nm

The hetero dielectric oxide layers provide direct regulation of both the channel current and the channel itself. The simulation methodology presented in this paper is primarily outlined in the flowchart shown in Fig. 2.

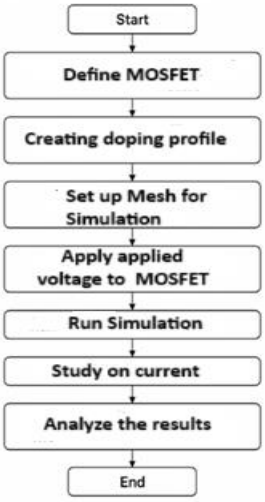

Fig. 2 – Flow chart diagram of Simulation work

3. RESULTS AND DISCUSSION

Sentaurus TCAD is used to simulate the proposed structure. Simulate the above structure using Silicon-Germanium (Si-Ge) Mainly, focus is reflected to extract on current from drain characteristics (i.e I_D Vs V_{GS}, keeping V_{DS} constant). The range of V_{GS} is -0.2 to 1.5 V, keeping V_{DS} = 0.5 V. Fig. 3 describes simulated structure and drain characteristics of proposed structure.

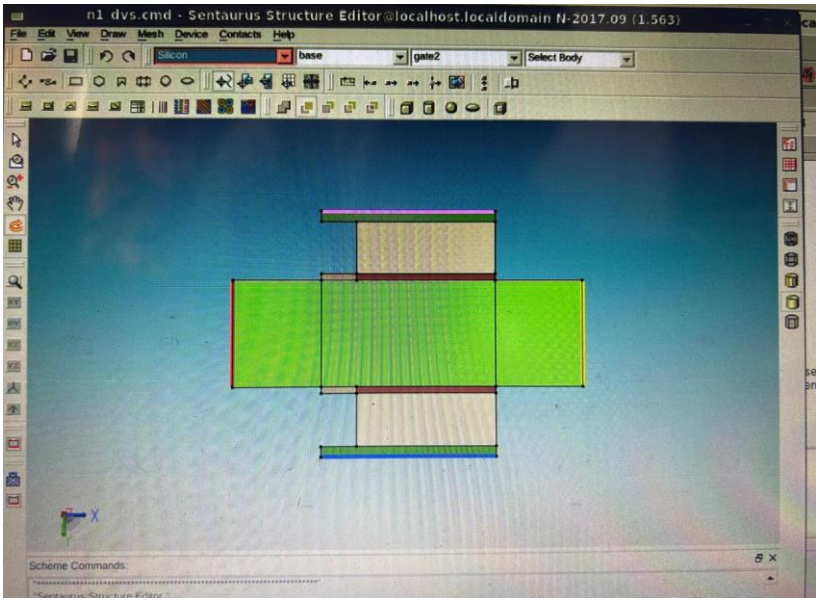

Fig. 3(a) – Simulated Structure

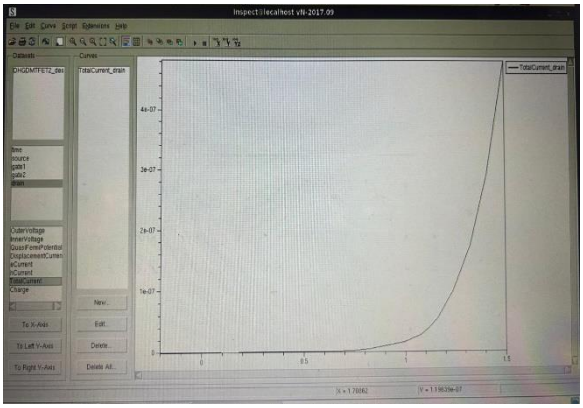

Fig. 3(b) – Drain characteristics (I_D Vs V_{GS}) without log scale

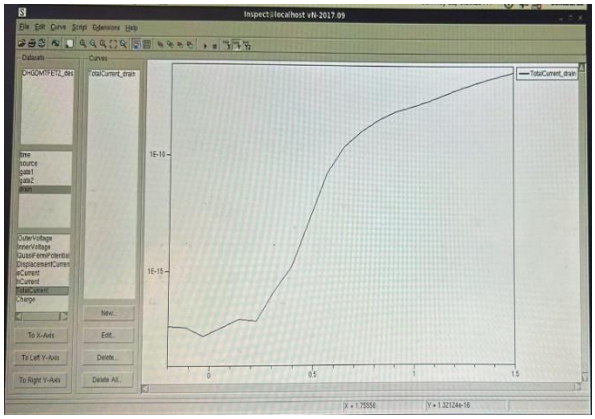

Fig. 3(c) – Drain characteristics (I_D Vs V_{GS}) with log scale

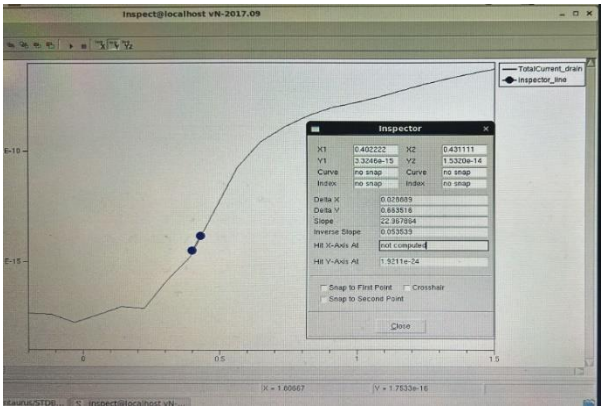

Fig. 3(d) – SS recorded about 53 mV/dec (inverse slope)

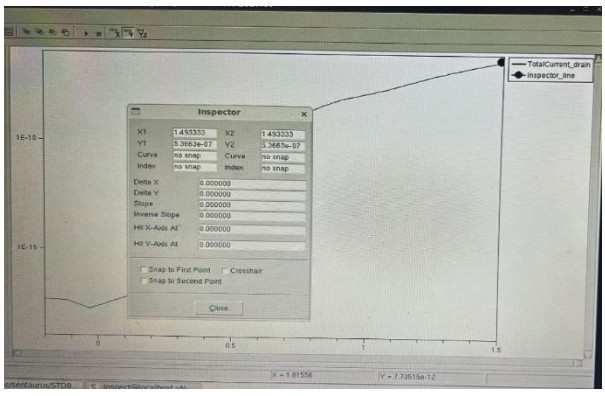

Fig. 3(e) – On current recorded about 5.36*10 $^{-7}$ A

In general, typical value of on current of conventional MOSFET in order of 10^{-10}. In proposed structure, obtained on current value is in order of 10^{-7}. Therefore, it can be concluded that the ON-current of the proposed structure has been enhanced. The improvement in subthreshold slope (SS) also indicates a better ON/OFF current ratio. The proposed Si- and Ge-based model demonstrates a subthreshold slope below the conventional limit of 60 mV/dec, [9] highlighting its superior switching performance compared to traditional MOSFETs. Here, some fluctuation occurs in below sub threshold condition.

4. CONCLUTION

Based on the simulation results, the proposed Si–Ge-based model achieves a subthreshold slope (SS) below the conventional MOSFET limit, with a value around 53 mV/dec. An improved SS indicates enhanced power efficiency. In this design, the heterostructure of silicon and germanium contributes to increased ON-current (or drain current), while the use of a hetero high-k dielectric layer helps minimize gate leakage current. As a result, the OFF-current behaviour is significantly improved. Future work will focus on applying the proposed structure in biosensing applications, where the silver–chromium combination has shown high effectiveness.

REFERENCES

[1] Ranita Basu, A review on single crystal and thin film Si–Ge alloy: growth and applications, DOI: 10.1039/D2MA00104G.

[2] Min Chu, Yongke Sun, Umamaheswari Aghoram, and Scott E. Thompson, Strain: A Solution for Higher Carrier Mobility in Nanoscale MOSFETs, Vol. 39:203-229 (Volume publication date August 2009), https://doi.org/10.1146/annurev-matsci-082908-145312.

, Design of ion-implanted MOSFET's with very small physical dimensions, IEEE J. Solid State Circ. 9 (5) (Oct. 1974) 256e268.

[3] Norani Bte Atan; Ibrahim Bin Ahmad; Burhanuddin Bin Yeop Majlis, Effects of high-K dielectrics with metal gate for electrical characteristics of 18nm NMOS device, 2014 IEEE International Conference on Semiconductor Electronics (ICSE2014), DOI: 10.1109/SMELEC.2014.6920794.

[4] P.M. Solomon; K.W. Guarini; Y. Zhang; K. Chan; E.C. Jones; G.M. Cohen, Two gates are better than one [double-gate MOSFET process], IEEE Circuits and Devices Magazine (Volume: 19, Issue: 1, January 2003), DOI: 10.1109/MCD.2003.1175108.

[5] J.J. Sun; R.F. Bartholomew; K. Bellur; A. Srivastava; C.M. Osburn; N.A. Masnari, The effect of the elevated source/drain doping profile on performance and reliability of deep submicron MOSFETs, IEEE Transactions on Electron Devices (Volume: 44, Issue: 9, September 1997), DOI: 10.1109/16.622606.

[6] Shih-Wei Sun; P.G.Y. Tsui, Limitation of CMOS supply-voltage scaling by MOSFET threshold-voltage variation, IEEE Journal of Solid-State Circuits (Volume: 30, Issue: 8, August 1995), DOI: 10.1109/4.400439.

[7] Yuan Taur, MOSFET channel length: extraction and interpretation, IEEE Transactions on Electron Devices (Volume: 47, Issue: 1, January 2000), DOI: 10.1109/16.817582.

[8] Yang-Kyu Choi, Daewon Ha, Tsu-Jae King and Jeffrey Bokor, Investigation of Gate-Induced Drain Leakage (GIDL) Current in Thin Body Devices: Single-Gate Ultra-Thin Body, Symmetrical Double-Gate, and Asymmetrical Double-Gate MOSFETs, DOI 10.1143/JJAP.42.2073.

[9] Fei Liu; Chenguang Qiu; Zhiyong Zhang; Lian-Mao Peng; Jian Wang; Hong Guo, "Dirac Electrons at the Source: Breaking the 60-mV/Decade Switching Limit", IEEE Transactions on Electron Devices (Volume: 65, Issue: 7, July 2018), DOI: 10.1109/TED.2018.2836387.