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Improvement of Leakage Off Current in MOSFET with Si and Ge Based Structure

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A B S T R A C T

In contemporary nano-scale CMOS technology, leakage current has emerged as acritical limiting factor in the optimization of device performance and energy efficiency. This study presents the simulation-based investigation into the suppression of off-state leakage current in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). The short-channel effect analysis is done to understand leakage mechanisms such as subthreshold conduction, gate- induced drain leakage (GIDL), and tunnelling. These phenomena are analytically addressed by modifying threshold voltage behaviour through channel engineering and high-κ dielectric integration. Implementation of structural optimizations is done through the use of retrograde well doping, lightly doped drain profiles within the TCAD framework. Simulation results demonstrate a significant reduction in off-state current in magnitude, validating the effectiveness of the proposed design modifications. This synergistic approach and device-level simulation offers a viable pathway toward leakage minimization in advanced MOSFET architectures. In this paper, extra p type with lightly doped region is introduced in between channel and drain for reducing gate leakage current. Double gates are used for better control over channel current.

Keywords: MOSFET, GIDL, Double Gate, Hetero Dielectric, Stacked Source, Subthreshold slopes, OFF-state current

1. INTRODUCTION

Over the past decades, transistor scaling has been a key strategy to achieve reduced power consumption and enhanced performance. When channel lengths dropped below 100 nm, the use of thinner gate oxides was introduced to boost drain current. However, this approach led to significant challenges related to increased power dissipation. To sustain high drain current levels, the threshold voltage also needed to be proportionally scaled down. Yet, this reduction in threshold voltage in miniaturized transistors causes a substantial rise in subthreshold leakage current [1]. Leakage in the weak inversion region is influenced by the threshold voltage [2], making it a key contributor to increased leakage current in short-channel transistors. Additionally, in these devices, a rise in drain voltage causes an expansion of the depletion region between the drain/source and the substrate, which further elevates leakage current. Another contributing factor is the surface current in the channel, which arises due to drain-induced barrier lowering (DIBL). Consequently, leakage current is affected by several parameters, including channel length, drain/source junction depth, gate oxide thickness, and threshold voltage. Collectively, the phenomena that lead to reduced threshold voltage and increased leakage in short-channel transistors are known as short-channel effects (SCEs) [3]. With advancements in semiconductor technology, leakage current in MOS devices has emerged as a critical limitation. As device dimensions shrink into the sub-nano meter range, the leakage current components approach magnitudes comparable to the ON-state current.

To manage short-channel effects (SCEs) and reduce the high leakage currents in scaled transistors, innovative technologies and advanced device designs are essential. One effective approach is channel doping engineering, where modifications to the doping profile within the channel alter the electrostatic potential and the extent of the depletion region. Techniques such as halo doping and pocket implantation [4] have been employed to reshape the doping distribution, effectively mitigating SCEs and thereby reducing leakage currents. Additionally, engineering of the gate material has been proposed as another strategy to suppress leakage and control SCEs more effectively.

The key idea in this work is to reduce the leakage current by extra p type with lightly doped region is introduced in between channel and drain just link pocket or halo doping. Here, stacked Source region (combination of Si and Ge) and hetero dielectric (combination of HfO_2 and SiO_2) are introduced to improved the performance of the proposed structure. Sub threshold slope is also investigated in this paper. The comparison between Si based structure and Ge based structure is also made during the analysis. Short-channel effects (SCEs) play a major role to implement the MOSFET design. In this paper, main focus is done on gate- induced drain leakage (GIDL). Gate-Induced Drain Leakage is a type of leakage current that occurs in MOSFETs, particularly in short-channel devices, and becomes more prominent as device dimensions scale down.

2. METHODOLOGY

Here, extra p type material is used for reducing GIDL. Basically, GIDL is the leakage current that flows between the drain and the substrate (or body) when the gate is at a low voltage and the drain is at a high voltage, typically when the transistor is supposed to be off. Gate- induced drain leakage Mechanism are as follows:

- When a high drain voltage and a low gate voltage are applied, a strong electric field develops near the drain-edge of the gate.
- This field causes band-to-band tunneling or impact ionization, especially in heavily doped regions.
- As a result, electron-hole pairs are generated, leading to a current even when the transistor should be in the off state.

Key Contributing Factors of gate- induced drain leakage are as follows:

- Thin gate oxides
- High drain voltages
- Short channel lengths
- Sharp doping gradients

Effects gate- induced drain leakage are as follows:

- Increases off-state power consumption
- Degrades device reliability
- Becomes a major issue in low-power and high-performance applications

Suppression Techniques for gate- induced drain leakage is:

- Use of high-K dielectrics
- Channel engineering (e.g., retrograde wells, halo doping)
- Drain engineering (e.g., lightly doped drain structures)
- Gate stack modifications to reduce vertical electric fields

In this paper, Proposed structure with extra p region, stacked source hetero dielectric oxide layer and double gate, is reflected in Fig.-1.

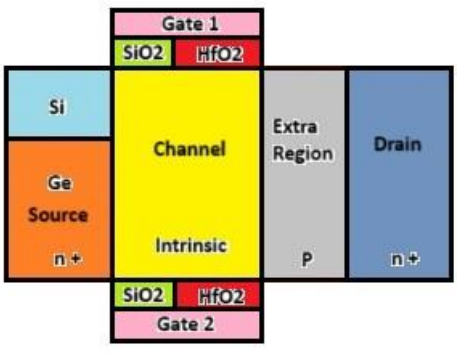

Fig. 1 – Structure of MOSFET

The above structure introduces stacked source with upper layer -high band gap material silicon (Si) and lower layer - low band gap material germanium (Ge). Due to this stacked source structure [5], drain current is improved. The hetero dielectric oxide layer [6] (combination of SiO_2 and HfO_2) play an important role to reduce hot carrier tunnelling to gate and GIDL. Whereas, double gates have better controllability over channel as well as extra region. The dimension of the following structure and doping concentration as follows:

- Gate length: 50 nm
- SiO_2 layer length: 20 nm
- HfO_2 layer length: 30 nm
- Gate oxide thickness: 2 nm

- Source length: 25 nm
- Drain length: 25 nm
- Si layer thickness in Source region: 10 nm
- Ge layer thickness in Source region: 15 nm
- Source doping: $1*10^{21}/cm^3$
- Drain doping: $1*10^{18}/cm^3$ (lightly doped)
- Channel doping: $1.5*10^{14}/cm^3$
- Extra region doping: $1.5*10^{16}/cm^3$

The hetero dielectric oxide layers have direct control on channel current and also channel. Here, drain region's doping level is low, that's mean current from drain to body or extra region is reduced. Mainly, the simulation work of the paper is illustrated through the following flow chart diagram in Fig.2:

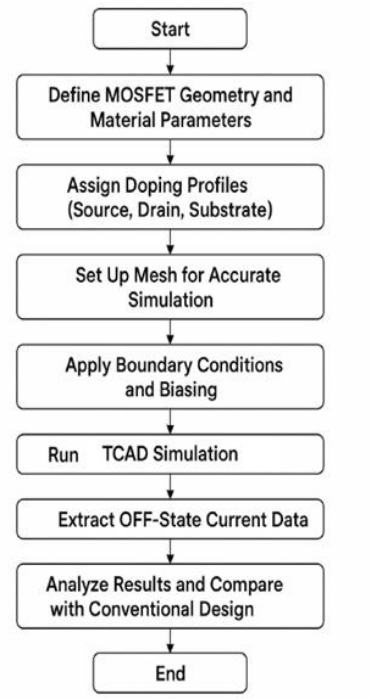

Fig. 2 – Flow chart diagram of Simulation work

3. RESULTS AND DISCUSSION

To simulate the above structure, Sentaurus TCAD is used. Simulate the above structure using Silicon (Si) based material. Channel, extra region and drain – all are silicon based but Germanium (Ge) is used in under lying layer in source region. Mainly, focus is reflected to extract off current from drain characteristics (i.e I_D Vs V_{GS}, keeping V_{DS} constant). The range of V_{GS} is -0.1 to 1.5 V, keeping V_{DS} = 0.6 V. Fig. 3 describes simulated structure and drain characteristics of proposed structure.

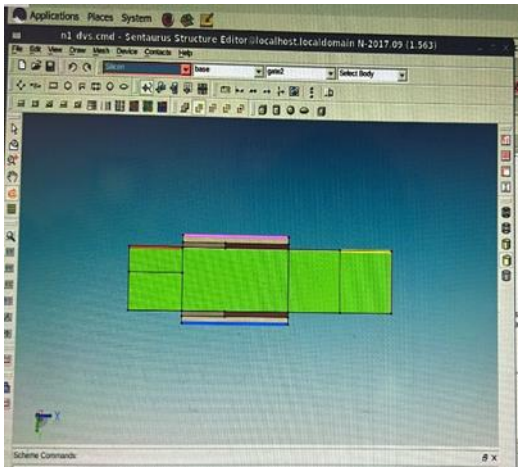

Fig. 3(a) – Simulated Structure

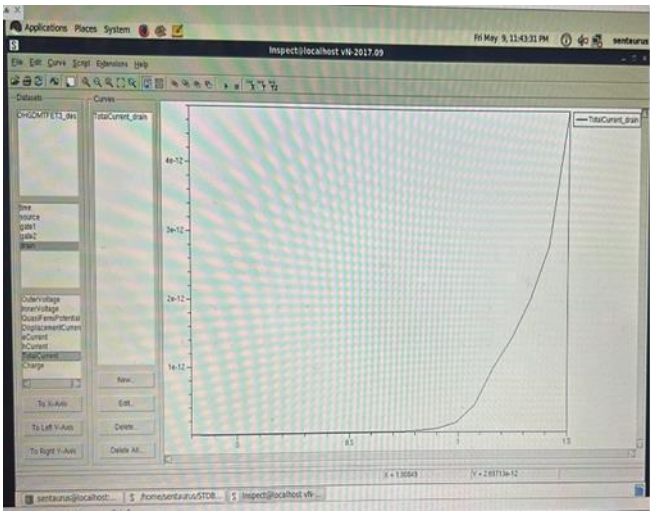

Fig. 3(b) – Drain characteristics (I_D Vs V_{GS}) without log scale

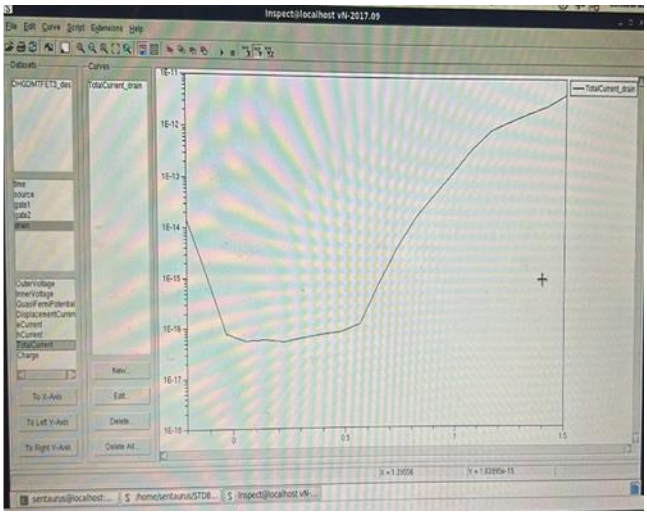

Fig. 3(c) – Drain characteristics (I_D Vs V_{GS}) with log scale

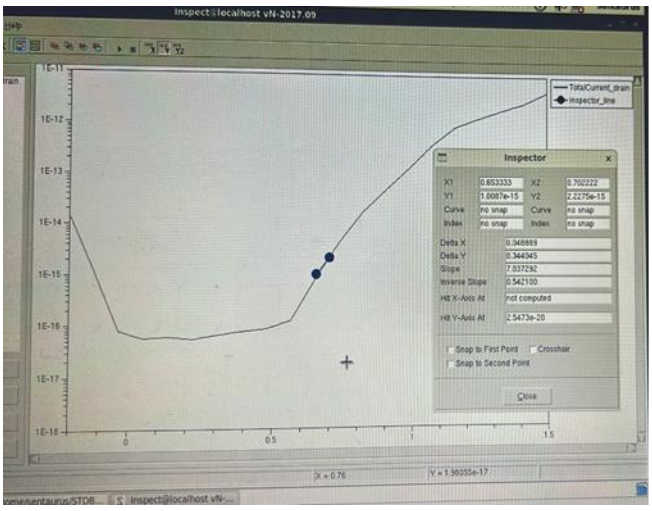

Fig. 3(d) – SS recorded about 54 mV/dec (inverse slope)

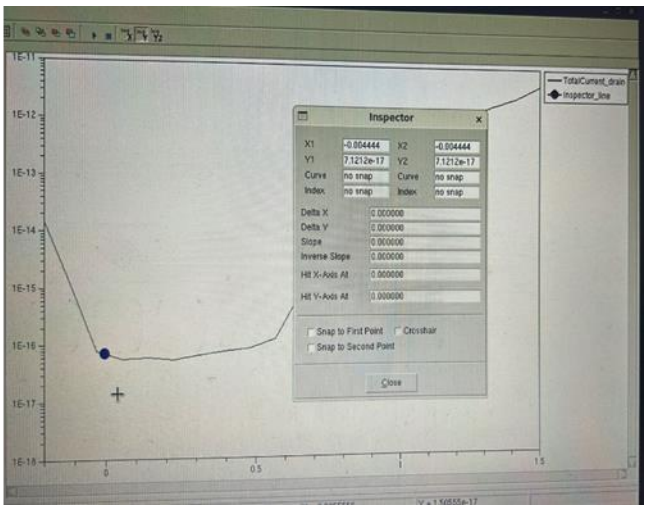

Fig. 3(e) – Off current recorded about 7.12*10 $^{-17}$ A

In general, typical value of off current of conventional MOSFET in order of 10^{-15}. In proposed structure, obtained off current value is in order of 10^{-17}. Hence, the conclusion can be drawn that off current of the proposed structure is improved. Here, SS improved that's mean on and off current ratio also improved. Proposed Si and Ge based model having subthreshold slope (SS) below of typical value (60 mV/dec) of conventional MOSFET [7].

4. CONCLUTION

After analyzing the simulation result, proposed Si and Ge based model having subthreshold slope (SS) below of limitation value of MOSFET. The value of SS (about 54 mV/dec). When SS improved that's mean power efficiency is also improved. In proposed structure, stacked source increases the on current or drain current and hetero high K oxide material reduces the gate leakage current. Hence, the off current response is improved using proposed structure. The future work is focussed on more reduction of leakage off current in MOSFET which leads to power efficiency of the device.

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