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Improvement of on and off current of TFET with low Band gap Material (Ge) based Model

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A B S T R A C T :

The escalating power dissipation in next-generation digital systems poses severe thermal management challenges, which are mitigated to some extent by lowering the supply voltage. Low-power systems require transistors that exhibit smaller subthreshold slopes (SS). In recent years, Tunnel Field Effect Transistors (TFETs) have emerged as promising alternatives to conventional MOSFETs, addressing the challenges of continued device dimension scaling. TFETs offer advantages such as minimized short channel effects (SCE), low OFF-state current (I_{OFF}), and a steep subthreshold slope (SS); however, their primary limitation is the significantly low ON-state current (I_{ON}). A straightforward approach to overcome this problem to use low bandgap material in heterostructures. As a result, it improves drain current. To reduce the ambipolar current, use comparatively low doping level and higher band gap material in drain region. In this paper, using the proposed structure able to reduce subthreshold slopes (SS), reduce the OFF-state current (I_{OFF}) and increase the ON-state current (I_{ON}).

Keywords: TFET, BTBT, Heterostructure, Gate length optimization, Subthreshold slopes, Ambipolar current, ON-state current, OFF-state current, I_{ON}/ I_{OFF} ratio

1. INTRODUCTION

Here introduces the paper, and put a new structure to improved subthreshold slopes (SS). While TFETs offer several advantages over MOSFETs, they also face challenges and limitations. Including: -

1. Lower ON-Current: - TFETs typically have lower ON-current than MOSFETs [1], which can impact device performance.
2. Higher Fabrication Complexity: - TFETs require more complex fabrication processes than MOSFETs, which can increase manufacturing costs.
3. Material and Interface Challenges: - TFETs require careful selection of materials and interfaces to optimize device performance, which can be challenging.

Overall, TFETs offer promising advantages over MOSFETs, but further research and development are needed to overcome the challenges and limitations associated with these devices. Band to band tunneling (BTBT) is the key concept of Tunnel Field Effect Transistors. BTBT is mainly responsible for low power consumption. Tunnel Field Effect Transistor offers several benefits such as-

- Performance Benefits: -

1. Low-Power Consumption: - TFETs have lower sub-threshold leakage current, resulting in reduced power consumption [2].
2. Faster Switching Speed: - TFETs exhibit faster switching speed due to their tunnelling mechanism [3].
3. Improved Frequency Performance: - TFETs can operate at higher frequencies.

- Technological Benefits: -

1. Scaling: - TFETs can be scaled down to smaller sizes, enabling more transistor on a chip.
2. Lower Voltage Operation: - TFETs can operate at lower voltages, reducing thermal issues [4].
3. Increased Density: - TFETs enable higher integration density.

- Other Benefits: -

1. Reduced Thermal Issues: - TFETs generate less heat, reducing thermal management challenges.
2. Cost-Effective: - TFETs can be manufactured using existing CMOS infrastructure.

TFETs have the potential to be used in a wide range of applications, including low-power electronics, high-speed digital circuits, and analog circuits. Lower band gap material (Ge) is introduced in the structure to enhance the on current and higher band gap material is deployed with relatively lower doping in drain region to reduced off current in TFET. Proposed structure also improves on-off current ratio, hence improve subthreshold slopes (SS) below 60mV/dec [5].

2. DESIGN OF STRUCTURE

Here, Tantalum Nitride (TaN) [6] as gate material is used for its hardness, wear resistance, and conductivity, making it useful in various applications. HfO_2 (Hafnium Dioxide) is used to prevent gate leakage current (I_G) due to hot carrier tunnelling. Proposed structure is described in Fig.-1.

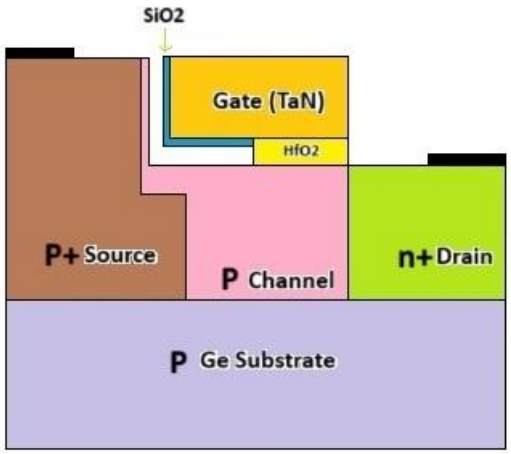

Fig. 1 – Structure of TFET

The above structure is p type TFET where p type germanium used as substrate. The dimension of the following structure and doping concentration as follows:

- Gate length: 100 nm
- Gate oxide length: 925 nm
- Gate oxide thickness: 20 nm
- Air gap thickness: 15 nm
- Air gap height: 680 nm
- Air gap length: 90 nm
- Sio_2 layer thickness: 5 nm
- Epilayer thickness: 8 nm
- Source doping: $1.5*10^{21}/cm^3$
- Drain doping: $1.5*10^{20}/cm^3$
- Channel doping: $5*10^{17}/cm^3$
- Source height: 850 nm
- Drain height: 145 nm
- Substrate thickness: 100 nm
- Source length: 650 nm (top)
- Source length: 1030 nm (bottom)
- Drain length: 800 nm

In this paper, implement an air cavity and functionalization layer for enhancing the electric field near the tunnelling junction. Here, Ge substrate is used for better tunnelling efficiency in TFET. Air gap consider as cavity in the proposed structure. Capacitive effect also improved here. L type gate shaped also improved leakage current because the use of HfO_2 and Sio_2. Metal layer thickness consider as 4 nm. Traditional MOSFET devices have reached their fundamental limitations in scaling and low-power performance, primarily due to their inability to achieve a subthreshold swing (SS) below 60 mV/decade at room temperature. In contrast, proposed Tunnel FETs (TFETs) have emerged as a promising alternative, utilizing band-to-band tunnelling (BTBT) to attain sub-60-mV/decade SS [7] under the same conditions.

3. RESULTS AND DISCUSSION

To simulate the above structure, Sentaurus TCAD is used. At first, simulate the above structure using Germanium (Ge) based material. Mainly, focus is done on drain characteristics (i.e I_D Vs V_{GS}, keeping V_{DS} constant). The range of V_{GS} is -0.2 to 1.5 V, keeping V_{DS} = 0.5 V. Fig. 2 describe simulated structure and drain characteristics using Germanium (Ge) based material.

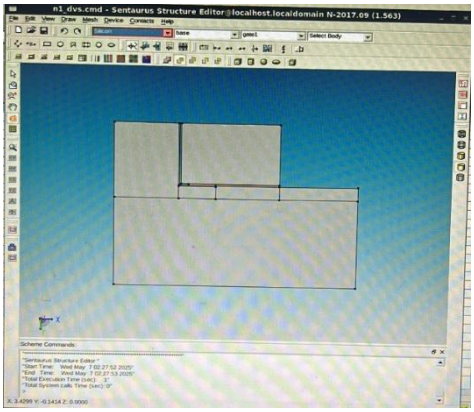

Fig. 2(a) – Simulated Structure

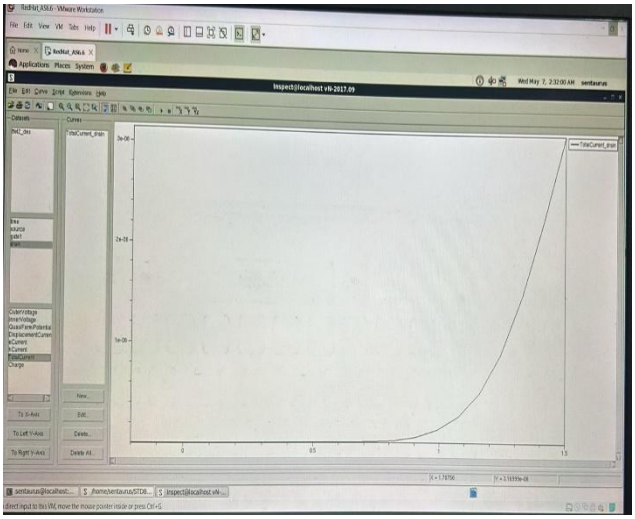

Fig. 2(b) – Drain characteristics (I_D Vs V_{GS}) without log scale

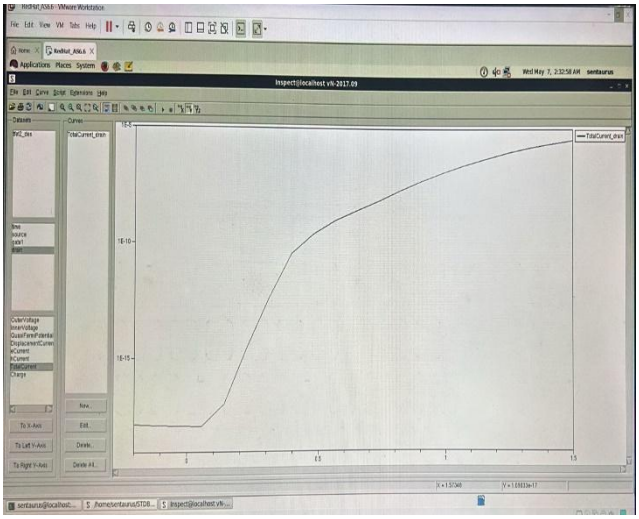

Fig. 2(c) – Drain characteristics (I_D Vs V_{GS}) with log scale

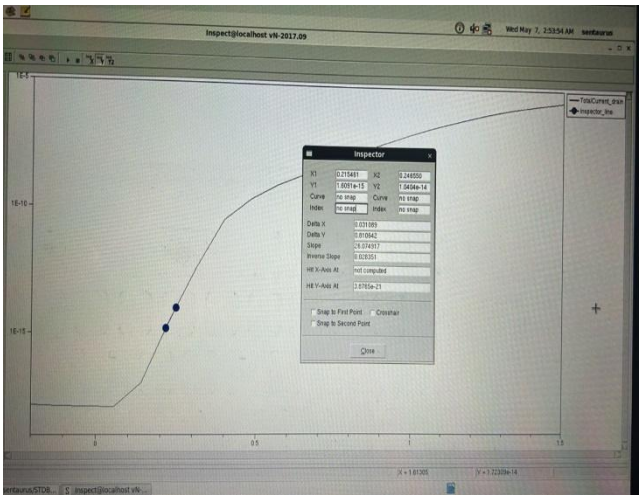

Fig. 2(d) – SS recorded about 28 mV/dec (inverse slope)

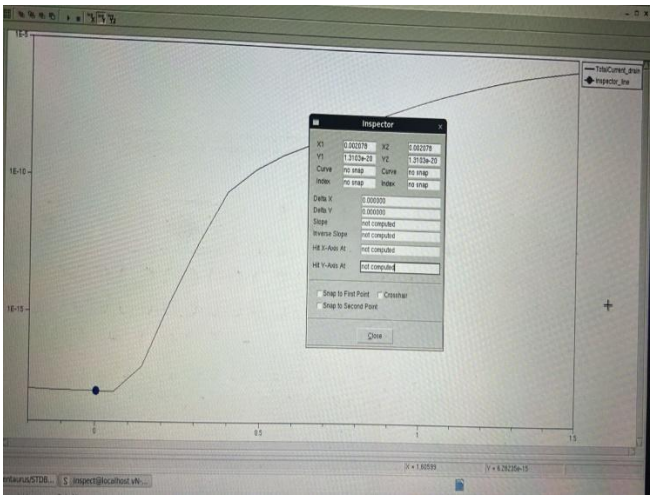

Fig. 2(e) – Off current recorded about $1.31*10^{-20}$ A

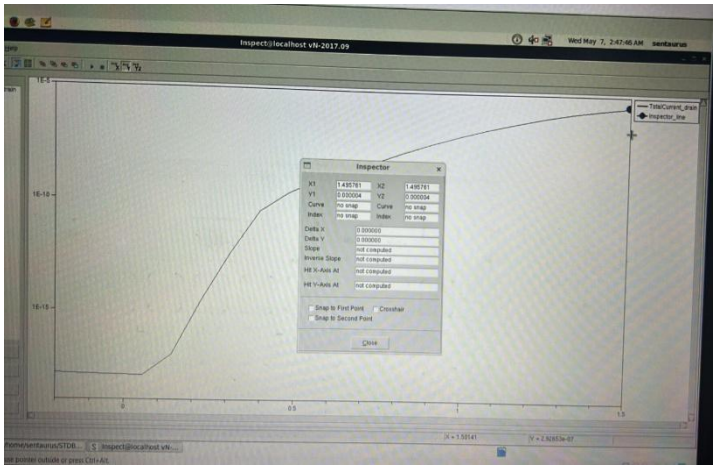

Fig. 2(f) – On current recorded about 4*10 $^{-6}$ A

Fig. 3 describe drain characteristics (i.e I_D Vs V_{GS}, keeping V_{DS} constant) using Silicon (Si) based material. The range of V_{GS} is -0.2 to 1.5 V, keeping V_{DS} = 0.5 V.

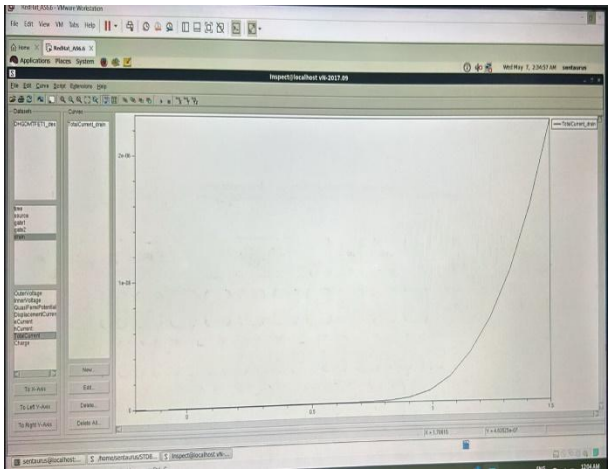

Fig. 3(a) – Drain characteristics (I_D Vs V_{GS}) without log scale

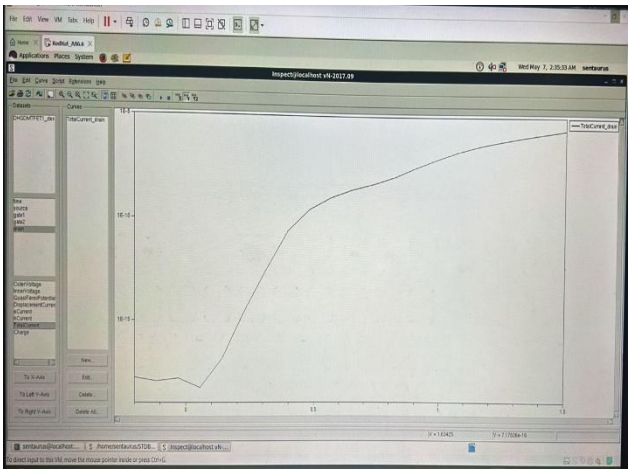

Fig. 3(b) – Drain characteristics (I_D Vs V_{GS}) with log scale

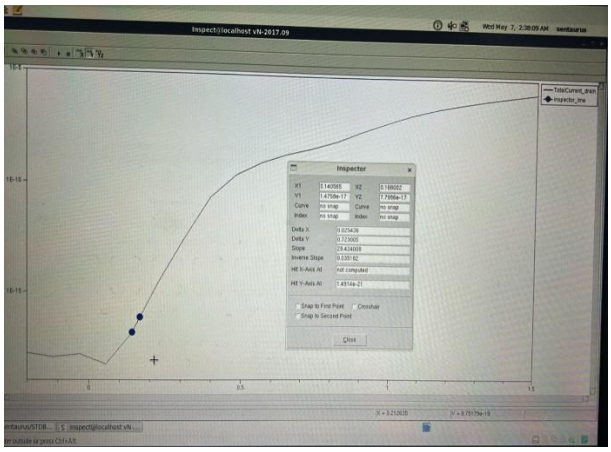

Fig. 3(c) – SS recorded about 35 mV/dec (inverse slope)

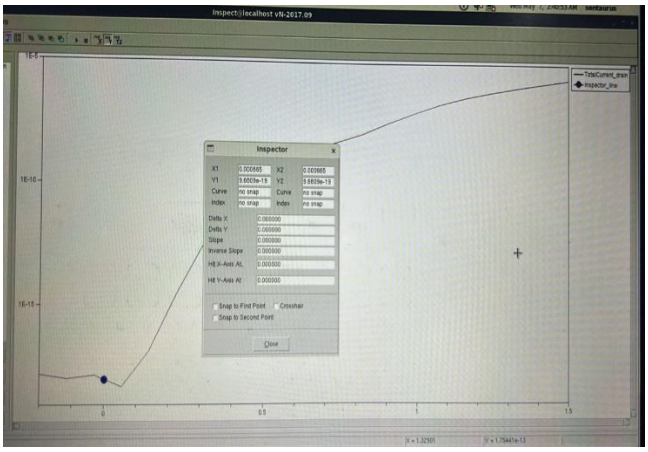

Fig. 3(d) – Off current recorded about 9.6*10 $^{-19}$ A

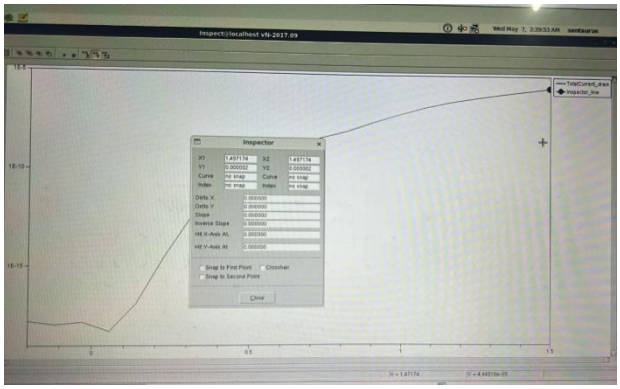

Fig. 3(e) – On current recorded about 2*10 $^{-6}$ A

If comparison done between Ge based and Si based model, the conclusion comes in the mind that Ge based model is better than Si based model in respect of SS, on current and off current. For Ge based structure, I_{ON}/ I_{OFF} ratio is the order of 10^{14} whereas I_{ON}/ I_{OFF} ratio of Si based is the order of 10^{12}. Low band gap material Ge having more tunnelling effect which improve the performance of proposed TFET structure. From drain characteristics of Si based structure, the observing factor is that there are certain fluctuations below sub threshold condition. For Ge based structure, no such fluctuations occur in drain characteristics that's why Ge based model is superior than Si based.

4. CONCLUTION

After analyzing the simulation result, proposed Ge based model having SS much below of limitation value 60 mV/dec of MOSFET. The value of SS (about 28 mV/dec) is also below the typical value around 40 mv/dec [8] of conventional TFET. The on -off current ratio is also improved in the order of 10^{12}.When SS improved that's mean power efficiency is also improved. So, the conclusion can be made that the proposed Ge based model is power efficient than the Si based. The future work is focussed on bio sensing with this proposed Ge based TFET model.

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