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A Seven-Level Cascaded Multilevel Inverter based on Simplified SVPWM Method

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A B S T R A C T :

Multilevel converters have gained significant attention in medium-voltage and high-power applications due to their superior performance over conventional two-level converters. Among the widely adopted modulation techniques for multilevel inverters, Sine Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are the most prominent. SVPWM, in particular, offers advantages such as better utilization of the DC link voltage and lower Total Harmonic Distortion (THD) in the output waveform when compared to SPWM. However, the traditional SVPWM method comes with certain challenges, including the need for complex calculations to determine the reference voltage vector's position, identify the appropriate sector and triangle, and reliance on memory-intensive lookup tables for switching vectors. To overcome these limitations, this paper proposes a simplified and improved SVPWM strategy tailored for a Cascaded H-Bridge Multilevel Inverter (CHBMLI). The proposed method eliminates the complexities associated with conventional SVPWM while maintaining its performance benefits. A seven-level CHBMLI is employed to implement and validate the effectiveness of the simplified SVPWM strategy, and its performance is benchmarked against the SPWM approach through MATLAB-based simulations.

Keywords: SVPWM, SPWM, Simplified SVPWM, CHBMLI.

1. Introduction

In recent years, there has been a significant rise in the demand for megawatt-level power equipment and medium-voltage systems, particularly within industrial sectors (Rodriguez et al., 2009). Many motor drive applications in industry require such high power and voltage levels to operate efficiently. To address these requirements, multilevel inverters have emerged as a highly effective solution (Kouro et al., 2010). These inverters generate stepped voltage waveforms by utilizing multiple DC voltage sources in conjunction with a network of semiconductor switches.

Compared to traditional two-level inverters, multilevel inverters offer several key advantages, including lower harmonic distortion in output currents and voltages, reduced voltage stress on power switches, minimized common-mode voltage, and improved output waveform quality (Rodriguez et al., 2002). Among the main topologies—Cascaded H-Bridge (CHBMLI), Flying Capacitor (FCMLI), and Diode-Clamped (DCMLI)—the CHBMLI is often preferred due to its simpler structure and lower component count, especially in terms of diodes and capacitors, which are more prevalent in the FCMLI and DCMLI designs (Rodriguez et al., 2007; Maurya et al., 2020).

The performance of multilevel inverters heavily depends on the modulation strategy employed. Widely used methods include Sine Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) (Attique et al., 2017). Phase Disposition-based SPWM is popular for its simplicity and low computational requirements (Sanjay et al., 2018). However, SVPWM typically delivers better performance, offering improved utilization of the DC bus voltage, reduced harmonic distortion, and the capability to operate within overmodulation regions (Chowdhary et al., 2020; Srivastava et al., 2020; Thakre et al., 2021; Hu et al., 2007; Thakre et al., 2020).
Despite these advantages, conventional SVPWM involves a series of complex steps, such as sector identification based on the reference voltage vector, triangle classification, dynamic vector timing calculation, switching sequence selection, pattern generation, and duty cycle computation for each semiconductor switch (Thakre et al., 2020; Manasa et al., 2011; Rushiraj et al., 2016). The presence of multiple switching states and overlapping sectors within the Space Vector Diagram (SVD) adds further complexity to the implementation (Sabarad et al., 2015; Ray et al., 2019; Ibrahim et al., 2014).

While some researchers have proposed simplified alternatives—such as decomposing a three-level SVD into basic two-level vector regions (Prasad et al., 2017; Ahmed et al., 2016)—these methods often become impractical for higher voltage levels due to increased complexity. Other techniques, such as the 60-degree coordinate approach (Wu et al., 2020), can encounter issues like incorrect switching sequences and capacitor voltage imbalances.

To address these challenges, this paper presents a novel, simplified SVPWM method specifically developed for a seven-level CHBMLI. The proposed strategy eliminates the need for sector detection, lookup tables, and complex computations, thereby streamlining the implementation while maintaining the performance advantages of traditional SVPWM.

2. Cascaded H-Bridge Multilevel Inverter

In recent years, the demand for equipment with megawatt-level power and medium voltage ratings has significantly increased, particularly across various industrial sectors (Rodriguez et al., 2009). Many motor drive systems used in industrial applications require this level of power and voltage to function efficiently. To meet these demands, multilevel inverters have emerged as the most effective solution (Kouro et al., 2010). These inverters generate a stepped voltage waveform using multiple DC voltage sources and semiconductor switches.

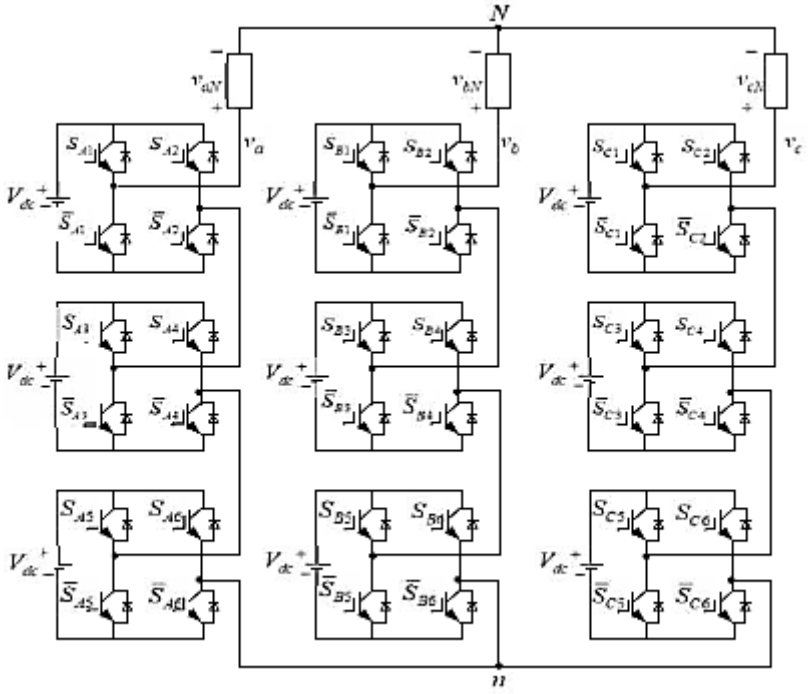

Figure 1. Seven-level cascaded multilevel inverter

3. PWM Techniques

Various modulation techniques are employed in multilevel power conversion systems to achieve efficient and accurate output. Among these, Sine Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are the most commonly implemented strategies. Specifically, for Cascaded H-Bridge Multilevel Inverters (CHBMLI), carrier-based PWM methods are predominantly used due to their compatibility and ease of implementation.

3.1 SPWM Technique

In CHBMLI systems, two main types of carrier-based SPWM techniques are utilized: level-shifted and phase-shifted PWM. In the SPWM method, a sinusoidal reference signal (modulating wave) is compared against multiple triangular carrier signals that are arranged vertically.

To generate a seven-level output voltage, six triangular carrier waves are needed, as depicted in Figure 2. These carrier signals all share the same amplitude and frequency. The output voltage of the inverter is controlled by adjusting the Amplitude Modulation Index (Ma), which determines how the sine wave amplitude compares to that of the carrier signals.

In multilevel inverter systems, the modulation index (Ma) is mathematically defined as:

$$M_a = \frac{V_m}{V_{cr}\,(m-1)}$$

Where, V_m represents modulating wave magnitude and V_{cr} represents individual carrier wave magnitude.

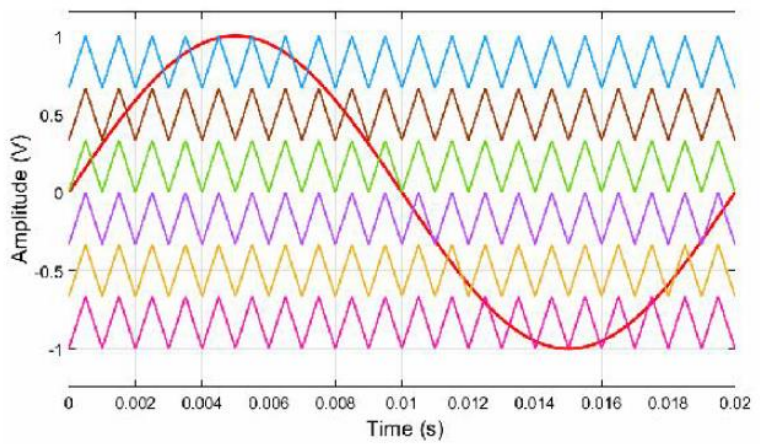

Figure 2. Sinusoidal reference wave and triangular carriers for a seven-level CHBMLI

3.2 Simplified SVPWM Technique

Conventional Space Vector Pulse Width Modulation (SVPWM) involves several computationally intensive steps, such as identifying the sector based on the reference voltage vector, determining the triangle region, calculating the ON times for the active voltage vectors, selecting redundant switching states, generating the appropriate switching sequence, and computing the ON durations for each switching device. To address these complexities, a simplified SVPWM technique is proposed. This method introduces an offset voltage to the reference phase voltages, which allows the modulation strategy to replicate the performance of conventional SVPWM while significantly reducing the computational burden. Additionally, it enhances the utilization of the DC bus voltage, enabling efficient inverter operation with a more straightforward implementation. The offset voltage is defined as:

$$V_{offset} = \frac{(V_{max} + V_{\min})}{2}$$

Here, Vmax and Vmin represent the maximum and minimum amplitudes of the reference phase voltages within a specific sampling period. By adding the calculated offset voltage Voffset to the reference voltages, all dynamic switching vectors in the multilevel inverter are effectively centered within the sampling interval. Figure 3 illustrates the simplified modulating signals along with the corresponding carrier waveforms. These modified space vector signals are then compared with the carrier waves to generate the gate pulses required to drive the IGBT switches.

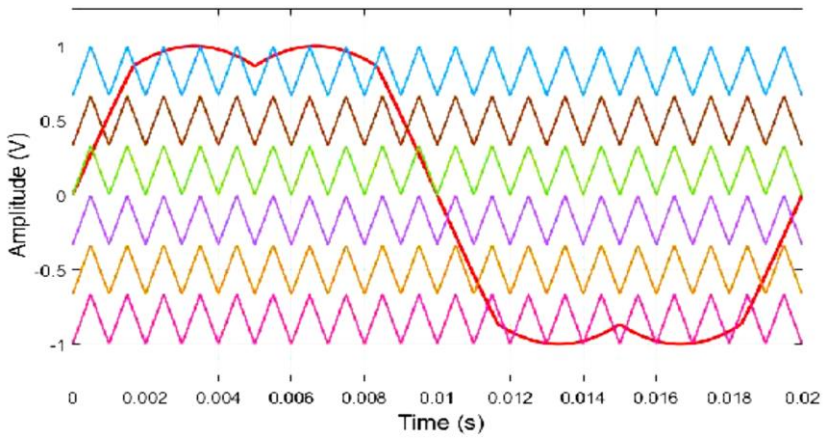

Figure 3. Space vector modulating wave and triangular carriers for a seven-level cascaded multilevel inverter

4. Simulation Results

A simulation study was conducted using MATLAB software to evaluate the effectiveness of the proposed simplified SVPWM technique. The simulation setup is based on a seven-level Cascaded H-Bridge Multilevel Inverter (CHBMLI) operating with an RL load. To thoroughly assess the performance, the system was tested at three different values of the amplitude modulation index (Ma).

For each value of Ma, the line voltage waveforms were generated using both the conventional SPWM and the proposed simplified SVPWM methods. In addition, the corresponding harmonic spectra were analyzed to compare the quality of output voltage. The detailed simulation parameters used for this study are listed in Table 1.

Table 1. Parameters of simulation

Parameter	Value
DC bus voltage	600 V
Switching Frequency	1050 Hz
Resistive load per phase (R)	50 ohms
Inductive load per phase (L)	20 mH

4.1 Simulation Results of the Seven-Level CHBMLI Using the SPWM Strategy

Figure 4 presents the implementation scheme of the SPWM strategy applied to a seven-level Cascaded H-Bridge Multilevel Inverter (CHBMLI). Figure 5 displays the output line voltage of the inverter operating with a modulation index Ma=1 using the SPWM technique, while the corresponding harmonic spectrum is shown in Figure 6. Similarly, Figure 7 illustrates the line voltage waveform for Ma=0.8, and the associated harmonic spectrum is depicted in Figure 8.

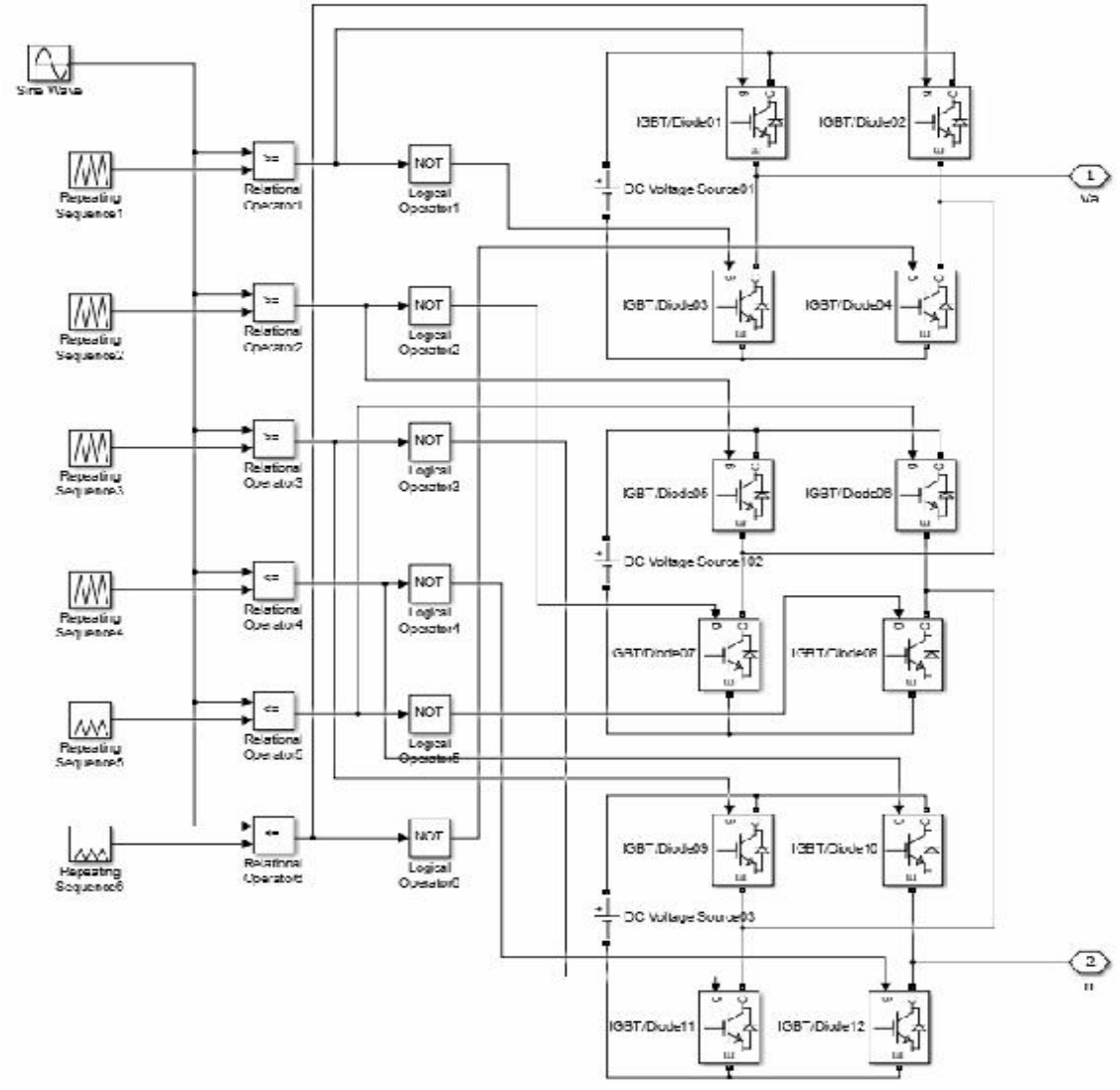

Figure 4. Scheme of the seven-level CHBMLI with SPWM strategy

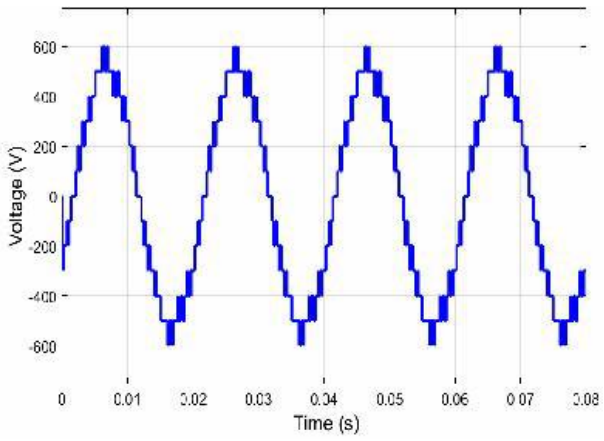

Figure 5. *Seven-level cascaded multilevel inverter line voltage in case of M_a=1*

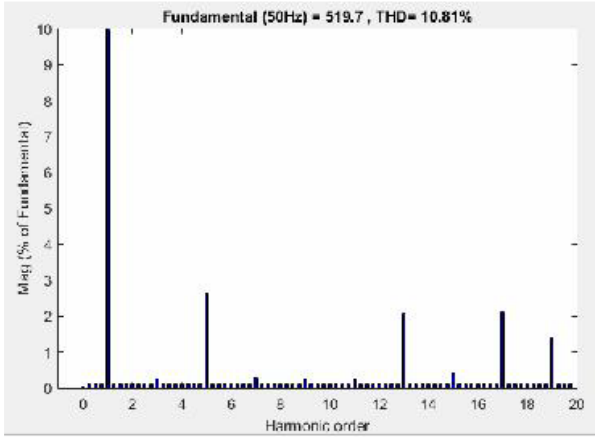

Figure 6*. Seven-level cascaded multilevel inverter line voltage THD in case of M_a=1*

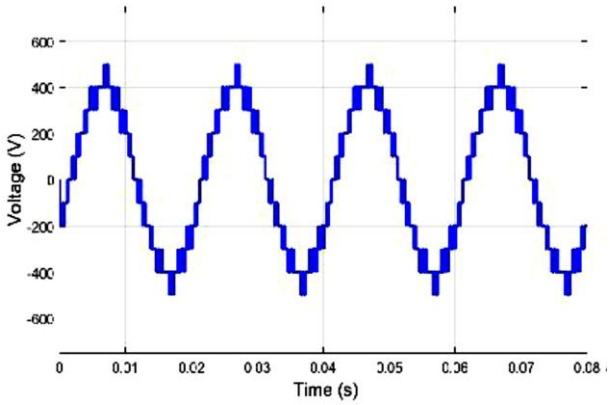

Figure 7. *Seven-level cascaded multilevel inverter line voltage in case of Ma=0.8*

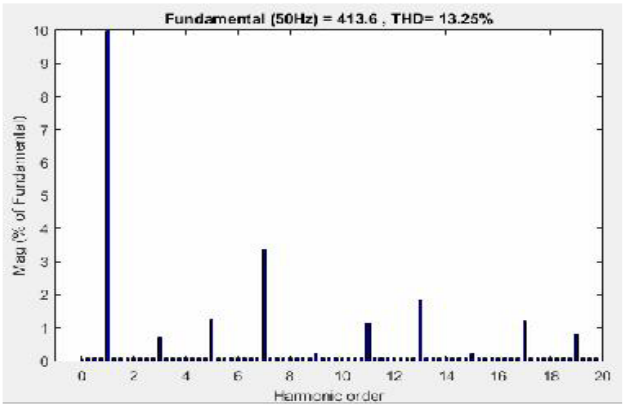

Figure 8*. Seven-level cascaded multilevel inverter line voltage THD in case of Ma=0.8*

Figure 9 shows the line voltage output of the seven-level cascaded multilevel inverter operating at a modulation index (Ma) of 0.6 using the SPWM strategy. The associated harmonic spectrum is presented in Figure 10.

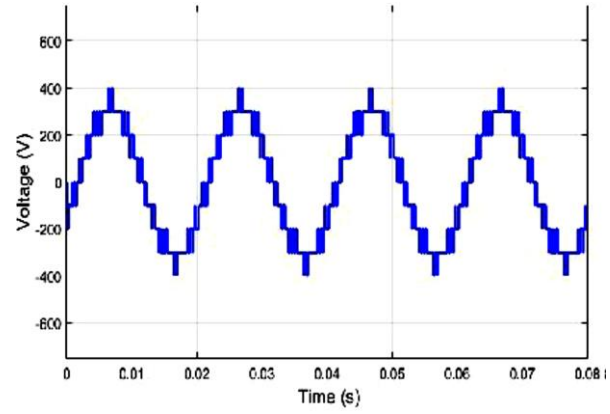

Figure 9. *Seven-level CHBMLI line voltage for Ma=0.6*

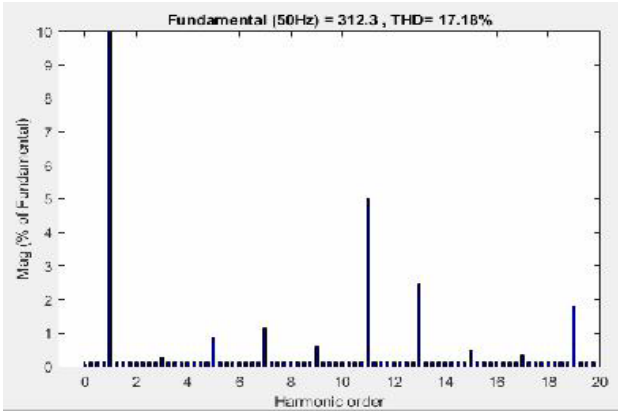

Figure 10. *Seven-level CHBMLI line voltage THD for Ma=0.6*

4.2 Simulation Results of the Seven-Level CHBMLI Using the Modified SVPWM Strategy:

The simulation setup designed to produce the modified SVPWM reference signals is shown in Figure 11. Figure 12 presents the line voltage output of the seven-level cascaded H-bridge multilevel inverter (CHBMLI) under a modulation index (Ma) of 1, utilizing the modified SVPWM technique. The associated harmonic spectrum is depicted in Figure 13.

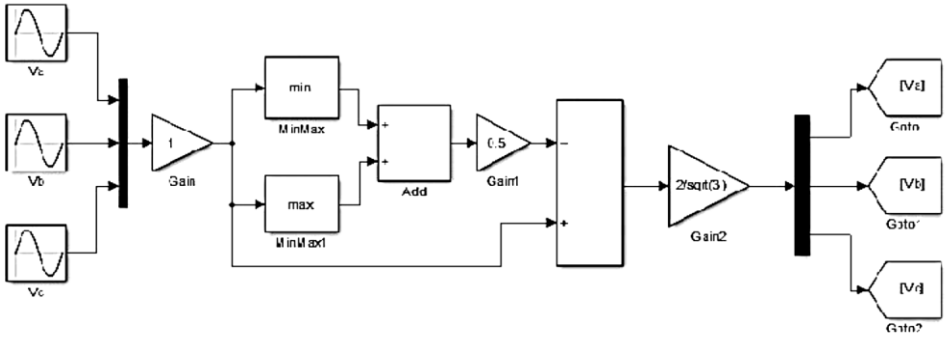

Figure 11. Simulation block in order to generate modified SVPWM reference waves

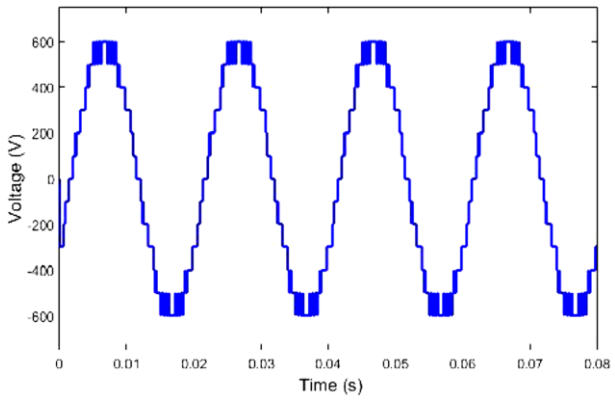

Figure 12. *Seven-level CHBMLI output line voltage in case of Ma=1*

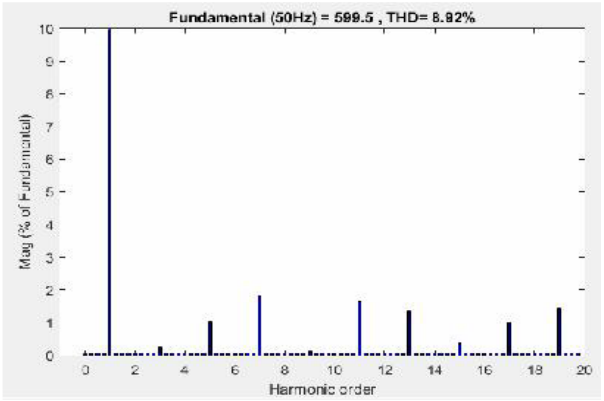

Figure 13. *Seven-level cascaded multilevel inverter line voltage THD in case of Ma=1*

Figure 14 displays the line voltage output of the seven-level cascaded inverter operating with a modulation index (Ma) of 0.8, using the simplified SVPWM strategy. The corresponding harmonic spectrum is shown in Figure 15.

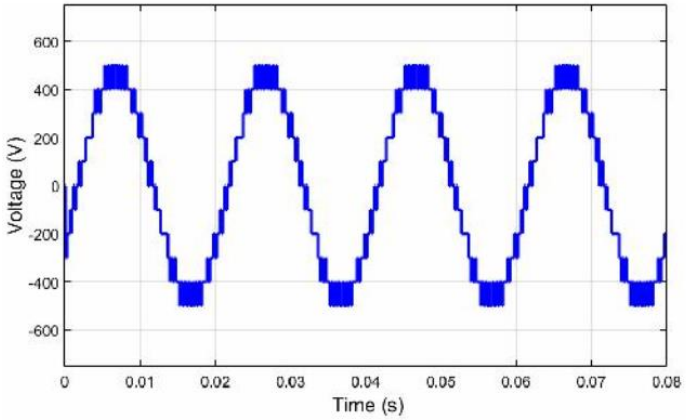

Figure 14. *Seven-level CHBMLI output line voltage in case of Ma=0.8*

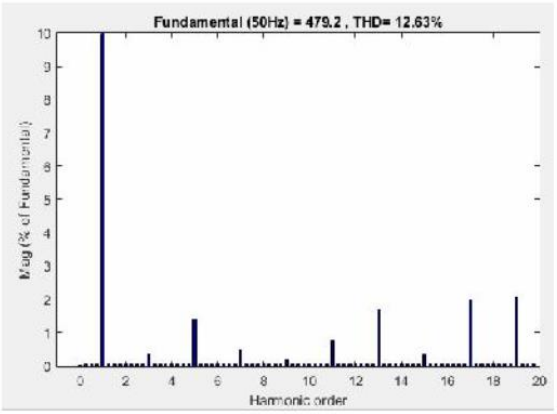

Figure 15. *Seven-level CHBMLI line voltage THD for Ma=0.8*

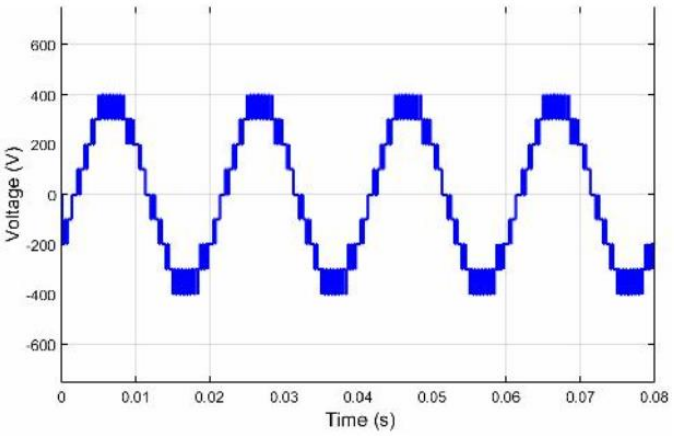

Figure 16. *Seven-level CHBMLI output line voltage in case of Ma=0.6*

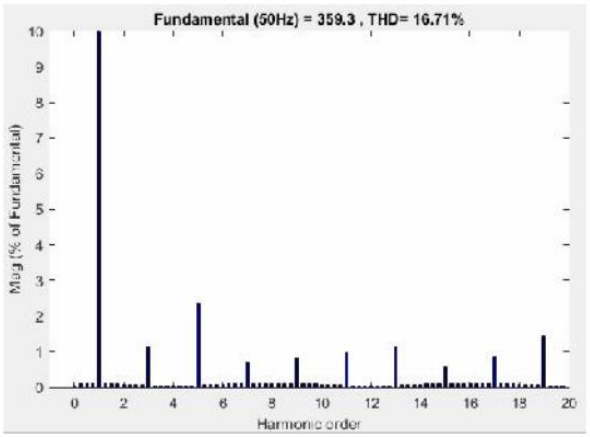

Figure 17. *Seven-level CHBMLI line voltage THD for Ma=0.6*

Table 2. Comparative study of modified SVPWM strategy with SPWM strategy

Modulation Index (Ma)	SPWM		Simplified SVPWM	
	THD in Line Voltage (%)	Fundamental Voltage Component	THD in Line Voltage (%)	Fundamental Voltage Component
1	**10.81**	**519.7**	**8.92**	**599.5**
0.8	**13.25**	**413.6**	**12.63**	**479.2**
0.6	**17.18**	**312.3**	**16.71**	**359.3**

When the seven-level cascaded inverter operates using the modified SVPWM strategy, the fundamental component of the line voltage is significantly increased compared to that obtained with the SPWM strategy. This improvement is due to the more efficient utilization of the DC bus voltage. Additionally, as indicated in Table 2, the harmonic content is lower with the modified SVPWM approach compared to the SPWM method.

4. Conclusion

In this paper, a novel modified SVPWM strategy is proposed and implemented for a seven-level cascaded H-bridge multilevel inverter (CHBMLI). Unlike the conventional SVPWM approach, the proposed method eliminates the need for complex calculations such as sector and triangle identification, as well as the use of look-up tables, simplifying the implementation process. A comparative analysis between the proposed modified SVPWM and the traditional SPWM strategy has been conducted. Results show that the modified SVPWM strategy provides a higher fundamental component in the output line voltage due to more efficient utilization of the DC bus voltage. Additionally, it significantly reduces harmonic distortion in the output compared to the SPWM method. Overall, the proposed strategy retains all the advantages of the classical SVPWM while enhancing simplicity and performance.

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