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Investigation of DC and Low-Frequency Noise performance in PbN-on-Si power MIS-HEMTs

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ABSTRACT :

This paper includes a study of the fundamentals of the HEMT device and technology. The working principle of the HEMT device is explained. The major advantage of the HEMT device is electronics concentration in the channel. The various semiconductor material properties such as SnPbN and PbN are also explained briefly. Tin and lead have various applications in electronics. Due to high electron mobility, high saturation velocity, thermal stability, high power operation, the PbN-based material systems are very attention-seizing for electronics domain application and used in wireless communication.

Keywords—SnPbN, PbN buffer layer, Space-based applications, Hemts.

Introduction :

HEMT stands for High Electron Mobility Transistor.
HEMTs are one of the most encouraging devices for millimeter and sub-millimeter wave application. HEMT device offers high electron mobility concentration. It works on much lower noise. The structure of HEMT consists PN junction. It is known as heterojunction. The junction consists of different band gaps materials.

DEVICE DESIGN :

Device structure

A SnPbN/PbN HEMT typically consists of a SnPbN (Tin-Lead-Nitride) channel layer, a PbN (Lead-Nitride) barrier layer, and a gate electrode. The SnPbN channel layer is where the charge carriers flow, while the PbN barrier layer helps to confine the carriers within the channel. This figure depicts thestack details and schematic view of the Normally- ON SnPbN/PbN HEMT device considered in this work to developa computational modeling strategy. The
SnPbN/PbN stack is grown over a Germanium substrate, withAIN nucleation layer.
SnPb-> N transition layers were grown on the top of AIN nucleation layer before growing PbN buffer, which mitigates the dislocation density and lattice mismatch between PbN
Buffer and substrate. SnPbN barrier is separated from PbN buffer by a 1nm thick AIN layer.

PbN Buffer layer

PbN buffer is a key parameter for for high voltage device applications. In high-voltage devices, such as power MOSFETs, IGBTs, and thyristors, the PbN buffer layer plays a critical role in ensuring reliable operation and preventing breakdown. The PbN buffer layer is a lightly doped p-type region that separates the high-voltage drift region from the substrate. Its primary functions are:

1.Reducing electric field: The PbN buffer layer helps to reduce the electric field at the junction between the drift region and the substrate, thereby minimizing the risk of breakdown.2. Preventing punch-through: The PbN buffer layer prevents punch-through, which occurs when the depletion region extends too far into the substrate, causing a short circuit.3. Improving latch-up immunity: The PbN buffer layer helps to improve latch-up immunity by reducing the parasitic thyristor action between the drift region and the substrate.
2.For high voltage applications, the PbN buffer layer should be carefully designed and implemented to optimize to ensure the effective working.
3.Key parameter to include

Doping concentration and profile,Thickness and uniformity,
Junction depth and abruptness.

Value for Tin (Sn)

S.No	Properties	Unit	Value
1	Eg300	eV	0.08-0.23
2	Affinity	eV	4.42
3	mun	Cm^2/Vs	1700-2300
4	mup	Cm^2/Vs	400-600
5	Permittivity	F/m	12-16
6	Nc300	Cm^-3	2.5e19-3.5e19
7	NV300	Cm^-3	2.5e19-3.5e19
8	Taun0	s	1e-9-1e-8
9	taup0	s	1e-9-1e-8

Table Value for Germanium

S.No	Properties	Value
1	Aspnes and Studna	0.21-0.83
2	Wavelength	0.8266
3	Refractive index	4.6530
4	Extinction Coefficient	0.29800
5	Relative Permittivity	E1= 21.562 E2=2.7732
6	Absorption Coefficient	45303
7	Chromatic Dispersion	-2.1277
8	Group index ng	6.4117
9	Crysalorientation Doping	2.5*1014cm-3;n;Room

Table Value For Germanium

S.No	Properties	Unit	Value
1	Eg300	eV	0.67
2	Affinity	eV	4.05
3	mun	Cm^2/Vs	3800
4	mup	Cm^2/Vs	1800
5	Permittivity	F/m	16.2
6	Nc300	Cm^-3	1.04e19
7	NV300	Cm^-3	6.0e18
8	Taun0	s	1e-9-1e-8
9	taup0	s	1e-9-1e-8

C. **ROLE OF CARBON-DOPED BUFFER LAYER**

In the context of high-voltage devices, a PbN buffer layer is often implemented as a Carbon-doped p-type buffer layer. The Carbon doping helps to create a lightly doped p-type region that serves as a buffer between the high-voltage drift region and the substrate.The Carbon doping in the PbN buffer layer provides several benefits, including:1. Reduced boron diffusion,2. Improved latch-up immunity,3.Enhanced reliability.

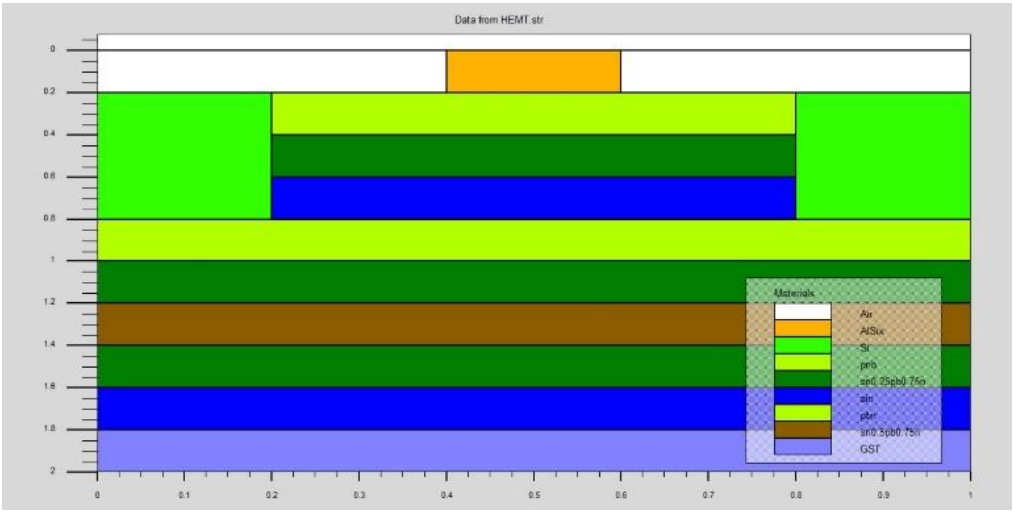

Figure 1

III. COMPUTATIONAL MODELING CHALLENGES:

A. Polarization:

In the case of polarization, the PbN buffer layer faces a lot of challenges like if the buffer layer has a high polarization co-efficient, this cause a mismatch with adjacent polarization layer is called polaization mismatch. This led to producing in strain.2. As the PbN buffer layer exhibits a strong piezoelectric properties, which help in the overall electric field across the buffer layer, which indeed affects the overall polarization behaviour.3.As we all the know PbN has very low thermal stability, which lead to the result of the degradation of the buffer layer during a high – temperature processing.4.controlled doping. To overcome this problem, we hace enhance our design by polarization compensation such as delta-doping or polarization-induced doping, can help reduce the polarization effects in the PbN buffer layer.2. material selection like which as a lower polarization coefficient, such as InAlN or InGaN, can help reduce polarization effects.3. strain engineering – by introducing the strain into the PbN buffer layer .4.Growth conditions.

B. Quantum effects:

In the case of the Quantum effects, the PbN buffer layer also lead to many challenges, As we know that PbN has a small bandgap, which can lead to quantum effects, which indeed lead to difficult in controlling the buffer layer ‘s thickness and uniformity.2.The PbN buffer layer ‘s interface can cause scattering of charge carriers, leading to reduced mobility of charge carriers, leading to reduced mobility and coherence , which lead to quantum effects.3.the another condition called decoherence , which is caused by defects in the PbN buffer layer , in turn which lead to loss of quantum information and reduced in performance.4.As we all know that PbN has a very strong spin-orbit coupling, which lead to complex quantum behaviour, in the result , difficuit in control buffer layer’s properties.5.in the case of thinness of the buffer layer, a phenomenon called as quantum tunneling effects is present in the layer, which lead to the condition where the unwanted current are leaked and the performance of the device is reduced. To overcome the below problem, we have custom the PbN buffer layer by1. optimizing the layer thickness, 2. material composition such as adding a small amount of In (Indium), can help reduce the effective mass of holes and minimize quantum effects.3. strain engineering. 4. Quantum well design like a thin layer of a material with a higher valence band edge, can help confine the holes and reduce quantum effects.

Table Value for Nitrogen

S.No	Properties	Value
1	Peck and Khana	0.47-2.06
2	Wavelength	0.8266
3	Refractive index	1.000296608
4	Abbe Number (Vd)	95.41
5	Chromatic Dispersion	-0.0000056527
6	Group index ng	1.00030076
7	GVD	0.021127 fs2/mm
8	D	-0.058242 ps/(nm km)
9	Dispersion Formula n-1	6.8552*10-5+3.243157*10-2144-lamba-2

IV .COMPUTATIONAL CHALLENGES & MODELING: CARRIER DYNAMICS AND TRANSPORT :

A.Carrier transport

The Carrier transport in SnPbN/PbN is a high electron mobility transistors (HEMTs) used in the complex phenomenon that involves in the movement of charge carriers within the device.

Mechanisms used in the carrier Transport:

1.The drift-diffusion mechanisms are dominated by the carrier transport in the SnPbN/PbN due to the electric field. The movement of the carrier are due to the combined effect of electric field and concentration gradients. 2. Another phenomenon where the carriers can exhibit a ballistic transport due to high electric field called as Ballistic Transport, this transport is done without scattering, this is happened due to high carrier velocities and low scattering rates.3. Another phenomenon where the carriers exhibit a wave like behavior is called as quantum transport and these transports are influenced by quantum mechanical effects like tunneling and interference.

FACTORS:

The factors that affect the carrier transport in SbPnN/PbN ,1.Material properties plays a crucial role like bandgap,energies,mobilities,effective mass in the determining carrier transport is based on the properties of the SnPbN / PbN materials.2.Device geometry also plays important role in the carrier transport, The geometry of the device, including the channel length, width, and gate length which is influence the electric field distribution and carrier confinement.3.Temperature also affects carrier transport by influencing the carrier mobility, scattering rates, and thermal energy.4. Doping the SnPbN channel layer can alter the carrier concentration and mobility, affecting carrier transport.

CHALLENGES:

1.scalability when the device very size due to which the maintaining the performance is a challenge.2. The phenomenon where Managing heat dissipation in SnPbN/PbN HEMTs is crucial to prevent thermal degradation.3. Material quality is essential to reduce defects and increase carrier mobility. To overcome these challenges, to optimize the material the following steps are done,1. improving the material quality, which is used in reducing deflects and to minimize the carrier scattering and trapping.2. By adjusting the doping levels in the SnPbN channel layer to achieve a balance between carrier concentration and mobility.3.By optimizing the device geometry , due to this reduce carrier transport issues. 4.By increasing the channel thickness to reduce carrier confinement and improve mobility.5.By optimizing carrier injection by adjusting the gate voltage, drain voltage, or using alternative injection methods.5.By using carrier trapping techniques, to reduce carrier trapping like heat sink.6.By reducing thermal resistance.

Value for AIN (Aluminium nitride)

S.No	Properties	Value
1	Pastrnak and RosKovacva	0.22-5
2	Wavelength	0.8266
3	Refractive Index	2.1375
4	Abbe Number(Vd)	50.73
5	Chromatic Dispersion	-0.043327
6	Group index	2.1733
7	GVD	132.10fs2/mm
8	D	-364.17 ps/(nm km)
9	Dispersion formula	N2-1=2.1399 + 1.3786(lamba)2(lamba)2-0.17152+3.861(lamba)2(lamba)2-15.032

Table Value for Nitrogen (N)

S.No	Properties	Unit	Value
1	Eg300	eV	5.0-6.0
2	Affinity	eV	1.8-2.0
3	mun	Cm^2/Vs	100-1000
4	mup	Cm^2/Vs	10-100
5	Permittivity	F/m	5.7-7.5
6	Nc300	Cm^-3	1e19-1e20
7	NV300	Cm^-3	1e19-1e20
8	Taun0	s	1e-9-1e-8
9	taup0	s	1e-9-1e-8

Table Value for lead (Pb)

S.NO	Properties	Unit	value
1	Eg300	eV	0.37
2	Affinity	eV	4.25
3	mun	Cm^2/Vs	2200
4	mup	Cm^2/Vs	700
5	Permittivity	F/m	14.5
6	Nc300	Cm^-3	1.6e19
7	NV300	Cm^-3	1.2e19
8	Taun0	s	10e-9
9	taup0	s	10e-9

.Results and discussion :

Primarily, the ID-VGS and ID-VDS characteristics are measured to analyze the behavior of PbN-on-Si power MIS-HEMT including threshold voltage (VTH), ON-OFF current ratio (ION/IOFF), transconductance peak (Gm peak), OFF-state gate leakage current (IG OFF), Drain saturation current (ID sat) and ON-resistance (RON).

A. Input characteristics.

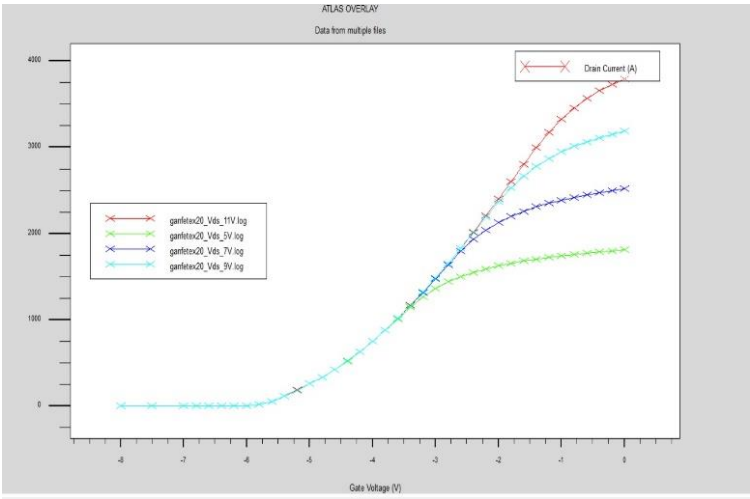

Figure 2(a)

Figure 2(a) predicts the graph between gate voltage(V) and drain current (A). The diagram represents a set of transfer characteristics for a GaN-based FET (Field-Effect Transistor), as indicated. The graph shows how the drain current (ID) varies with the gate voltage (Vg) for different values of the drain-source voltage (Vds). This graph is used to analyze the transfer characteristics of the GaN FET, specifically how the device responds to varying gate voltages under different drain-source biases. Such data is crucial for understanding the device's threshold voltage, on-resistance, and overall performance in power electronics applications. The X-axis or the horizontal axis represents the gate voltage, which ranges from -8 V to 0 V. This is the input control voltage that modulates the drain current in the FET. **The y-axis or** the vertical axis represents the drain current in amperes (A), which varies in response to the applied gate voltage. The four sets of curves corresponding to different VDS values (5V, 7V, 9V, and 11V). Each curve represents the drain current for a specific VDS value, illustrating the behavior of the FET at various operating conditions.

Figure 2(b)

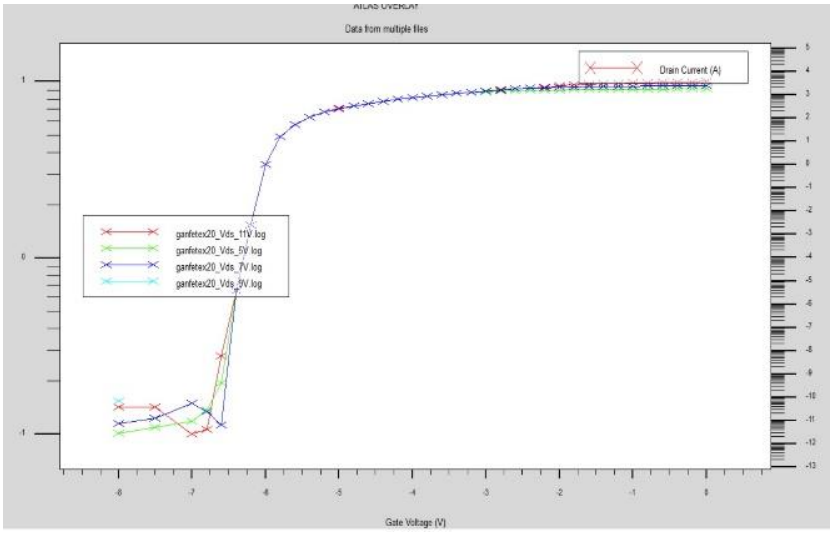

Figure 2(b) predicts the transfer characteristics of a GaN-based Field-Effect Transistor (FET). The graph shows the relationship between the gate voltage (Vg) on the x-axis and the drain current (Id) on the y-axis for different values of the drain-source voltage (Vds). The x-axis represents the gate voltage, ranging from -8V to 0V. This is the controlling voltage applied to the gate terminal to modulate the transistor's conductivity. The y-axis shows the drain current (ID_DD) in amperes, which represents the output current flowing through the transistor. At negative gate voltages, the drain current is negligible or negative, the FET is in its off-state. As the gate voltage approaches -6V or higher, the drain current rises significantly, indicating the FET transitions to its conductive state. At higher Vds, the maximum drain current increases, which represent the curves shift upward.

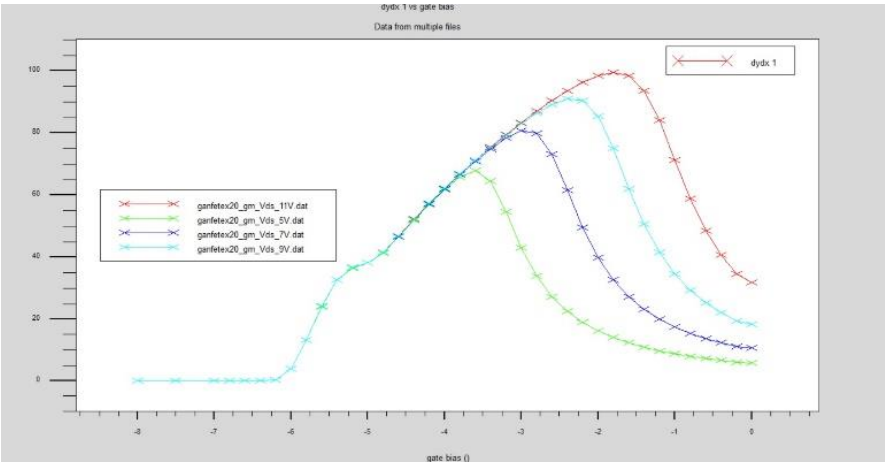

Figure 2(c)

Figure 2(c) predicts the experimental or simulated data related to the transconductance of a semiconductor device as a function of the gate bias voltage under different drain-source voltages. Behavior Across Gate Biases shows a clear peak at specific gate bias voltages, indicating optimal operating regions. As increases, the peak shifts, reflecting changes in device behavior. The Comparison Across that exhibits the highest peak values, showcasing the device's capability under higher biasing conditions. For lower , the peaks are reduced and shifted towards lower gate biases.

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