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Design and Implementation of Low Dropout Voltage Regulator with PSRR and Low Power Dissipation

Mohit Nayak[1] and Laxmi Singh[2]

[1] PhD. Scholar, Department of Electronics & Communication Engineering, Rabindranath Tagore University (RNTU), Bhopal
[2] Professor, Department of Electronics & Communication Engineering, Rabindranath Tagore University (RNTU) , Bhopal
mohilnayakl788@gmail.com, 15olaxmisingh@gmail.com
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ABSTRACT—

This brief presents an approach to utilize of sliding-mode (SM) controller in digital low-dropout/linear regulators. Various design aspects, including the extraction of the regulator state-space model and sliding coefficients by considering the hitting, existence, and stability conditions are described. Moreover, the freeze control block is introduced as a solution to compensate for the high frequency chattering phenomenon of SM, resulting in reduction of switching losses. In order to verify the statements, a quasi digital low-dropout/linear regulator is implemented in a discrete form on a PCB. The circuit consists of the proposed current-mode current feedback amplifier-based SM controller and switched-mode pMOS array driven by a bidirectional serial shift register, which is controlled by the SM controller. The results reveal that the controller detects the load changes rapidly, and eliminates the output limit-cycle oscillation, providing a robust and stable output voltage.

Index Terms—Digital LDO, linear regulator, low-dropout, PSRR, power dissipation.

I Introduction

Low Dropout Voltage Regulator

LDOS is a linear regulator with much less voltage difference between the input and output in order to properly adjust the input voltage. In Figure 1, you can see the classic topology of the LDO regulator. It consists of path elements, error amplifiers, and resistance feedback networks. The feedback network includes resistive voltage division that provides a scaled output voltage that corresponds to the reference voltage when the output is on the nominal voltage. The error amplifier always compares the reference voltage with the voltage feeding from the voltage divider. This difference is reinforced, and the output of the error amplifier drives the output voltage level to the desired value by which the passing element drives the output voltage level.

In the figure 1 we can identify following building blocks:

The Voltage Reference

The voltage reference is the starting point of all regulators to determine the operating point of the error amplifier. In most cases, this voltage reference from band grape types provides the opportunity to work with low supply stress, so accuracy and stability at different temperatures are sufficient for the construction of linear regulators. The key parameters of voltage reference are the initial noise and contribution to the total PSRR of the error amplifier. These effects can be minimized by adding passive component filters such as RC filters.

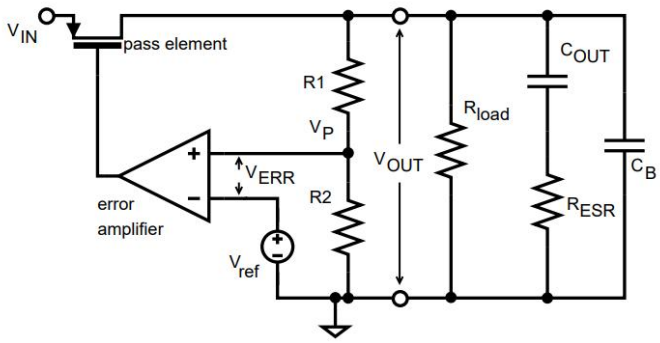

Figure 1: Basic linear voltage regulator

The Error Amplifier

Design amplifier designs should be kept as simple as possible, so as not to draw too much electricity. The lower the electricity, the less electricity is drawn from the input, and the overall current is lower. Even if you try to keep your resting stream as low as possible, there is a compromise between electrical distortion and the performance of the error amplifier (bandwidth, slew rate, etc.). The gate capacitance of passing is very large, so the output resistance of the error amplifier should be as low as possible to ensure system stability. DC open loop reinforcements must be high under all load conditions to ensure output accuracy. The amplifier range must be large enough to respond quickly when changing load conditions and input voltage. The initial voltage swing of the amplifier is also important. This means that the error amplifier is driven near one of the supply rails depending on the type of pass device, as the pass device needs to be turned off with a low load flow.

Error amplifier takes the voltage scaled down by the voltage divider composed of resistors R1 and R2

" VP = VOUT R1/(R1 + R2)"

compares it with the reference voltage and adjusts the resistance of the pass element to drive the error signal

" (VERR = VP − VREF)"

as close to zero as possible.

If we set

"VREF = VP" the we get VOUT as:

$$v_{out} = \left(1 + \frac{r_2}{r_1}\right) \times v_{ref} \ldots\ldots\ldots\ldots 1$$

LDO Parameters In this section, basic steady state and transient parameters of LDO regulators will be presented.

II Dropout Voltage Regulators

Voltage represents the differential voltage between the input and output nodes of the voltage controller, and is listed by the circuit to adjust itself to further decrease in the input voltage. This occurs when the input voltage of the output voltage approaches from above. In order for the controller to maintain sensitivity to change the output voltage, the transistor is usually designed to remain in high-enhanced mode (saturation), and the input voltage VIN defines the amount of headroom for the transistor. A drop in VIN reduces the dynamic voltage range of the transistor, which operates in a feedback loop to control the output voltage. If one or more transistors drop from saturation to the triple, the system reinforcement and output voltage "Vout" will deviate from the output voltage V specified in the drop area. The control's conductivity is missing, making it behave very poorly like a switch. Therefore, the output voltage Vout is the difference between the input voltage and the ohm drop of the pass device.

$$v_{out,drop} = v_{in} - v_{pass}$$

$$= v_{in} - i_{pass} r_{pass}$$

$$= v_{in} - v_{do} \ldots\ldots\ldots\ldots\ldots 2$$

Quiescent Current

The difference between input and output flows is rest or soil. In particular, low power supply systems, small flows of peace are required to maximize efficiency.

Efficiency

The efficiency of an LDO controller is limited by the input to the quiescent current and output voltage, as described in the equation below:

$\eta = \frac{i_0 v_0}{(i_0+i_q)v_i} \times 100\%$.....3

High efficiency can be achieved by minimizing dropout voltage and resting current. The voltage difference between the input and output must be minimal to keep the power supply low

$$power\ dissipation = (v_i - v_0)i_0$$

The input to the output voltage difference is a defining factor that determines performance efficiency regardless of load conditions.

Transient Response

Transient responses are defined as the maximum output voltage variation in the load current step or input voltage step. This is a function of the output capacitor and its equivalent series resistor (ESR) and can be further improved bypass capacitors if necessary. The equation for maximum voltage fluctuation at the output is defined as follows:

$\Delta v_{tr,max} = \frac{i_{0,max}}{c_0+c_b}\Delta t_1 + \Delta v_{esr}$.....4

Where

Δt1 is defined by the closed loop bandwidth of an LDO regulator.

ΔVESR is the voltage variation resulting from the presence of the ESR (RESR) of the output capacitor.

The value of maximum output voltage transient is determined by the application.

III. Result and Analysis

Line control is a parameter that defines the controller's ability to maintain the desired output voltage at different input voltages.

It is defined as:

$line\ regulation = \frac{\Delta v_0}{\Delta v_i}$ 5

Where

AP ASS is the gain of the pass device,

β is the feedback factor and

AEA is the gain if the error amplifier.

Line regulations improve with open grinding profits, but THA must be considered as increased profits can affect stability. Line payments are proportional to open loop gain, but they essentially reject power sources directly at current frequencies.

LDO regulators respond to major temporary steps. As the input voltage increases, the output voltage fluctuations also increase. Because line control is a parameter of hospitalization status (measured after transients), it can be measured as the variance of output voltage when the input voltage is changed.

Power Supply Rejection

Power resignation (PSRR), also known as ripple, is the ability of the controller to prevent fluctuations in the regulated output voltage caused by the incoming voltage fluctuations. The PSRR equation is the same as the line regulation, but the entire frequency spectrum is taken into account. The PSRR is defined by a control loop. The low ESR value of the output capacitor is the large capacity, which improves the power supply ratio.

$$PSRR(\omega) = 20.\log_{10}\frac{A(\omega)}{A_{supply}(\omega)}dB$$

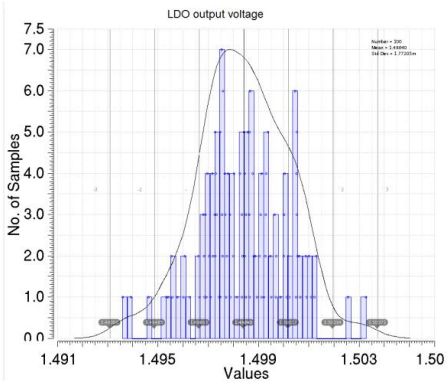

Figure 2:Distribution of the output voltage from monte carlo simulation

The simulations had three sigma variations with output voltages below 5 mV. The results of the Monte Carlo simulation can be found in Figure 2 below. The gate area of the device is enlarged, which minimizes the threshold voltage deficiency (highest) (highest) (highest) and is minimized based on the Pelgrom model [3]

Table 1: circuit devices sizes

Device	W/Lμm
M_1M_2	2.21/1
M_3	1/21
M_4	11.(1/20)
M_5M_6	3/3
M_7M_8	3/3
M_9M_{10}	2/5
$M_{11}M_{13}$	3/3
M_{12}	10/0.6
M_{PASS}	10/0.18

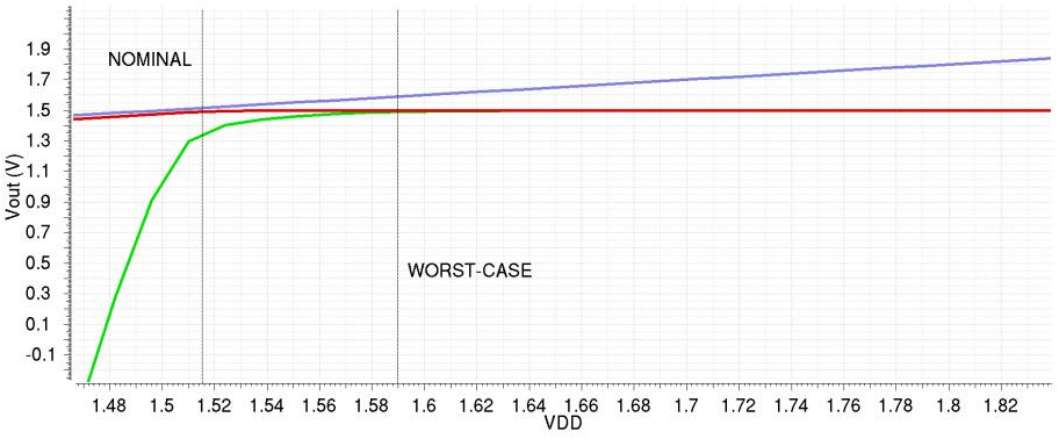

Figure 3: Input voltage sweep - dropout and regulation region

The dropout voltage was measured as the output voltage drops from its nominal value of 1.5 V and the maximum load current of 1.1 mA and the input voltage measured at the nominal corner.

In Figure 4, we can see how the controller is not controlled when the input voltage drops below 1.57 V, the pass transistor starts operating in the TRIDAREA and the system starts to lose its reinforcement. Therefore, the feedback loop cannot hold the starting value exactly as accurately as before.

Line regulations define how the outcome behaves with built-in slow changes. Essentially, it is a constant direct current supply of the controller. Cleaning up tension at the entrance allows you to observe the values that change in the output and calculate how much the outcome has changed in relation to the exit. Figure 5 shows line restrictions for nominal and worst corners. As expected, the worst corners are the lowest preload current and the largest output capacitor, leading to a drop in reinforcement proportional to line regulation.

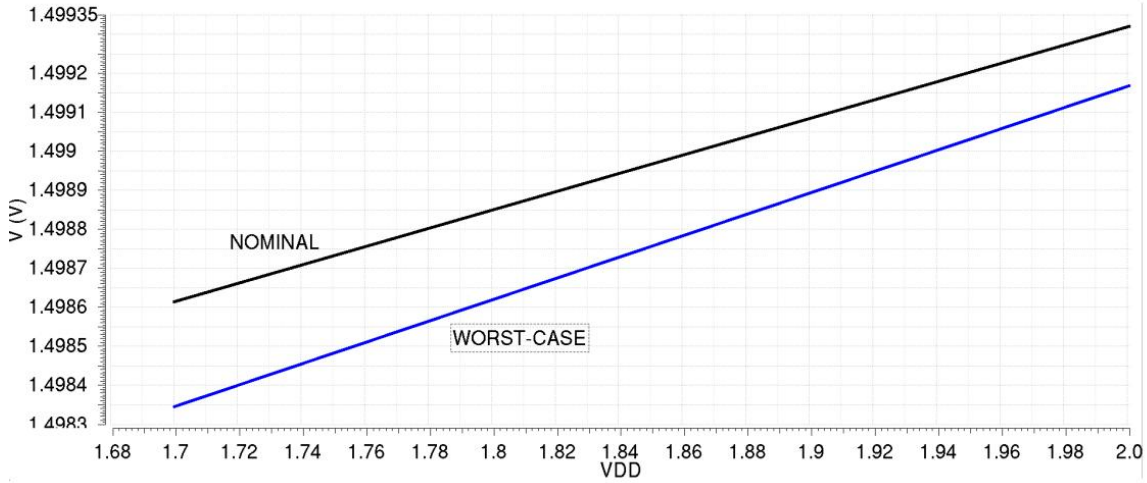

Fig.5:Graph of line regulation

Load Regulation

Another parameter of hospitalization status is load adjustment. The loop gain is ultimately, so the controller cannot cancel the effect of changing the load current completely. Load control is performed in Figure 6.

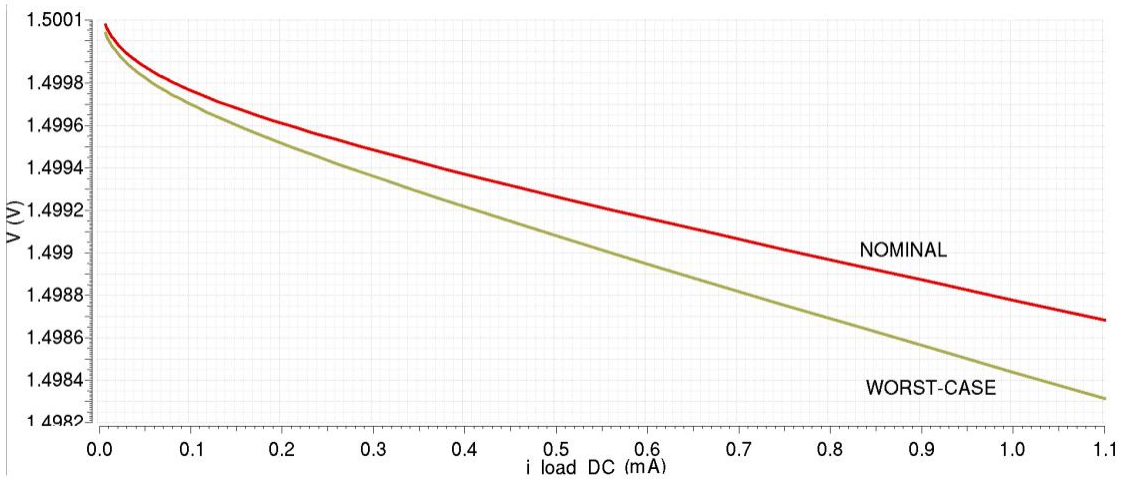

Figure 6: Load regulation for nominal and worst corner

IV. Conclusion

This work presents the design of the LDO controller to satisfy the defined parameters. Several parameters were considered during the design, but the main focus was the quiescent current, designated as less than 10μA. First, we discussed how typical parameters of LDO regulatory authorities are interpreted and how to measure them. The most important task when designing an LDO voltage controller is to maintain stability under all load conditions. PMOS passports have been selected as the best option for applications from load currents and fault voltages. Because passersby is a large load, an operational transductance amplifier was used as an error. The symmetric OTA topology was chosen for a wide range of output swings due to the significant changes in tension in the resulting change in load conditions.

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