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TRAFFIC LIGHT CONTROLLER USING VERILOG

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ABSTRACT:

This project presents the design, implementation, and comparison of traffic light controllers for both T-shaped and four-way intersections using Verilog HDL. The objective is to create an efficient and reliable signal control system that improves traffic flow and enhances road safety. Finite State Machines (FSMs) are used to model the signal phases, ensuring precise transitions between Red, Yellow, and Green lights for each intersection type. Separate controllers are developed for the T-junction and the four-way intersection based on their unique traffic patterns and movement priorities. These controllers are then integrated into a unified module capable of handling both intersection configurations. A comparative study is conducted to analyze differences in design complexity, number of states, timing requirements, and vehicle throughput. The analysis shows that four-way intersections demand more states, longer cycles, and higher synchronization, whereas T-shaped intersections are simpler and more efficient for low-to-moderate traffic. Simulation results verify the correct functioning, timing accuracy, and safety constraints of both systems. The project demonstrates the effectiveness of Verilog-based digital design for intelligent traffic management and provides insights useful for smart-city applications

1. INTRODUCTION

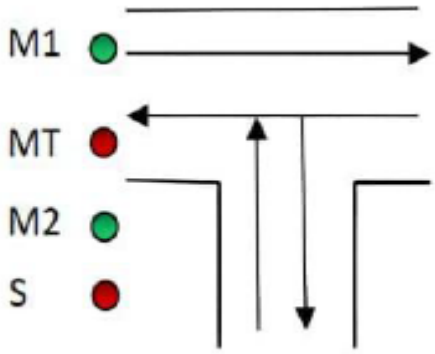
Traffic congestion has become a serious problem in modern urban areas due to the rapid increase in the number of vehicles, making efficient traffic control systems very important. In this project, a Traffic Light Controller is designed using Verilog HDL to automatically control traffic signals and ensure smooth vehicle movement. The main focus of this project is to compare the performance of a T-shaped intersection and a Four-way intersection by analyzing their on-chip power consumption and FPGA resource utilization. Both traffic models are implemented, simulated, and analyzed using Xilinx Vivado software, which is widely used for digital design, synthesis, and power analysis. This comparative study helps in identifying the most efficient and optimized traffic control design suitable for real-time traffic applications.

2. LITERATURE SURVEY

Traffic control systems have evolved significantly with the rapid growth of urbanization, population, and vehicle density, making efficient traffic management essential to reduce congestion, waiting time, and accidents. Early traffic light controllers were mechanical and relay-based systems with fixed timing, which lacked flexibility and required regular maintenance. This was followed by analog timer-based controllers using devices like 555 timers and counters; although more stable, they still suffered from timing drift and limited scalability. With the advancement of embedded systems, microcontroller-based traffic light controllers using devices such as 8051, PIC, and ARM became popular due to their programmability and improved accuracy, but their sequential execution limited performance for complex intersections. To overcome these limitations, FPGA-based traffic controllers using Verilog and VHDL were introduced, offering true parallel processing, high speed, low latency, and reliable real-time performance. Several studies have demonstrated that FSM-based traffic controllers implemented on FPGA efficiently handle multi-road intersections, adaptive timing, emergency vehicle detection, and density-based prioritization. Research also shows that while T-shaped intersections require fewer FSM states, logic resources, and consume lower power, Four-way intersections demand more hardware and exhibit higher dynamic power due to increased switching activity. Simulation, power analysis, and resource utilization using tools such as Xilinx Vivado play a vital role in verifying correctness and optimizing hardware efficiency. However, only limited research has directly compared T-shaped and Four-way intersections in terms of on-chip power and FPGA resource utilization, which forms the key motivation for the present work.

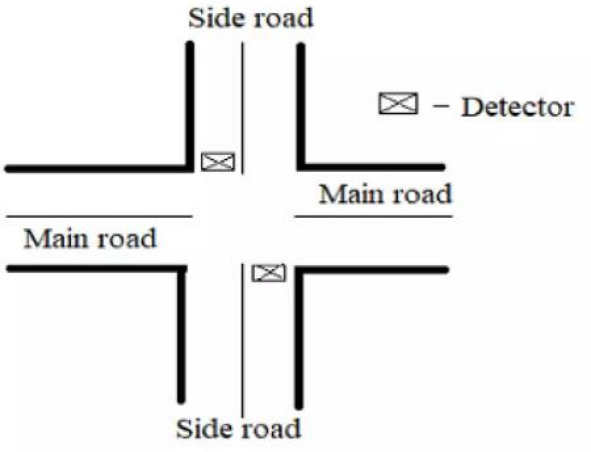
3. METHODOLOGY

T-Shaped Intersection Traffic Light Controller



In the T-shaped intersection model, the traffic light controller is designed using a structured finite state machine (FSM) that manages the right-of-way between the major straight road and the side road junction. The methodology begins with defining traffic phases that ensure safe and conflict-free movement for vehicles approaching from three directions. The major road is given priority by assigning longer green intervals, while the side road receives regulated green time based on predetermined timing logic. Each state in the FSM represents a specific combination of light outputs—Green, Yellow, and Red—for the three arms of the intersection. A central timer module controls state transitions, ensuring smooth switching between major-road green, major-road yellow, side-road green, and side-road yellow phases. The design also integrates pedestrian crossing logic where required, with dedicated timing for walk and wait intervals. Verilog HDL is used to implement the FSM, counters, and control logic, enabling cycle-accurate simulation in Xilinx Vivado. Synthesis verifies hardware feasibility and resource efficiency. This methodology allows accurate modelling of real-world T-junction behaviour and provides a basis for comparing performance, timing, and resource utilization with the four-way intersection controller developed in the same project.

Four-Way Intersection Traffic Light Controller



For the four-way intersection, the methodology focuses on developing a coordinated traffic light controller that manages vehicle flow across all four directions: North, South, East, and West. A finite state machine (FSM) is designed to generate safe and sequential traffic phases, ensuring that only non-conflicting directions receive the green signal at any given time. The controller operates in a cyclical pattern where the North–South direction receives priority green time followed by a controlled yellow interval, after which the right-of-way shifts to the East–West direction using a similar green and yellow timing structure. Dedicated timer and counter modules regulate the duration of each phase to maintain consistent traffic movement and minimize waiting time. Pedestrian crossing logic is incorporated as an optional component and is synchronized with the vehicular states to prevent unsafe overlaps. The entire design is implemented in Verilog HDL, enabling modular construction of FSMs, multiplexers, and timing units. Functional simulation in Xilinx Vivado validates the correctness of the state transitions, while synthesis provides insights into hardware mapping and resource requirements. This structured methodology allows the four-way intersection controller to closely emulate real urban traffic conditions and serves as a reliable basis for comparing efficiency, performance, and on-chip utilization with the T-shaped intersection controller developed in the project.

4. EXPERIMENT DIAGRAM

T-Shaped Intersection Traffic Light Controller

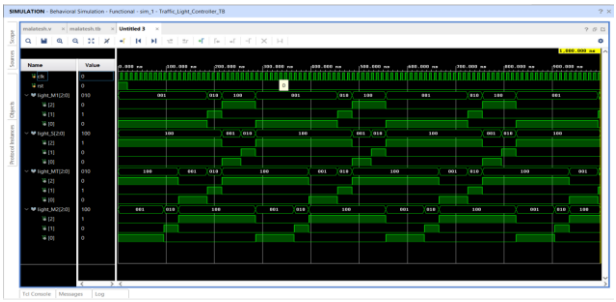


Fig 1: T-Shaped Wave Form

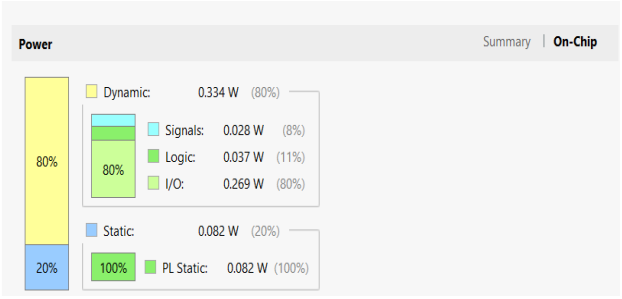
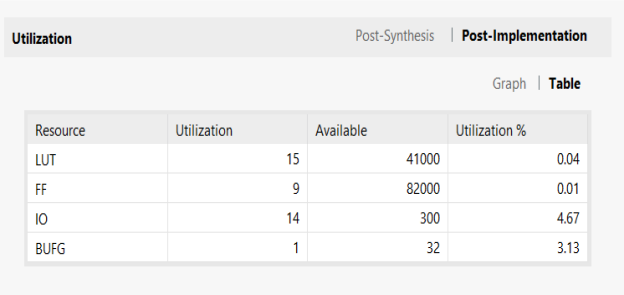


Fig 2: T-Shaped On-chip Power



Resource	Utilization	Available	Utilization %
LUT	15	41000	0.04
FF	9	82000	0.01
IO	14	300	4.67
BUFG	1	32	3.13

Fig 3: T-Shaped Resource Utilization

Four-Way Intersection Traffic Light Controller

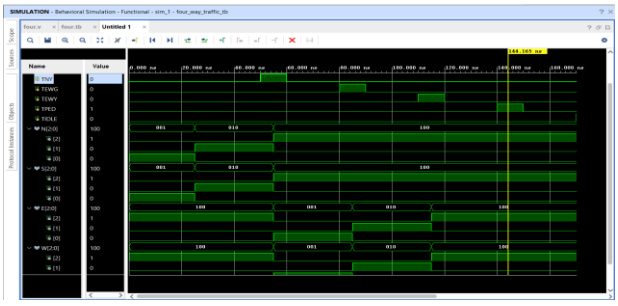


Fig 4: Four Way Wave Form

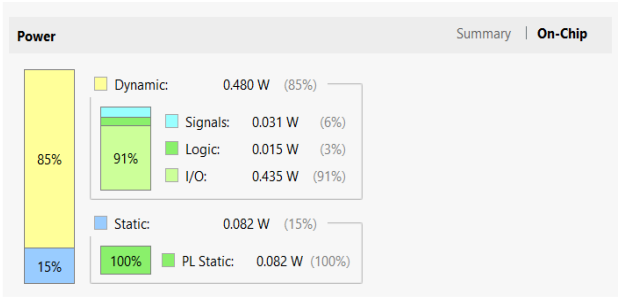


Fig 5: Four Way On-Chip Power

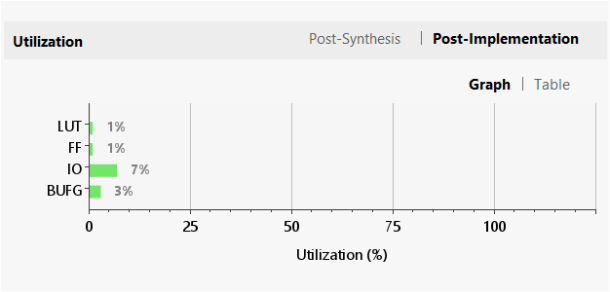


Fig 6: Four-way Resource Utilization

5. ADVANTAGES

- **Low Power Consumption:** The FPGA-based design consumes less on-chip power compared to traditional controllers.
- **High Speed Operation:** Parallel processing in FPGA allows fast and accurate signal switching.
- **Efficient Resource Utilization:** Optimized FSM design reduces LUT and Flip-Flop usage.
- **Easy Modification:** Traffic timings and signal logic can be easily changed by updating the Verilog code.
- **Scalable Design:** The controller can be easily extended to support more intersections or advanced features.
- **Accurate Timing Control:** FPGA provides precise and stable signal timing without drift.
- Real-Time Performance: The system responds instantly to state changes, making it suitable for real-time traffic control.
- **Reliable Operation:** Hardware-based control reduces software errors and increases system reliability.

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