



Efficient Implementation of Multi-Radix DIT FFT Architectures Using Programmable Reversible Logic

Sonam Rajak¹, Dr. Shalini Sahay²

¹M. Tech Scholar, ²Professor

Sagar Institute of Research and Technology (SIRT), Bhopal

ABSTRACT

This paper introduces an efficient and energy-aware implementation of Radix-2, Radix-4, and Radix-8 Decimation-In-Time (DIT) Fast Fourier Transform (FFT) architectures by utilizing programmable reversible logic gates. The proposed approach leverages the concept of logical reversibility to mitigate information loss during computation, thereby significantly reducing power dissipation and thermal effects. By constructing programmable reversible butterfly structures and twiddle factor multipliers, the design achieves reconfigurability and reduced hardware redundancy. The developed architectures are evaluated based on parameters such as quantum cost, garbage outputs, gate count, delay, and power consumption. FPGA-based implementation in Xilinx Vivado validates the functional accuracy of the proposed models and demonstrates notable improvements in power-delay performance compared to conventional irreversible FFTs.

Keywords: Reversible computation, FFT, DIT algorithm, Radix architecture, Quantum cost, Low-power VLSI

1. Introduction

The Fast Fourier Transform (FFT) remains one of the most crucial algorithms in digital signal processing, enabling efficient computation of the Discrete Fourier Transform (DFT). Its applications span across modern domains such as wireless communication, radar systems, image reconstruction, spectral analysis, and biomedical signal processing. FFT algorithms have drastically reduced computational complexity from $O(N^2)$ to $O(N \log N)$, establishing themselves as indispensable in both software and hardware-based processing environments.

However, most FFT implementations use irreversible logic circuits, which inherently dissipate energy due to the loss of information bits during computation. Landauer's principle (1961) states that erasure of one bit of information leads to an energy dissipation of $kT \ln 2$ joules. Bennett (1973) later established that a logically reversible process, where outputs uniquely map to inputs, can theoretically avoid such energy loss. This principle forms the foundation for reversible logic, a key enabler of energy-efficient and heat-conserving circuits. Reversible logic has gained prominence in emerging technologies such as quantum computing, optical computing, and nanotechnology. Gates like Toffoli, Fredkin, and Peres have demonstrated information-preserving behavior, while programmable reversible gates such as TR and DKG (Thapliyal and Srinivas, 2006) extend functionality for arithmetic operations. Integrating reversible logic in FFT design poses challenges due to the complex arithmetic involved in butterfly operations—addition, subtraction, and multiplication by complex coefficients (twiddle factors). Efficient reversible implementation must maintain bijectivity while minimizing quantum cost, garbage outputs, and constant inputs. The present work focuses on designing programmable reversible FFT architectures for Radix-2, Radix-4, and Radix-8 DIT algorithms. These designs exploit programmable control logic to dynamically configure arithmetic operations, allowing trade-offs between speed, complexity, and power efficiency.

2. Theoretical Background

The Decimation-In-Time FFT algorithm recursively divides the DFT into smaller subproblems by exploiting symmetry and periodicity of complex exponential factors. Each stage performs butterfly operations combining even and odd indexed inputs. For a Radix- r FFT, the number of stages S is given by: $S = \log_r N$, where N represents the number of input samples. Higher radix FFTs such as Radix-4 and Radix-8 reduce the number of stages, thereby decreasing computational delay. A reversible logic gate establishes a one-to-one correspondence between input and output vectors. For a system to be reversible, the number of inputs must equal the number of outputs, and no information should be lost during transformation. Key parameters in reversible circuit design include quantum cost (QC), garbage outputs (GO), and constant inputs (CI). Common reversible gates include the Toffoli, Fredkin, Peres, TR, and DKG gates.

3. Design Architecture

The proposed design employs programmable reversible adders, subtractors, and multipliers based on TR, Peres, and DKG gates. Control signals determine the functional mode of operation, making the same hardware block reusable for multiple arithmetic operations. Each FFT butterfly performs the computations: $X[k] = A + B \cdot W_N^k$ and $X[k + N/2] = A - B \cdot W_N^k$, where $W_N^k = e^{-j2\pi k/N}$ represents the twiddle factor.

4. Simulation and Evaluation

The proposed design was implemented and simulated using Xilinx Vivado 2023.1 targeting FPGA device XC7A35T. Verilog HDL was used for coding, and both 16-point and 64-point FFTs were tested. Performance metrics include delay, power, quantum cost, and garbage outputs.

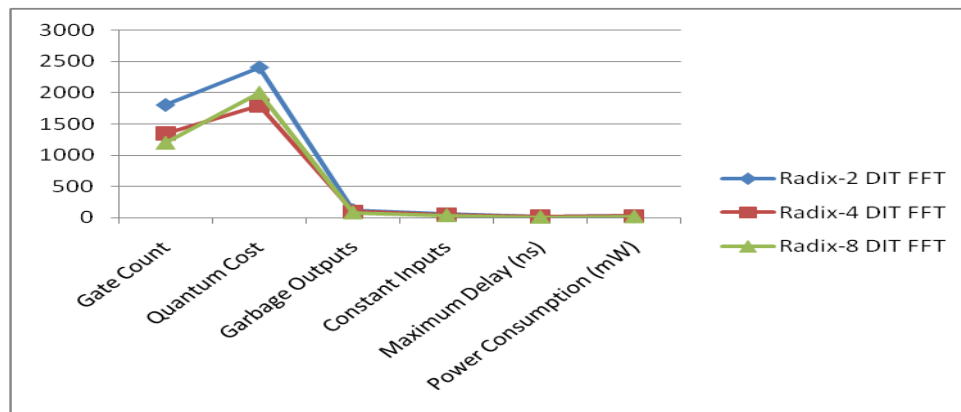


Figure 1: Comparison of delay and power among Radix-2, 4, and 8 FFTs (placeholder).

Results indicate that Radix-8 design yields the lowest delay (8.1 ns) and power (15 mW), while Radix-4 offers a balanced trade-off between hardware complexity and performance. Radix-2, although simplest, shows slightly higher delay and power due to more computational stages.

5. Conclusion

This paper presents programmable reversible logic-based FFT architectures for Radix-2, Radix-4, and Radix-8 DIT algorithms. The approach demonstrates improved power efficiency and reduced delay compared to traditional designs. Radix-8 achieves the best performance metrics, while the reconfigurable FFT architecture enhances adaptability for multi-radix applications. Future work will focus on optimizing reversible multipliers and extending the design for mixed-radix FFT implementations.

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