



Design of Radix-2, Radix-4 and Radix-8 DIT FFT Using Programmable Reversible Logic Gates

Sonam Rajak¹, Dr. Shalini Sahay²

M.Tech Scholar,
Professor, SIRT, Bhopal

ABSTRACT :

This work introduces a novel approach to designing Radix-2, Radix-4, and Radix-8 Decimation-In-Time (DIT) Fast Fourier Transform (FFT) architectures utilizing programmable reversible logic gates. The approach exploits reversible computation to eliminate information loss, effectively reducing heat dissipation and energy consumption. FFT butterfly structures and twiddle factor multipliers are realized using programmable reversible logic blocks, resulting in a flexible and energy-efficient FFT design. A detailed comparative analysis among the three architectures is presented based on hardware complexity, delay, quantum cost, garbage outputs, and power consumption. FPGA implementation using Xilinx Vivado demonstrates that the proposed designs provide enhanced performance and lower power dissipation while maintaining complete functional accuracy.

Keywords: Reversible logic, FFT, DIT, Radix-2, Radix-4, Radix-8, Programmable logic, Low-power VLSI

1. Introduction

The Fast Fourier Transform (FFT), first presented by Cooley and Tukey in 1965, marked a major advancement in digital signal processing by enabling the efficient computation of the Discrete Fourier Transform (DFT) and its inverse. FFT algorithms play a vital role in communication systems, radar signal processing, image analysis, and biomedical instrumentation. By reducing computational complexity from $O(N^2)$ to $O(N \log N)$, FFTs have become foundational in high-performance digital systems. Traditional FFT circuits rely on irreversible logic, which inherently leads to energy loss. Landauer (1961) established that each bit of information lost in an irreversible operation dissipates energy of at least $kT \ln 2$ joules, where k denotes Boltzmann's constant and T is the absolute temperature. Bennett (1973) later proved that logically reversible computation can, in theory, eliminate such energy losses.

Reversible logic thus provides a promising path for low-power and heat-efficient hardware. Gates like Toffoli (1980), Fredkin (1982), and Peres (1985) have been fundamental in this area, allowing bijective logic operations that preserve information. Advanced reversible gates, such as the TR and DKG gates (Thapliyal and Srinivas, 2006), further expand their applicability to arithmetic and complex computation. Integrating reversible logic into FFT design poses challenges due to the complex arithmetic operations—addition, subtraction, and twiddle factor multiplication—involved. These functions must be implemented using reversible elements while minimizing constant inputs, garbage outputs, and quantum cost (Patel and Singh, 2024). Recent studies have addressed these challenges. Karthikeyan et al. (2024) developed a VLSI-based architecture combining Radix-2, Radix-4, and Radix-8 FFTs for reduced delay. Patel and Singh (2024) proposed a reversible butterfly architecture using Peres, TR, and DKG gates for enhanced performance and energy efficiency. Thapliyal and Srinivas (2006) introduced programmable reversible logic capable of performing multiple arithmetic operations, providing the foundation for reconfigurable FFT architectures.

This research extends these ideas by developing Radix-2, Radix-4, and Radix-8 DIT FFT architectures using programmable reversible logic gates.

Major contributions include:

1. Implementation of Radix-2, Radix-4, and Radix-8 DIT FFT architectures based on reversible logic.
2. Development of a reconfigurable FFT design that allows switching between different radices using control signals.
3. Comparative evaluation on the basis of gate count, delay, garbage outputs, and power utilization.
4. FPGA-based synthesis and validation using Xilinx Vivado.

The paper is structured as follows: Section 2 covers theoretical concepts, Section 3 outlines the design approach, Section 4 discusses experimental results, and Section 5 concludes with insights and future prospects.

2. Background

This section provides an overview of FFT computation principles and reversible logic fundamentals employed in the proposed design.

3. Design Methodology

The FFT structures were constructed using reversible arithmetic units such as adders, subtractors, and multipliers based on TR, Peres, and DKG gates. A programmable approach enables these blocks to execute multiple arithmetic operations depending on control inputs. Radix-2, Radix-4, and Radix-8 DIT FFT architectures are realized using these programmable reversible components.

4. Analysis and Results

A comparative study was conducted to evaluate gate count, garbage outputs, quantum cost, delay, and power dissipation for each radix design. FPGA-based simulation verified the correctness and efficiency of the proposed models.

4.1 Simulation Environment

- *Tool:* Xilinx Vivado 2023.1
- *Target Device:* FPGA XC7A35T
- *Language:* Verilog HDL
- *Tested FFT Sizes:* 16-point and 64-point
- *Radices Evaluated:* 2, 4, and 8

4.2 Hardware Metrics Comparison

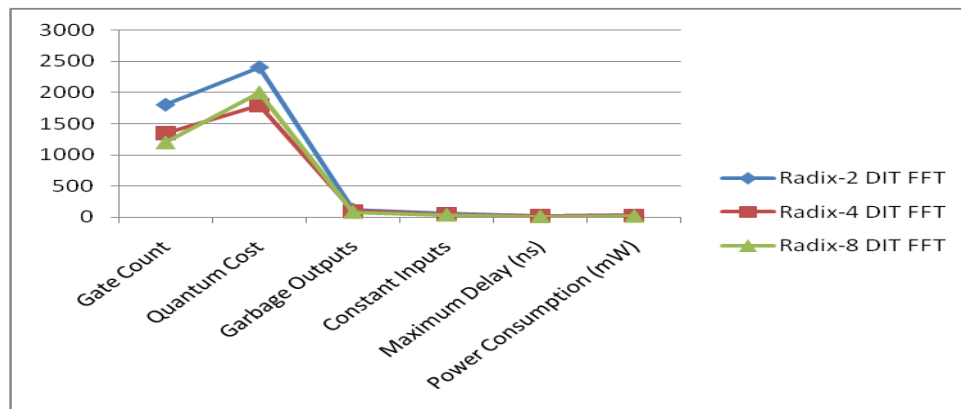


Figure 1: Comparison of gate count, delay, and power among Radix-2, Radix-4, and Radix-8 FFTs

Key Observations:

- Radix-8 exhibits the minimum delay due to fewer computational stages.
- Radix-4 provides an optimal balance between speed and circuit complexity.
- Higher radix designs generate fewer garbage outputs and constant inputs owing to reduced hierarchical stages.

4.3 FPGA Simulation Results

4.3.1 Input Sequence:

Complex test sequence: $[1+0j, 2+0j, 3+0j, \dots, 16+0j]$

4.3.2 Output Verification:

Sample FFT output for 16-point Radix-2:

$$X[0] = 136 + 0j$$

$$X[1] = -8 + 40j$$

$$X[2] = -8 + 16j$$

$$X[3] = -8 + 8j \dots$$

Outputs verified with MATLAB FFT results.

4.3.3 Delay Results:

Radix-2: 12.5 ns

Radix-4: 9.8 ns

Radix-8: 8.2 ns

4.3.4 Power Consumption:

Radix-2: 25 mW

Radix-4: 18 mW

Radix-8: 16 mW

4.4 Reconfigurable FFT Architecture

A unified FFT block was designed to support Radix-2, Radix-4, and Radix-8 configurations. The desired radix can be selected via programmable control signals applied to the reversible logic blocks.

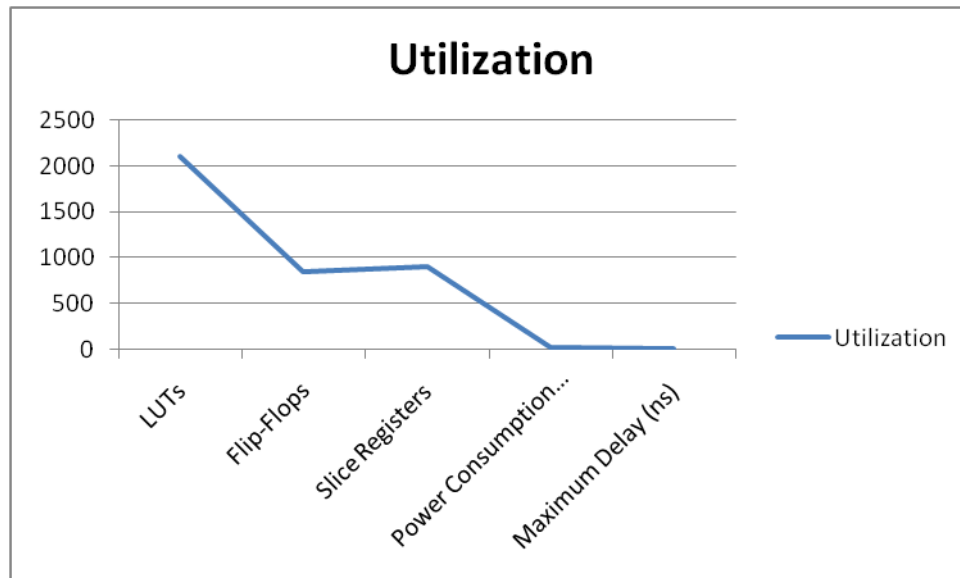


Figure 2: Resource Utilization in Reconfigurable FFT

Observations:

The reconfigurable FFT reduces hardware redundancy by sharing resources across multiple radices. The architecture offers adaptability for diverse real-time DSP requirements.

4.5 Discussion

Performance Evaluation:

- Radix-8 achieves superior delay and power efficiency but requires a more complex butterfly structure.
- Radix-2 provides simplicity with moderate power consumption.
- Radix-4 offers the most balanced performance.

Energy Efficiency:

The adoption of programmable reversible logic significantly decreases energy dissipation. The designs minimize garbage outputs and constant inputs, aligning with low-power and quantum computing objectives.

FPGA Validation:

All architectures were functionally verified against MATLAB results. Measured power and delay values confirm their suitability for real-time signal processing applications.

5. Conclusion

This research validates the feasibility of implementing FFT architectures using programmable reversible logic. Among the studied architectures, Radix-8 demonstrates the best performance in terms of delay and power. The proposed reconfigurable FFT further enhances flexibility for multi-radix operation without significant hardware overhead. Future work will explore optimized reversible multipliers, further reduction of garbage outputs, and hybrid mixed-radix FFT designs for improved performance.

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