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Fault Diagnosis of 24 Hours Based Clock Internal Modules using VHDL and Implementation with FPGA

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ABSTRACT

This paper presents the design and implementation of a 24-hour digital clock using VHDL, identifies the fault detection of various modules such as counters, bus multiplexer, test vector generator, comparator and BCD seven segment display. The proposed system is based on fault detection of inter modules results to accurate timing and better security. The counter modules include a mod 10 counter for 1-minute cycles, a mod 6 counter for 10-minute cycles, a mod10 or mod5 counter for 1-hour cycles, and a mod 3 counter for 10-hour cycles. These counters together track minutes and hours which provides a complete time representation. The bus multiplexer efficiently tracks data between the different modules based on control signals in the system rise to smooth data flow and system synthesis. The test vector generator produces specific input patterns to verify the functionality of the counters and other system components, for testing and verification. The comparator plays a critical role in fault detection by comparing actual outputs from the counters with expected values, thereby identifying any discrepancies or faults within the system. Lastly, the BCD (Binary-Coded Decimal) segment display converts the binary outputs from the counters into a readable decimal format, after enabling the clear pin of seven-segment display. The integration of these components ensures the digital clock's precision and reliable, allowing for 24-hour timekeeping mechanisms for fault detection and system validation.

Keywords: VHDL, bus multiplexer, counter, test vector generator, BCD segment display

Introduction:

Existing system comprises of clock and a stopwatch operates in two modes: clock mode and stopwatch mode. In clock mode , the digital tube displaying hours, minutes and seconds in a 24 hour cycles. Alarms can be set and off and data can be stored temporarily or in sequence. The system uses a frequency divider to divide the system clock signal for each module. The existing system uses a counter to count hours, minutes and seconds, and a scanning display module to display the digital tubes dynamic display. The frequency divider module take a incoming clock signal and reduces its frequency to different levels required by various components, it can take a high-frequency signal and reduce it to 1Hz or 1kHz signals, which are utilized by other components of the system. This module ensures that each component receives the correct timing signal for its function. The counter module is responsible for keeping track of time or counting pulses. In clock mode, it counts seconds, minutes, and hours based on the 1Hz signal from the frequency divider. In stopwatch mode, it measures in similar units such as milliseconds, seconds, and minutes. The limitations of the existing system are stop watch design,clock mode only showing the current time the stopwatch mode not tracking events, the alarm setting being unnecessary, counters not counting events accurately, and the lack of effective fault detection and correction, To overcome the problems in the existing system, proposed system is implemented with accurate timing and reliable operation of the system. The paper focuses on clock with additional features includes display with 1 minute, 10 minutes, 1 hour and 10 hours in clock mode, stop watch for timing events, removing the alarm setting feature, making counters accurately track events, and fault detection and correction mechanism of the clock.

Proposed System:

The proposed system operates in two main modes: working mode and test mode. The proposed system uses various modules, such as counters, bus multiplexers, test vector generator, comparator and a BCD seven segment display is shown in fig:1 The counter modules in the system are essential for accurately tracking and displaying time. There are four counters, each plays a specific role based on their module such as two Mod-10, Mod-6, and Mod-3 counters.[1]. In working mode, these counters are connected in series. First Mod-10 counter[2] keeps track of minutes (0-9), the Mod-6 counter[3] counts ten minutes (0-5), second Mod-10 counter[4] counts hours (0-9), and the Mod-3 counter [5] increments to ten-hours. (0-2). This series configuration allows the system to keep and show time in a standard 24-hour format. In test mode, the counters are reconfigured in parallel mode enables the counters to be tested individually for faults by applying test vectors[6] to the comparator, the outputs of test vector generator[7] and comparator differs then fault

is identified and it can be corrected. The control signal is applied to the bus multiplexer selects the counter, then counter output compares both outputs of bus multiplexer output and test vector[8-9] generator results to correct the fault in the system and displayed with the help of BCD seven segment display.

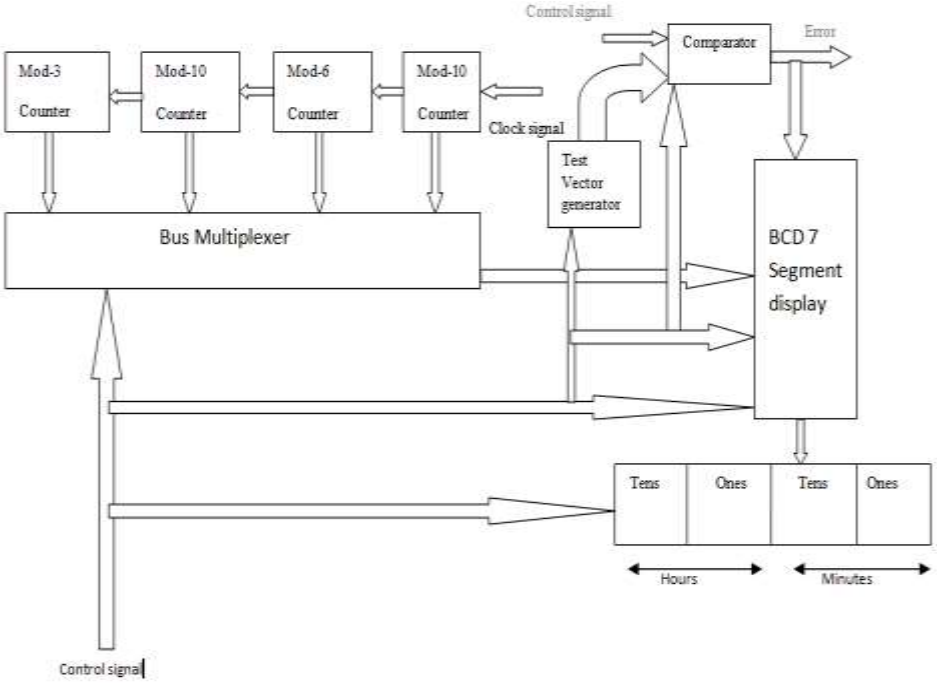

Figure:1 Proposed system in 24-Hours digital clock in FPGA

Testable Mod counters:

60 Counter:

The 60-hours comprises of mod 10 counter[10] and a mod 6 counter consists of four inputs are MIN_CLK, RESET, TM_CLK, T_C_MOD and two outputs are ONE_MIN and TEN_MINS. In working mode when the RESET = 0, MIN_CLK=1, T_C_MOD=0, mod 10 counts[11] from 0 to 9 minutes with effective the mod 6 increments by 1 it means 10 minutes again this process repeated till mod 6 counter increments by 5 it means by 50 minutes[12]. Now mod 10 counters from up to 9 minutes then the counter display 60 minutes in the clock. In test mode the 60 minutes counter[13] RESET = 0, TM_CLK=1, T_C_MOD =1,then the mod 6 counter [14] counts from 0 to 5 minutes, and mod 10 counter counts from 0 to 9 minutes if counting is not proper during the testing of mod 6 and mod 10 counter results to error in the clock. The fault can be rectified based on the error generate in the corresponding counter[15].

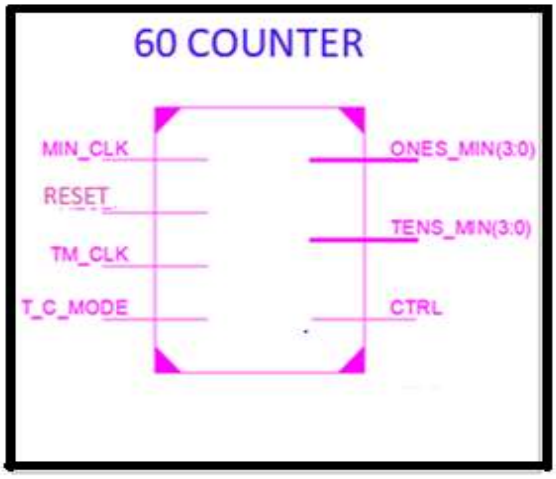

Figure 2: The schematic diagram of 60 Counter

Simulation Result:

Figure 3 represents this simulation waveform of 60 counter, Mod 60[16] has four inputs are clock, enable, reset, and two output one minute and ten minutes When reset=0,enable=1 then one minute counter counts[17] from 0 to 9 minutes with effective the ten minutes increments by 1 again this process repeated till ten minutes counter[18] increments by 5 it means it means by 50 minutes. Now ten minutes counter from up to 9 minutes then the counter display 60 minutes in the clock.

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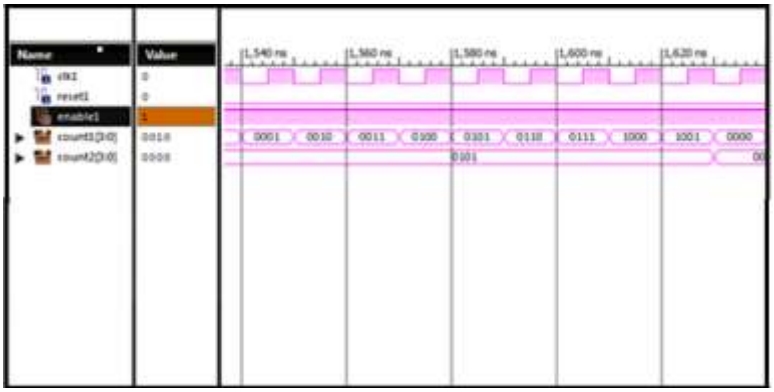


Figure 3: simulation waveform of 60 counter.

24 Counter:

The 24-hours comprises of mod 10 counter[19] and a mod 2 counter consists of four inputs are HRS_CLK, RESET, TM_CLK, T_C_MOD and two outputs are ONE_HRS and TENS_HRS. In working mode when the RESET = 0, HRS_CLK =1,mod 10 counts[20] from 0 to 9 hour with effective the mod 2 increments by 1 it means 10 hours again this process repeated till mod 2 counter increments by 2 it means by 20 hours. Now mod 10 counters[21] from up to 4 hours then the counter display 24 hours in the clock. In test mode the 24 hours counter RESET = 0, TM_CLK=1,then the mod 2 counter counts [22]from 0 to 2 hour, and mod 10 counter counts from 0 to 9 hour if counting is not proper during the testing of mod 2 and mod 10 counter[23] results to error in the clock. The fault can be rectified based on the error generate in the corresponding counter.

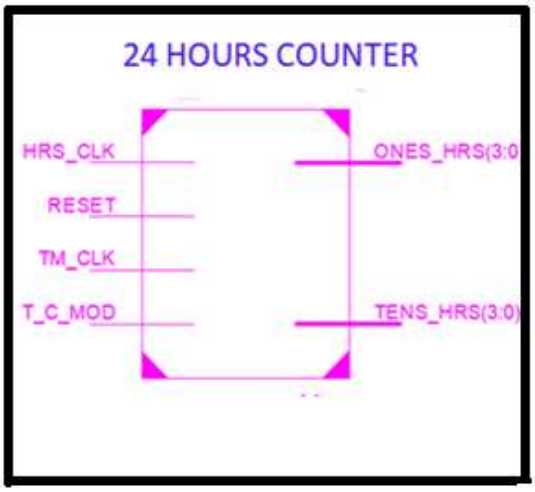
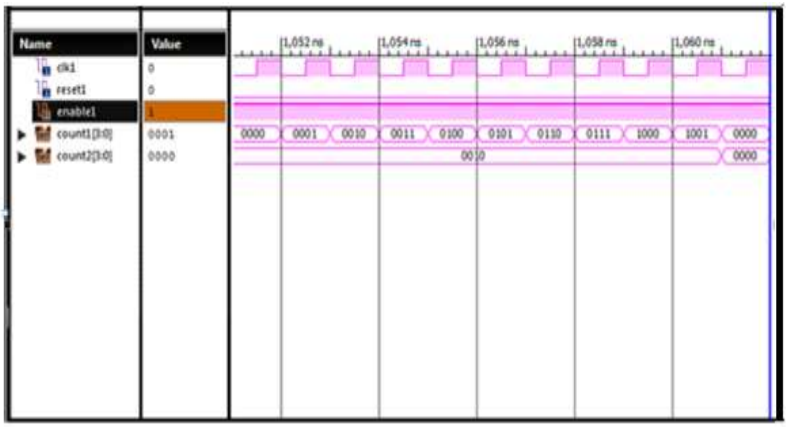


Figure 4: The schematic diagram of 24 Counter

Simulation Result:

Figure 5 represents this simulation diagram 24 counter, Mod 24 has four inputs are clock, enable, reset, and two output one hour and ten hours. When reset=0,enable=1 then one hour counter [24] counts from 0 to 9 minute with effective the ten hours increments by 1 again this process repeated till ten hours counter increments by 2 it means it means by 20 hours. Now ten minutes counter from up to 4 minute then the counter display 24 hours in the clock.



.**Figure 5: Simulation waveform of 24 counter.**

Test Vector Generator:

The test[25] vector generator produces a specific input patterns to verify the functionality of counters and other components, the test vector generator has four inputs are reset, clock, enable, select, and one output in the test vector generator. when clock =1, reset=0, Select=00 is connected, to the output is mod 3 counter counts from 0 to 2, indicating a 10 hours display on a clock, with select =01 are connected, to the output is mod 6 counter counts from 0 to 5 ,indicating a ten minutes display on a clock, with select = 10 is connected, to the output is mod 6 counter counts from 0 to 9 ,indicating a 1 minute display on a clock, with select= 11 is connected, to the output is mod 6 counter counts from 0 to 5 ,indicating a ten minutes display on a clock

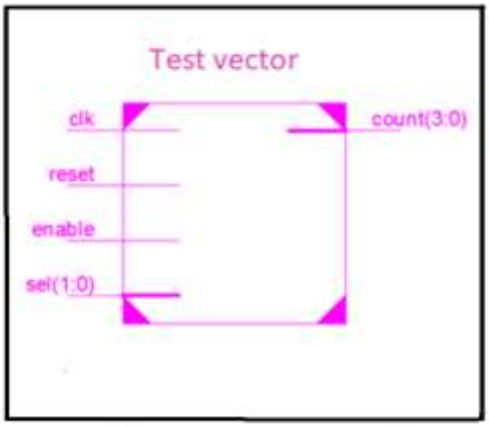


Figure 6: The schematic diagram of the 60 Counter

Figure 7 represents this simulation diagram of the test vector generator has four inputs are reset, clock, enable, select, and one output. when clock =1, reset=0, select=00 is connected to the output is mod 3 counter counts from 0 to 2, indicating a 10-hour display on a clock.

Figure 7: Simulation waveform of test vector generator(mod -3 counter).

Figure 8 represents this simulation diagram of the test vector generator has four inputs are reset, clock, enable, select, and one output. when clock =1, reset=0, Select=01 are connected to the output is mod 6 counter counts from 0 to 5 ,indicating a ten minutes display on a clock.

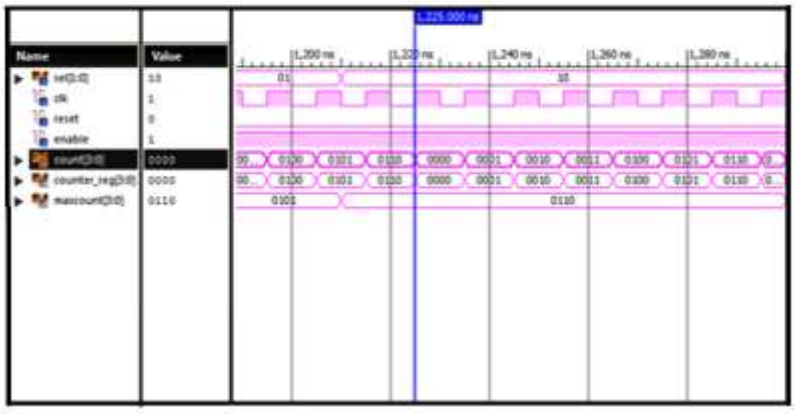


Figure 8: Simulation waveform of test vector generator(mod-6 counter).

Figure 9 represents this simulation diagram of the test vector generator has four inputs are reset, clock, enable, select, and one output. when clock =1, reset=0, Select=10 are connected to the output is mod 10 counter counts from 0 to 9 ,indicating a one minute display on a clock.

Figure 9: Simulation waveform of test vector generator(mod-10 counter).

Figure 10 represents this simulation waveform of the test vector generator , has four inputs are reset, clock, enable, select, and one output. when clock =1, reset=0, Select=11 are connected to the output is mod 10 counter counts from 0 to 9 ,indicating a ten minutes display on a clock.

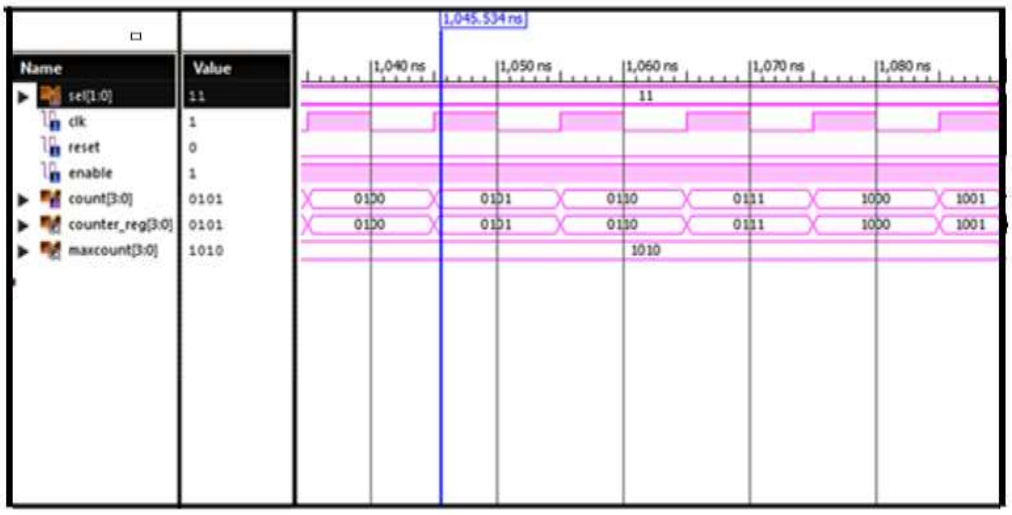


Figure 10: Simulation waveform of test vector generator(mod-10 counter).

Clock:

A testable 24-hour clock is a timekeeping device that displays time in a 24-hour format and is designed to be easily tested for accuracy and functionality[26].

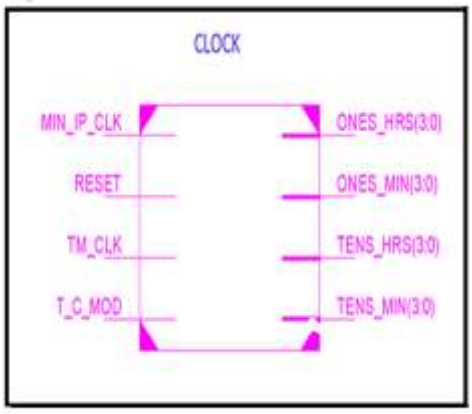


Figure 11: The schematic diagram of the clock

Figure 11 represents the clock consists of four inputs : MIN_CLK, RESET, TM_CLK, T_C_MOD and four outputs are ONE_MIN ,TEN_MINS, ONE_HR and TEN_HRS. In working mode when the RESET = 0, MIN_CLK=1,TM_CLK=0, T_C_MOD=0, mod 10 counts from 0 to 9 minute with effective the mod 6 increments by 1 it means 10 minutes again this process repeated till mod 6 counter increments by 5 it means by 50 minutes. Now mod 10 counters from up to 9 minute then the counter display 60 minutes in the clock.mod 10 counts from 0 to 9 hour with effective the mod 2 increments by 1 it means 10 hours again this process repeated till mod 2 counter increments by 2 it means by 20 hours. Now mod 10 counters from up to 4 hours then the counter display 24 hours in the clock. In test mode when the RESET = 0, MIN_CLK=0, T_C_MOD=1, and TM_CLK=1,then the mod 6 counter counts from 0 to 5 minute, and mod 10 counter counts from 0 to 9 minute and then the mod 2 counter counts from 0 to 2 hour, and mod 10 counter counts from 0 to 9 hour if counting is not proper during the testing[27] of mod 2 and mod 10 counter results to error in the clock. The fault can be rectified based on the error[28] generate in the corresponding counter.

Simulation Result:

Figure:12 represents this simulation waveform of the clock has four inputs are MIN_CLK, RESET, TM_CLK and four outputs are ONE_MIN ,TEN_MINS, ONE_HR and TEN_HRS. when the RESET = 0, MIN_CLK=0, T_C_MOD=1, and TM_CLK=1,then the mod 6 counter counts from 0 to 5 minute, and mod 10 counter counts from 0 to 7 hour and then the mod 2 counter counts from 0 hour, if counting is not proper during the testing of mod 10 counter results to error in the clock.

Figure 12: Simulation waveform of Fault

Simulation Result:

Figure:13 represents this simulation waveform of the clock has four inputs are MIN_CLK, RESET, TM_CLK and four outputs are ONE_MIN, TEN_MINS, ONE_HR and TEN_HRS. when the RESET = 0, MIN_CLK=0, T_C_MOD=1, and TM_CLK=1,then the mod 6 counter counts from 0 to 5 minute, and mod 10 counter counts from 0 to 9 hour and then the mod 2 counter counts from 0 to 2 hour, if counting is not proper during testing, if the Mod-10 counter does not count properly or fails to cycle through its range from 0 to 9, it indicates a fault[29] in the clock system. For example, if the counter shows incorrect values or skips counts, it suggests that the counter's logic or its integration with other components might be faulty[30]. Any discrepancies or errors detected in the Mod-10 counter are critical, as they directly affect the accuracy of the minute and hour displays[31]. The specific errors observed during the test mode allow for targeted diagnostics by identifying the Mod-10 counter is producing incorrect outputs or failing to cycle correctly[32], maintenance can isolate the issue and perform necessary repairs or adjustments..

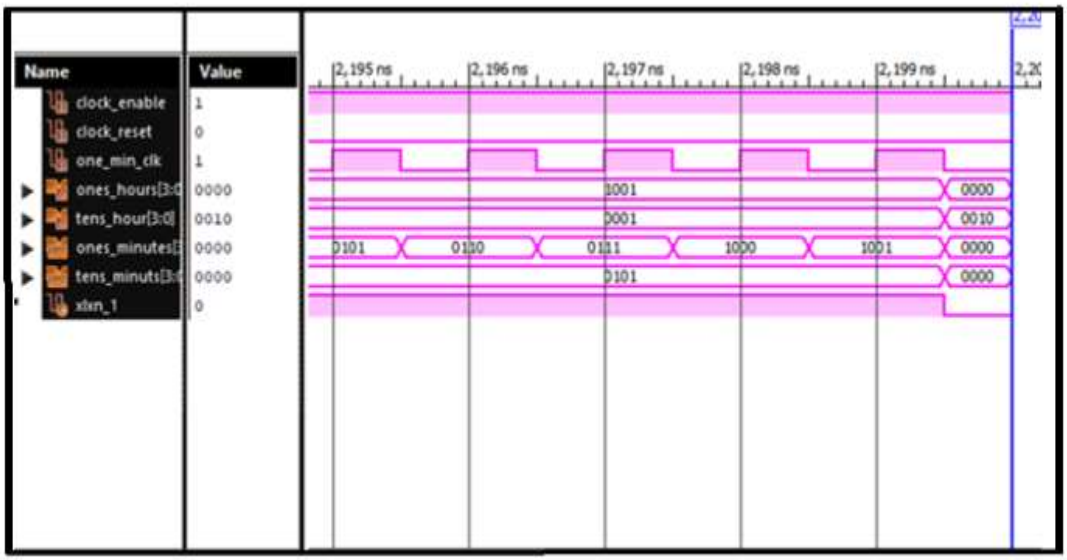


Figure 13 : Simulation waveform of No fault

Conclusion :

In this project work the digital clock is capable of displaying minutes,12/2hours with stopwatch display up to 60 minutes, proposed system is implemented with VHDL coding technique and verified the simulation results of 10 counter,3counter,10 counter,6 counter, bus multiplexer, test vector generator, comparator, clock, fault and no fault detection. These observations indicate that the various modules tested, both with and without fault detection, function properly in the 24-hour digital clock while maintaining low power consumption. In the future, the system will be implemented with fabrication techniques that lead to machine learning or artificial intelligence to further enhance the system's ability to proactively identify and correct issues.

Future Scope:

Future development in fault detection of inter-module connections in VHDL and FPGA-based 24-hour digital clock systems can focus on incorporating sophisticated fault detection methods like machine learning or artificial intelligence to further improve the system's capacity to in advance identify and correct issues and additionally, improved fault tolerance techniques, such as redundancy and self-healing mechanisms, can be considered to enhance overall reliability by ensuring effective error correction and fault tolerance support include new features into the system, such as date tracking, alarms, and network time synchronization, could enhance its usefulness and expand its range of applications. In additionally, analyzing power optimization methods can lead to more energy-efficient FPGA implementations and particularly for portable or battery operated devices and furthermore, implementing in FPGA technology can make the way for more complex and innovative systems, enhancing user interfaces to make them more accessible and overall user experience, leading to the development of more complex, reliable and flexible digital clock systems.

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