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Design and Implementation of Efficient Multiplier Using Reversible Logic Gates

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ABSTRACT

Reversible logic has emerged as a noteworthy technological advancement in recent times. It is introduced to reduce the power dissipation due to energy consumption. Reversible gates have the capacity to maintain both input and output data, which lowers errors and increases the dependability of electronic systems. This paper presents the design of a 4-bit array multiplier by employing Dual Key Gate (DKG). The proposed design is implemented to improve design features like Gate Count, Quantum Cost, Ancillary Inputs and Garbage Outputs. The suggested reversible multiplier has reduced the quantum cost of 30% and gate count of 50% over the existing design. The proposed design was simulated by using Xilinx 14.7 tool.

Keywords: Reversible gates, Quantum Cost, DKG gate, Unsigned Array Multiplier.

I.INTRODUCTION

Low power and high speed of operation, or minimum time delay, are the trade-offs in VLSI design. The majority of digital systems have low power requirements, higher operating speed with no delay. Digital integrated circuit design is rapidly evolving field in VLSI design that is in high demand. According to Landauer's law, irreversible logic operations ought to generate heat equivalent to kT joules for each bit of information lost, where T is the absolute temperature and k is Boltzmann's constant. The amount of heat radiating at room temperature is minimal but not negligible [1].Multiplier is the prime component in any digital computing machine. Power dissipation should be evaluated when designing the multiplier. Power losses can be reduced by introducing reversible logic into the multiplier design. In the fields of digital signal processing, nanotechnology, rapid computing, and power optimization circuits, reversible logic may become the new standard. [2].Reversible functions may be built as a series of reversible logic gates since they are equipollent. [3].In these circuits, the quantity of inputs and outputs must be equal, fan out, and feedback is prohibited [3]. Recent developments in quantum computing have also improved since quantum operations are inherently reversible [3].Quantum bits, or qubits, are the fundamental information units of quantum computing. [4-5]. The primary concern of this paper is multiplication, a crucial operation used in a wide range of applications. There are several ways to put a digital multiplier into practice. One popular approach is to compute an array of intermediate products, which are then combined via binary adders to obtain the end result.

II. REVERSIBLE LOGIC

The reversible logic is initiated when the main objective is optimisation of low-power and time-efficient designs [6]. By utilising reversible logic, the truth table of the combinational logic is developed in a uniquely specified pattern [6].

The reversible logic gate incorporates a one-to-one correspondence, which is known as bijective: determine the outputs based on the inputs, and conversely. This condition satisfies the Landauer's principle. In terms of power dissemination and latency, reversible logic is a possible substitute for traditional digital logic in arithmetic operations. The following parameters are used to define the efficiency of the reversible circuits.

A. Ancillary input [6]: It is also called as constant input which is not used in computation but plays a crucial role in reversibility.

B. Garbage output [6]: The outputs that aren't participated in the computation are called garbage outputs. Without garbage outputs, we can’t achieve reversibility.

B. Quantum cost [6]: Quantum cost is used to define how many primitive gates are used in the circuit. It describes the efficiency of the circuit.

III. PRIMARY REVERSIBLE LOGIC GATES

A number of reversible logic gates have been introduced. The primary reversible logic gates are:

Feynman Gate [7]: The logic circuit for this 2 input 2 output gate is outlined in Figure 1. Another name for it is the Controlled Not (CNOT) Gate. It is typically employed for Fan Out scenarios and has a quantum cost of one.

Peres Gate [7]: The logic circuit for this 3 input 3 output gate is outlined in Figure 1. Quantum cost of Peers gate is four. It is employed to implement several Boolean operations, including AND and XOR.

Fredkin Gate [7]: It is a 3 input 3 output gate, and Figure 1 depicts its logic circuit and itsQuantum cost is five. A Multiplexer will be designed by using this gate.

Toffoli Gate [7]: It is also 3 input 3 output gate, and Figure 1 depicts its logic circuit and it has Quantum cost five. It is also named as universal gate due to any combinational logic can be implemented by using this gate.

The above mentioned reversible gates are also known as the primary reversible logic gates and the logic diagrams are Outlined the below figure 1.

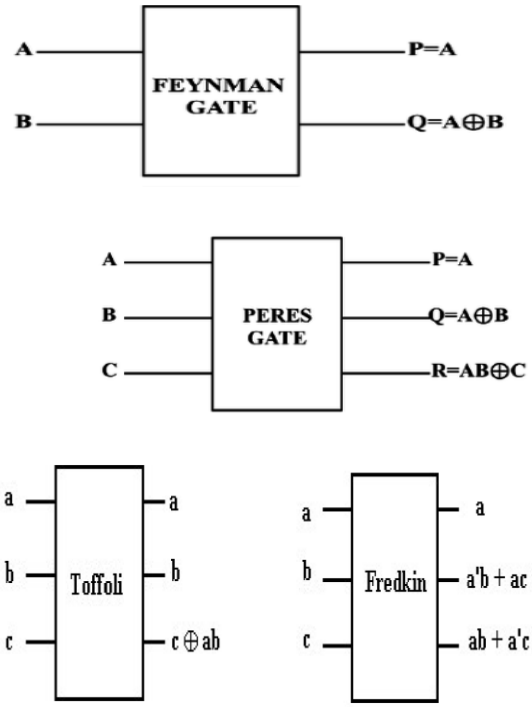

Figure1 Primary Reversible Logic Gates

IV. EXISTING DESIGN

In the existing design the multiplier was developed by using Toffoli Gates. So, the multiplier has gate count 56 and quantum cost is 160. To lower the gate count and quantum cost proposed multiplier has introduced by using proposed gates.

V. PROPOSED DESIGN

In this paper, unsigned array multiplier is used to multiply the positive binary numbers. Figure 2 illustrates how a 4x4 reversible multiplier works. To Compute 4-bit multiplication, it comprises of 16 intermediate products of the X and Y inputs. However, we can implement the multiplier design up to N x N bits. The proposed multiplier design was following two steps.

Step I: Intermediate Product Generation

Step II: Multi-Operand Addition (MOA)

Each bit of the multiplicand is multiplied by the multiplier in intermediate product generation.Carry save adder is used for addition of intermediate product bits, and carry propagation adder is used for final addition in multi-operand addition.

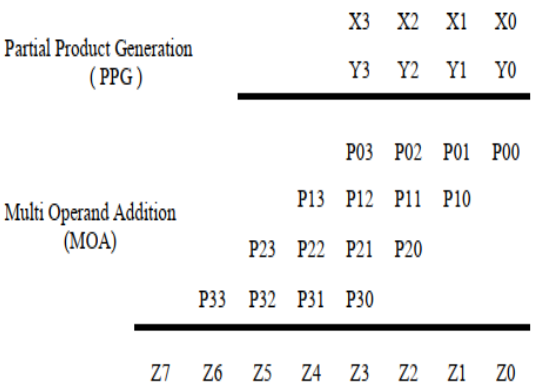

Figure.2. 4*4 Unsigned Multiplier

For intermediate product generation, Peers gates and Toffoli gates are used for operations as shown in Figure 4. Dual Key Gate (DKG) and Peers Gate are used for Multi Operand Addition. Peers gate serves as a half adder, while DKG gate functions as a full adder. [8]. DKG gate is 4 input 4 output gate as shown in Figure 3. A Full adder/ Full Subtractor circuit can be developed with this gate. When input 'A' is 0, then the gate is used for addition purpose, and when the input 'A' is 1, then the gate is used for subtraction purpose. When compared to other gates, the DKG gate uses less power [9]. The 4x4 DKG gate has a quantum cost of 5[8].

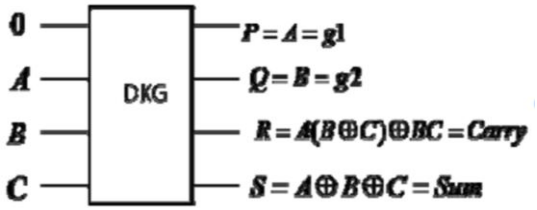

Figure3: Double Key Gate as Full Adder

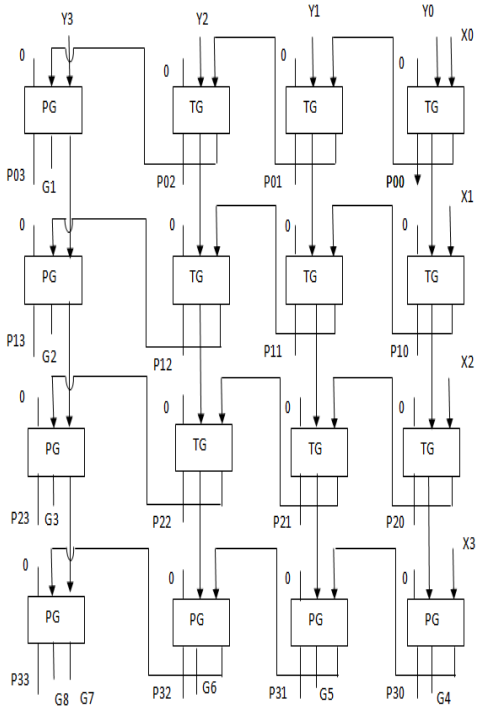

Figure4: Intermediate Product Generation Using Peers Gates and Toffoli gates

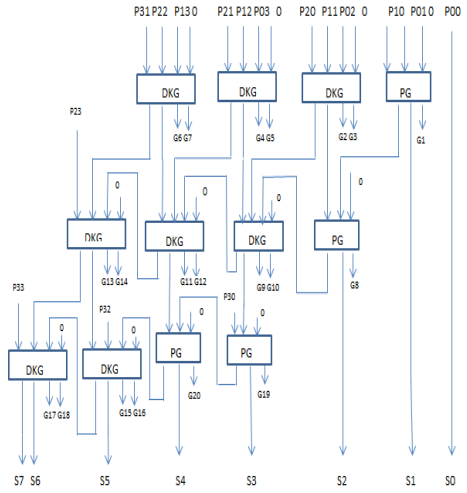

Figure5: Multi Operand Addition using DKG and PG gates

V.RESULTS

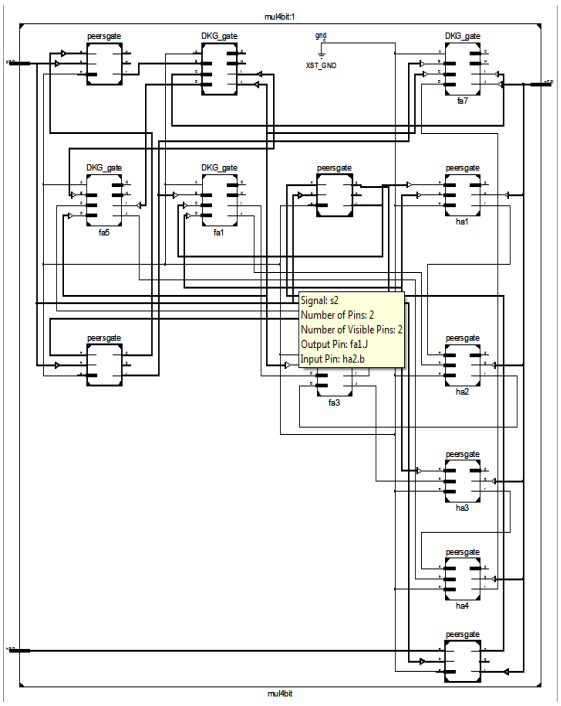

Figure7: RTL Schematic of 4 bit Unsigned Multiplier

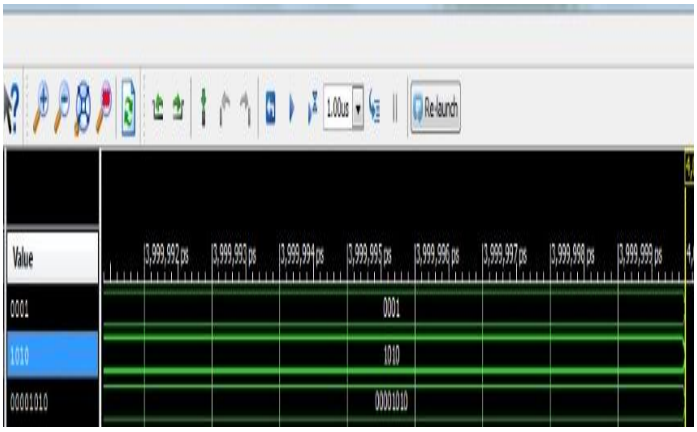

Figure 8: Output waveforms of unsigned multiplier

Table 1.Comparison of results

Parameter	Existing design	Proposed design
Gate count	56	28
Constant inputs	28	28
Garbage outputs	28	28
Quantum cost	160	129

As shown in the above table 1, proposed design was reduced the quantum cost and gate count and gives an efficient multiplication with DKG gates compared with the existing design [11-12].

VI. CONCLUSION

The unsigned array multiplier employing DKG gates in the proposed architecture has lower power dissemination with higher operating speed. By using DKG gates, the multiplier architecture implemented with less no. Of gates and a lower quantum cost. The proposed multiplier is faster than the existing one. It is simulated in Xilinx 14.7 tool.

VII. FUTURE WORK

The Baugh-Wooley Multiplier is an efficient multiplier used for signed and unsigned multiplication. It can be designed with less no. of gates, and additional efficient multipliers such as encoded Wallace Tree multipliers and Dadda multipliers have been designed in subsequent work utilizing the proposed reversible logic gates.

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