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SETUP AND HOLD ANALYSIS OF AXI PROTOCOL FOR INCREMENT BURST TYPE USING UVM VERIFICATION

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ABSTRACT :

Designs for System-On-Chips (SoCs) are getting more and more intricate. Several Intellectual Properties (Ips) are integrated into a single SoC, and Several bus protocols are used by these IPs to communicate with one another. Since verification accounts for more than 70% of the design cycle for these widely used protocols. Reusable verification environments are essential. In this work, the AXI protocol is validated using the UVM. Based testbench structure. As a master device, the UVM testbench transmits all addresses and data. And control information to the slave device read back the random data. Chips have to be examined to ensure that the design is correct and that they are functioning within the given parameters. The waveforms acquired to verify that the code for the Increment Burst type is correct. The AXI protocol's code coverage results from the code coverage-based test case validation have reached 100%. The timing report is obtained to examine the slack is met or violated in the design. The simulation is run with the Synopsys VCS tool.

Keywords: System-on-chip, Intellectual Properties, Universal Verification Methodology (UVM), System Verilog (SV), AXI Protocol.

INTRODUCTION :

The Universal Verification Methodology (UVM) is a notion that has been developed to offer robustness, reusability, and reliability for the functional verification of System on Chips (SoC) [4]. Since UVM was related to become an IEEE 1800.2 standard in 2017, it has taken over as the industry standard for verification. Many hours and resources are saved during verification because to UVM's capability of code reuse [3].

High-bandwidth, low-latency designs use the AXI protocol. As a result, the AXI protocol is frequently utilized in contemporary SoCs as a system bus for inter-IP communication. The AXI protocol's primary characteristics include separate read and write data channels, burst-based transactions, support for unaligned data transport, and separate address and data lines [5].

A test environment for AXI interface verification has been successfully implemented using UVM methodology. VCS has been used in simulations. The test environment's architecture is based on UVM components such as sequencers, drivers, scoreboards, agents, and others. A number of sequences of tests have been implemented to address both special cases and sporadic transactions. The AXI protocol-enabled data transfers are successfully displayed in the simulation waveform. In order to complete the verification, code coverage reports are evaluated. During the synthesis process, the timing report is obtained.

RESEARCH METHODOLOGY :

The AXI protocol operates on a master and slave device as shown in “Figure. 1”. The five distinct channels for reading and writing are read address, read data, write address, write data, and write response. "Fig. 1" depicts the write channel architecture. Data transfer from a master device to a slave device occurs via a write data channel. The slave uses a write response signal to tell the master that the data transmit is finished.

Figure 1: AXI read and write channel

The write and read channel architecture is shown in "Fig. 2". The basis of the AXI interface is the two-way handshake mechanism. In order to let the slave know that the IP address or data on the channel is correct, the master sends a valid signal. The slave alerts the master when it is ready to receive the information. In this manner, before any data is sent over the channel, the master and slave shake hands. The address and control data required for a write transaction over a write address channel must be sent by the master. Write data is transferred from the master to the slave via write data channels, which have a width of either 32 or 64 bits. When the transaction is complete, the slave sends an indication over the write response channel.

Figure 2: AXI read and write Transactions

Verification Environment: A reusable verification environment is created using the System Verilog UVM methodology. The primary benefit of using UVM is that all components can be created by simply extending base classes, as the System Verilog leverages OOPs concepts to make component development simpler and faster. Therefore, parts of the verification process can be reused in various applications.

"Fig. 3" depicts the AXI testbench structure based on UVM. The sequencer provides this sequence to the driver. Every data field that the driver drives and the monitor watches are contained in the sequence-item of the sequencer. The information in these places is randomly assigned a number before being sent to the driver via a sequencer. The driver waits for the sequencer's transaction. The driver sends the AXI packets of data to the AXI DUT after receiving them from the sequencer. Through the TLM port, the driver and sequencer are connected. After converting the data from the DUT into transactions, the data is sent by the monitor to additional related components, such as the scoreboard. The sequencer, driver, and monitor are all contained within the agent. It could be either active or passive; the former has three components and drives stimulus to the DUT, while the latter has merely a monitor. During an agent's linking phase, the sequencer and driver are linked. The scoreboard compares the DUT's output with the AXI transaction it receives from the monitor. Shift operation is executed to generate a result based on the DUT's signals for input

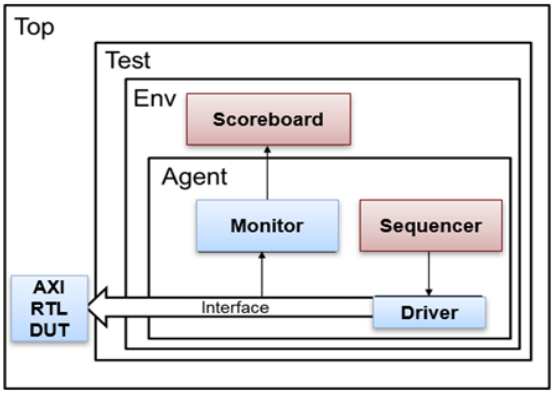

Figure 3: AXI testbench structure of UVM

and compares it with the information obtained from the AXI slave device. It is then possible to confirm that write and read transactions via the Successful completion of the AXI interface is achieved by comparing the information on the scoreboard. The UVM verification environment sits atop the environment. It creates an agent and the scoreboard and joins them. It consists of several agents and a bus monitor. The environment makes it possible to alter performance and topology to create a verification environment that is extensible, adaptable, and reusable. A top-level block in UVM is called a test block. It serves two purposes. Make the environment block first. In the second step, attach the sequencer to the sequence.

After writing takes four clock cycles, a different sequence is driven to read the data via the register that holds the data. As a result, shifted data is written to the DUT's data register, from which it is read. The read sequence provides the data register address and related AXI read channel signals. The monitor tracks this DUT response and transforms it into a transaction. Next, the written data and the data read from DUT are compared on the scoreboard. If the two sets of data match, the AXI interface is correctly transferring the data. To conclude the verification process, reports on code coverage are assessed. During the synthesis process, the timing report is obtained.

RESULTS AND DISCUSSION

Results of read and write transactions made via the AXI protocol are shown in this section. The Synopsys VCS tool is used to run the simulation [2]. To optimize the interface's bandwidth, separate address and data channels should be used for read and write transfers. There is no timing relationship between the groups of read and write channels. This implies that a read sequence and a write sequence may occur simultaneously. The reason of such approach is to check the data correctness. The output waveform of the AXI protocol implementation for the Increment burst type is displayed in Figure 5.

Test case: Random read and write AXI transactions for INCR Burst Type

In this case, the data that will be entered into the shift register is generated at random. "Fig. 5" displays the write and read operation simulation results.When executing the test case, the number of transactions is specified using the command line argument. We can observe from the waveform, the Data is Incrementing for every positive edge of the clock in the write and Read Transaction. The input data that was provided to DUT and validated using Testbench. The code coverage results based on the AXI protocol test case verification are displayed in Fig. 4. It is evident from Fig. 4 that the test case environment has verified the read and write transactions with 100% coverage. Timing reported has been generated using synthesis process in VCS tool. The AXI Protocol has been designed and generated for the 14nm Technology and the timing report is shown below. As a result, able to determine in the timing report whether the suggested methodology's slack is met or not.

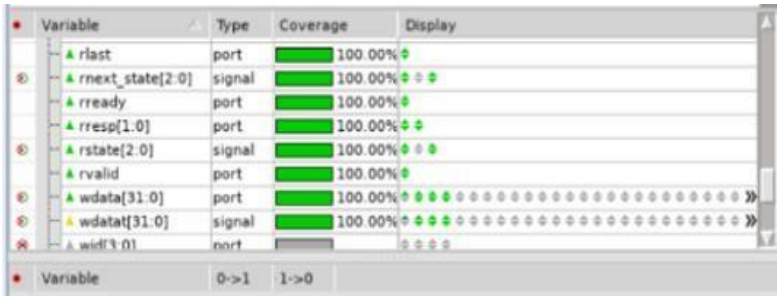

Figure 4: Code coverage results

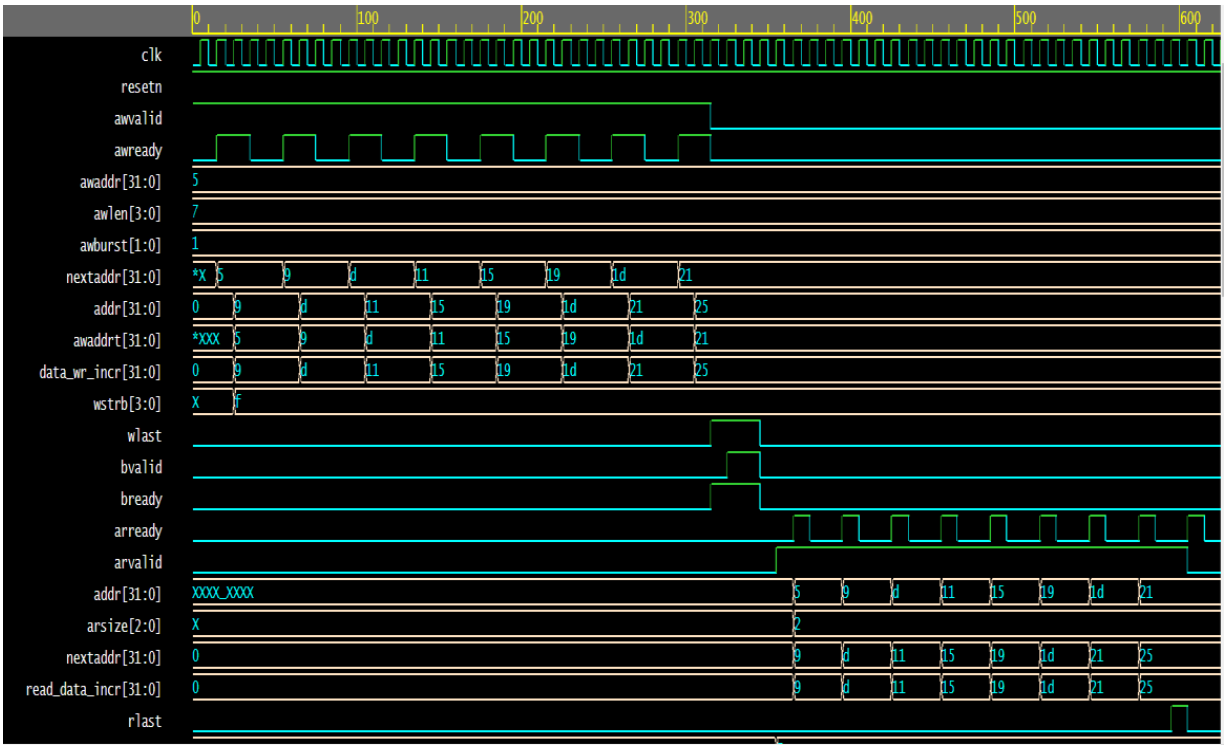

Figure 5: Simulation result of write and read operation for Increment Burst Type.

```
Startpoint: wlast (input port clocked by clk)
Endpoint: bstate_reg[0]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
axi_slave          35000                 saed14rvt_ss0p72vm40c

Point                                    Fanout      Cap     Trans    Derate     Incr       Path
-----------------------------------------------------------------------------------------------
clock clk (rise edge)                                                            0.00       0.00
clock network delay (ideal)                                                      0.00       0.00
input external delay                                                             1.20       1.20 r
wlast (in)                                                        7.00           0.00       1.20 r
wlast (net)                              4          0.82                         0.00       1.20 r
U116579/B2 (SAEDRVT14_ND3B_0P75)                                  7.00           0.00       1.20 r
U116579/X (SAEDRVT14_ND3B_0P75)                                   0.02           2.23       3.43 f
n31184 (net)                             2          0.34                         0.00       3.43 f
U132286/A (SAEDRVT14_INV_S_0P5)                                   0.02           0.00       3.44 f
U132286/X (SAEDRVT14_INV_S_0P5)                                   0.01           0.01       3.45 r
n31185 (net)                             1          0.18                         0.00       3.45 r
U132287/B (SAEDRVT14_AOI21_0P75)                                  0.01           0.00       3.45 r
U132287/X (SAEDRVT14_AOI21_0P75)                                  0.02           0.01       3.46 f
n929 (net)                               1          0.22                         0.00       3.46 f
bstate_reg[0]/D (SAEDRVT14_FDPRBQ_V2LP_0P5)                       0.02           0.00       3.47 f
data arrival time                                                                           3.47

clock clk (rise edge)                                                            4.00       4.00
clock network delay (ideal)                                                      0.00       4.00
clock uncertainty                                                               -0.40       3.60
bstate_reg[0]/CK (SAEDRVT14_FDPRBQ_V2LP_0P5)                                     0.00       3.60 r
library setup time                                                              -0.02       3.58
data required time                                                                          3.58
-----------------------------------------------------------------------------------------------
data required time                                                                          3.58
data arrival time                                                                          -3.47
-----------------------------------------------------------------------------------------------
slack (MET)                                                                                 0.12
```

Figure 6: Setup Analysis for Testcase-1

```
Startpoint: wlast (input port clocked by clk)
Endpoint: bstate_reg[1]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
axi_slave          35000                 saed14rvt_ss0p72vm40c

Point                                    Fanout      Cap     Trans    Derate     Incr       Path
-----------------------------------------------------------------------------------------------
clock clk (rise edge)                                                            0.00       0.00
clock network delay (ideal)                                                      0.00       0.00
input external delay                                                             1.20       1.20 f
wlast (in)                                                        7.00           0.00       1.20 f
wlast (net)                              5          0.82                         0.00       1.20 f
U116579/B2 (SAEDRVT14_ND3B_0P75)                                  7.00           0.00       1.20 f
U116579/X (SAEDRVT14_ND3B_0P75)                                   0.01           2.21       3.42 r
n31184 (net)                             2          0.33                         0.00       3.42 r
U116580/B (SAEDRVT14_OAI21_0P5)                                   0.01           0.00       3.42 r
U116580/X (SAEDRVT14_OAI21_0P5)                                   0.02           0.01       3.43 f
bnext_state[1] (net)                     1          0.22                         0.00       3.43 f
bstate_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_0P5)                       0.02           0.00       3.44 f
data arrival time                                                                           3.44

clock clk (rise edge)                                                            4.00       4.00
clock network delay (ideal)                                                      0.00       4.00
clock uncertainty                                                               -0.40       3.60
bstate_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_0P5)                                     0.00       3.60 r
library setup time                                                              -0.01       3.59
data required time                                                                          3.59
-----------------------------------------------------------------------------------------------
data required time                                                                          3.59
data arrival time                                                                          -3.44
-----------------------------------------------------------------------------------------------
slack (MET)                                                                                 0.15
```

Figure 7: Setup Analysis for Testcase-2

Figure 8: Hold Analysis for Testcase-1

```
Startpoint: wlast (input port clocked by clk)
Endpoint: bstate_reg[0]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
axi_slave          35000                 saed14rvt_ss0p72vm40c

Point                                    Fanout      Cap     Trans    Derate     Incr       Path
-----------------------------------------------------------------------------------------------
clock clk (rise edge)                                                            0.00       0.00
clock network delay (ideal)                                                      0.00       0.00
input external delay                                                             1.20       1.20 f
wlast (in)                                                        7.00           0.00       1.20 f
wlast (net)                              4          0.82                         0.00       1.20 f
U116579/B2 (SAEDRVT14_ND3B_0P75)                                  7.00           0.00       1.20 f
U116579/X (SAEDRVT14_ND3B_0P75)                                   0.01           2.21       3.42 r
n31184 (net)                             2          0.33                         0.00       3.42 r
U132286/A (SAEDRVT14_INV_S_0P5)                                   0.01           0.00       3.42 r
U132286/X (SAEDRVT14_INV_S_0P5)                                   0.00           0.01       3.43 f
n31185 (net)                             1          0.17                         0.00       3.43 f
U132287/B (SAEDRVT14_AOI21_0P75)                                  0.00           0.00       3.43 f
U132287/X (SAEDRVT14_AOI21_0P75)                                  0.02           0.00       3.44 r
n929 (net)                               1          0.20                         0.00       3.44 r
bstate_reg[0]/D (SAEDRVT14_FDPRBQ_V2LP_0P5)                       0.02           0.00       3.44 r
data arrival time                                                                           3.44

clock clk (rise edge)                                                            4.00       4.00
clock network delay (ideal)                                                      0.00       4.00
clock uncertainty                                                               -0.40       3.60
bstate_reg[0]/CK (SAEDRVT14_FDPRBQ_V2LP_0P5)                                     0.00       3.60 r
library setup time                                                              -0.02       3.58
data required time                                                                          3.58
-----------------------------------------------------------------------------------------------
data required time                                                                          3.58
data arrival time                                                                          -3.44
-----------------------------------------------------------------------------------------------
slack (MET)                                                                                 0.14
```

Figure 9: Hold Analysis for Testcase-2

```
Startpoint: wlast (input port clocked by clk)
Endpoint: bstate_reg[1]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
axi_slave          35000                 saed14rvt_ss0p72vm40c

Point                                    Fanout      Cap     Trans    Derate     Incr       Path
-----------------------------------------------------------------------------------------------
clock clk (rise edge)                                                            0.00       0.00
clock network delay (ideal)                                                      0.00       0.00
input external delay                                                             1.20       1.20 r
wlast (in)                                                        7.00           0.00       1.20 r
wlast (net)                              4          0.82                         0.00       1.20 r
U116579/B2 (SAEDRVT14_ND3B_0P75)                                  7.00           0.00       1.20 r
U116579/X (SAEDRVT14_ND3B_0P75)                                   0.02           2.23       3.43 f
n31184 (net)                             2          0.34                         0.00       3.43 f
U116580/B (SAEDRVT14_OAI21_0P5)                                   0.02           0.00       3.44 f
U116580/X (SAEDRVT14_OAI21_0P5)                                   0.02           0.01       3.45 r
bnext_state[1] (net)                     1          0.20                         0.00       3.45 r
bstate_reg[1]/D (SAEDRVT14_FDPRBQ_V2LP_0P5)                       0.02           0.00       3.46 r
data arrival time                                                                           3.46

clock clk (rise edge)                                                            4.00       4.00
clock network delay (ideal)                                                      0.00       4.00
clock uncertainty                                                               -0.40       3.60
bstate_reg[1]/CK (SAEDRVT14_FDPRBQ_V2LP_0P5)                                     0.00       3.60 r
library setup time                                                              -0.02       3.58
data required time                                                                          3.58
-----------------------------------------------------------------------------------------------
data required time                                                                          3.58
data arrival time                                                                          -3.46
-----------------------------------------------------------------------------------------------
slack (MET)                                                                                 0.12
```

14nm Technology		DATA ARRIVAL TIME	DATA REQUIRED TIME	SLACK	SLACK MET/ VIOLATED
AXI Protocol Test case 1	SETUP	-3.47s	3.58s	0.12s	MET
	HOLD	-3.44s	3.58s	0.14s	MET
AXI Protocol Test case 2	SETUP	-3.44s	3.59s	0.15s	MET
	HOLD	-3.46s	3.58s	0.12s	MET

Table I – Detail view of Setup and Hold Timing analysis.

CONCLUSIONS :

The write and read transactions from the registers, which are visible from the simulation results, the AXI protocol is validated. for the purpose of confirming the AXI interface between the slave and master devices. The UVM technique is used in the development of every reusable part of the testbench, including the sequencer, driver, monitor, scoreboard, agent, and so on. By examining the code coverage report and able to determine that 100% code coverage has been reached. The AXI Protocol has been designed and generated for the 14nm Technology for the synthesis process. As a result, the slack is met in the timing report from the proposed methodology. The Synopsys VCS tool is used for all simulation.

REFERENCES :

1. ARM, ”AMBA AXI™ Protocol Specification”.
2. Synopsys, VCS / VCSi User Guide Version 10.3 Available at, www.synopsys.com
3. “IEEE Standard for Universal Verification Methodology Language Reference Manual,” in IEEE Std 1800.2-2020 (Revision of IEEE Std 1800.2-2017) , vol., no., pp.1-458, 14 Sept. 2020, doi:10.1109/IEEESTD.2020.9195920.
4. V. Melikyan, S. Harutyunyan, A. Kirakosyan and T. Kaplanyan, ”UVM Verification IP for AXI,” 2021 IEEE East-West Design & Test Symposium (EWDTS),2021, pp.1-4, doi: 10.1109/EWDTS52692.2021.9580997.
5. Madhura M C, Bhagya, Deepika M, Manjushree R, Nisarga D, “Verification of Advanced Extensible Interface (AXI) Bus using UVM Methodology,” International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering. Vol. 9, Issue 7, July 2021,
6. Tuy Nguyen Tan, Phap Duong-Ngoc, Thang Xuan Pham, and Hanho Lee,” Novel Performance Evaluation Approach of AMBA AXI-Based SoC Design,” 2021 18th International SoC Design Conference (ISOCC),IEEE, DOI: 10.1109/ISOCC53507.2021.9613920
7. N. Gaikwad and V. N. Patil,” Verification of AMBA AXI On-Chip Communication Protocol,” 2018 Fourth International Conference on Computing Communication Control and Automation (ICCUBEA), 2018, pp. 1-5, doi: 10.1109/ICCUBEA.2018.8697587.
8. Venkatesh.T, Dr.Narendra C.P, " Development of VIP for AMBA AXI v4.0 Protocol using UVM," International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE) Vol 7, Issue 7, July 2021.
9. Hardi Sangani, Dr. Usha Mehta, " UVM based Verification of Read and Write Transactions in AXI4-Lite Protocol," 2022 IEEE Region 10 Symposium (TENSYMP) | 978-1-6654-6658-5, 2022 IEEE, DOI: 10.1109/TENSYMP54529.2022.9864552.
10. Tanupriya A G , Kiran V, “Testing of AMBA AXI Protocol,” International Journal of Research and Review Vol. 9; Issue: 11; November 2022, DOI: https://doi.org/10.52403/ijrr.20221114.
11. Bijal Thakkar and V Jayashree. " Verification of driver logic using AMBA AXI UVM ". International Journal of VLSI design & Communication Systems (VLSICS) Vol.9, No.3, June 2018.
12. Mr. Mukesh Kumar Yadav, Dr. R.K.Paliwal, Dr. K.C.Mahajan, " AXI Interface with a Multiple Master and Slave through Interconnect," International Journal of Advanced Research in Computer and Communication Engineering Vol. 7, Issue 10, October 2018.
13. Murali .M, Umadevi. S, Sakthivel.S.M. " Verification IP for AMBA AXI Protocol using System Verilog" International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 17 (2017) pp. 6534-6541
14. M Prasanna Deepu, Prof. R. Dhanabal, " Validation of Transactions in AXI Protocol using System Verilog," 2017 IEEE.
15. P. Naveen Kalyan, K. Jaya Swaroop. " AMBA-AXI protocol verification by using UVM", International Journal of Electronics and Communication Engineering and Technology (IJECET) Volume 7, Issue 4, July-August 2016, pp. 76–84, Article ID: IJECET_07_04_009.