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DESIGN AND REALIZATION OF BARREL SHIFTER USING FPGA

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ABSTRACT :

A barrel shifter is a digital circuit that can be used to shift the required number of bits in required direction in one clock cycle. It is used to perform operations like logical left shift, logical right shift, rotate left shift and rotate right shift. Barrel shifters are utilized for bitwise operations like encryption/decryption, enhancing encryption security via circular shifts. It is also used in digital signal processing employed in FIR filter implementations for efficient coefficient shifting based on filter order. In this paper we have designed the 1-bit, 4-bit, 8-bit and 16-bit barrel shifters, obtained the simulations of the same using Xilinx Integrated Software Environment (ISE) project navigator and ISE simulator (Isim). The results are compared for the barrel shifters in terms of delay, gate count, scalability, and performance. The designed barrel shifter can be used as IP core for developing 32-bit, 64-bit, and beyond architectures for diverse applications.

Keywords: Barrel Shifter, FPGA, Cryptography, Encryption, Decryption, ALU, Verilog HDL

1. Introduction :

Barrel shifters are handy tools in cryptography because they can quickly and efficiently move bits around in binary data. This ability is crucial for encryption and decryption processes where bits need to be rearranged securely. For example, in encryption, a barrel shifter can be used to perform circular shifts on binary values, making it harder for unauthorized parties to understand the data [1]. Similarly, in decryption, barrel shifters aid in reversing these operations to reconstruct the original information. Barrel shifters are great for shifting and rotating data [2]. Barrel shifters are crucial in arithmetic operations, acting as logic circuits to manipulate data efficiently. Barrel shifters are major elementary circuit in Arithmetic and Logical Unit of digital signal processing and all other processor applications [3]. The Barrel shifter is used for logical shift left, logical right, rotate right and rotate left operations. The architecture of barrel shifter is realized by using 2x1, 4x1, 8x1 and 16x1 multiplexer circuits [4]. The Shifting and rotating data play vital roles in various applications such as numerical calculations, variable length coding, and bit ordering. Barrel shifters excel in swiftly shifting or rotating data within a single cycle, utilizing select lines to determine the amount of shift required [5]. These shifters can be constructed using multiplexer trees for efficient design [6]. In this paper four different barrel shifters are designed by using Verilog Hardware Description Language and compared their performances.

2. Design Analysis :

The algorithm for barrel shifter is shown in Figure 1. In accordance with the selection line, a barrel shifter executes four different shift operations. The different operations are logical left shift, logical right shift, rotate left shift and rotate right shift [7]. The algorithm shifts logically left when the selection line is 00 and logically right when it is 01. Furthermore, when the selection line is 10 it rotates left and when it is 11, it rotates right [8]. The barrel shifter performs different shift operations as per the given specifications and application. The selection of type of shifting is done in accordance with the selection lines given by the designer. The algorithm is analyzed for different types of shifters to provide the best design analysis using Verilog HDL. The design of barrel shifter is done for 1-bit, 4-bit, 8-bit and 16-bit sizes for four different data inputs a0, a1, a2, a3. The MSB is a3 and LSB is a0. The operation of logical left shift, logical right shift, rotate left shift and rotate right shift are described below.

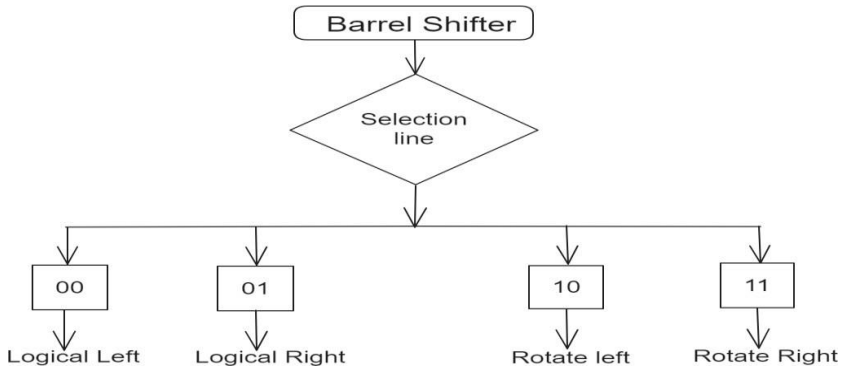


Figure 1: Algorithm for Barrel Shifter

Operation of Logical Left Shift:

Logical left shift is a bit-wise operation [9]. The operation of logical left shift is shown in Figure 2. As illustrated in the given example, the MSB (Most Significant Bits) is eliminated, and each bit is shifted left towards MSB position. The last empty position in the LSB (Least Significant Bit) is filled with zero.

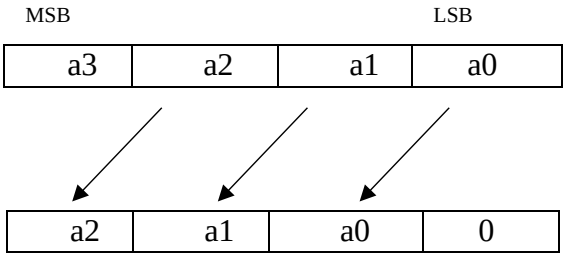


Figure 2: Operation of Logical Left Shift

Operation of Logical Right Shift:

Logical right shift is a bit-wise operation. The operation of logical left shift is shown in Figure 3. As illustrated in the given example, the LSB (Least Significant Bits) is eliminated, and each bit is shifted left towards LSB position. The last empty position in the MSB is filled with zero.

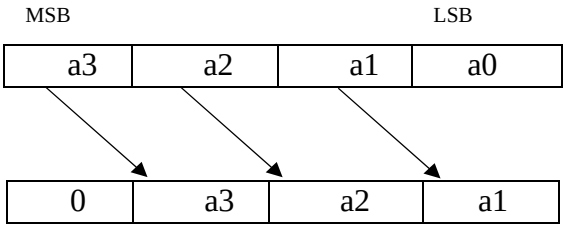


Figure 3: Operation of Logical Right Shift

Operation of Rotate Left Shift:

Rotate left shift is a bit-wise operation. The operation of rotate left shift is shown in Figure 4. As illustrated in the given example, each bit is shifted left towards MSB position and the MSB is relocated to LSB.

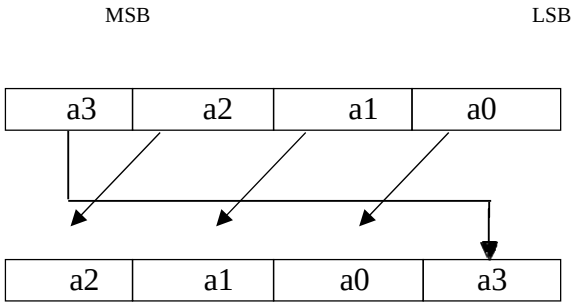


Figure 4: Operation of Rotate Left Shift

Operation of Rotate Right Shift:

Rotate right shift is a bit-wise operation. The operation of rotate right shift is shown in Figure 5. As illustrated in the given example, each bit is shifted right towards LSB position and the LSB is relocated to MSB.

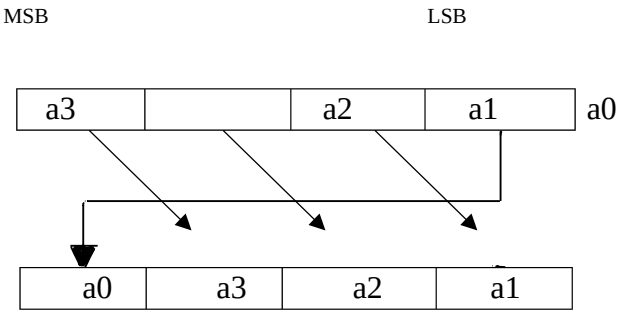


Figure 5: Operation of Rotate Right Shift

3. Implementation

The barrel shifter for different data sizes of 1, 4, 8, 16-bit inputs are designed by using 4x1 multiplexer [10]. By applying the various test vectors as inputs to the shifters, encompassing different data values and shift amounts. The synthesis of barrel shifters was completed utilizing XST and Verilog HDL [11]. Analyzed the simulation outputs to verify the functionality of each barrel shifter for all supported operations. All these designs are implemented on FPGA hardware as shown in Table 1[12].

Table 1: FPGA Specifications

Hardware Elements	**Specifications**
Family	Spartan 3
Device	XC3S400
Package	FG320
Speed	-5
Synthesis Tool	XST Verilog
Simulator	ISim Verilog

The FPGA design flow is shown in Figure 6. The synthesis results of 1-bit barrel shifter, 4-bit barrel shifter, 8-bit barrel shifter and 16-bit barrel shifter are shown in Figure 7 to Figure 14.

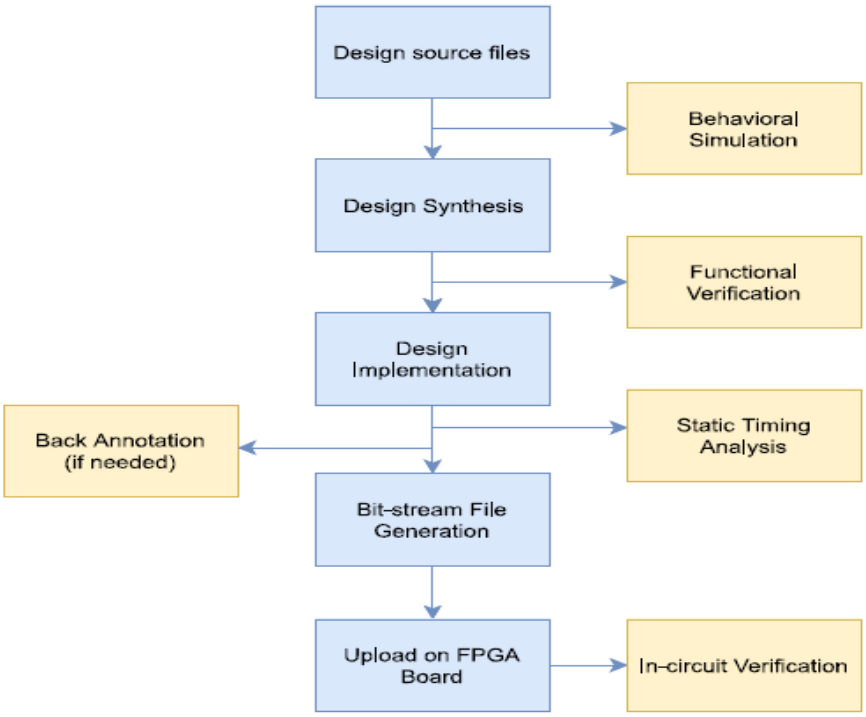


Figure 6: FPGA Design Flow

1-Bit Barrel Shifter

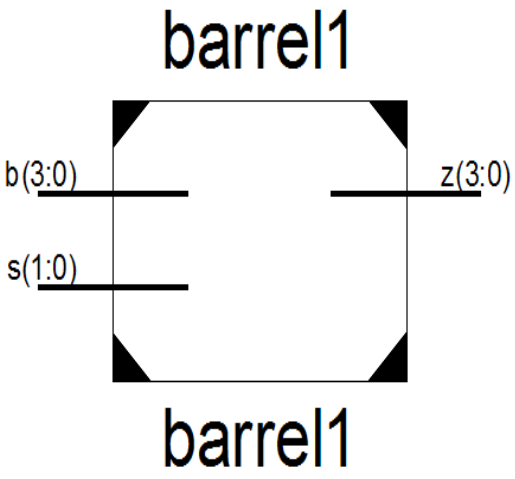


Figure 7: Block diagram of 1-Bit Barrel Shifter.

4-Bit Barrel Shifter

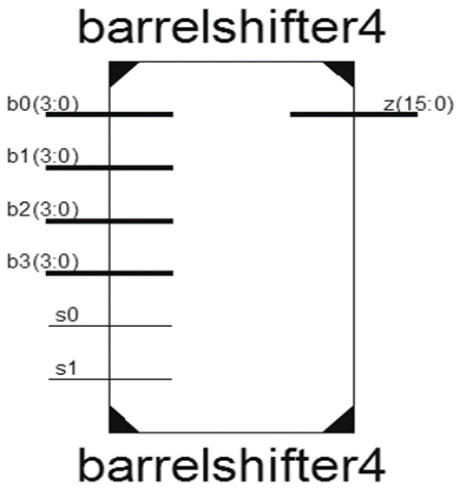


Figure 8: Block diagram of 4-Bit Barrel Shifter

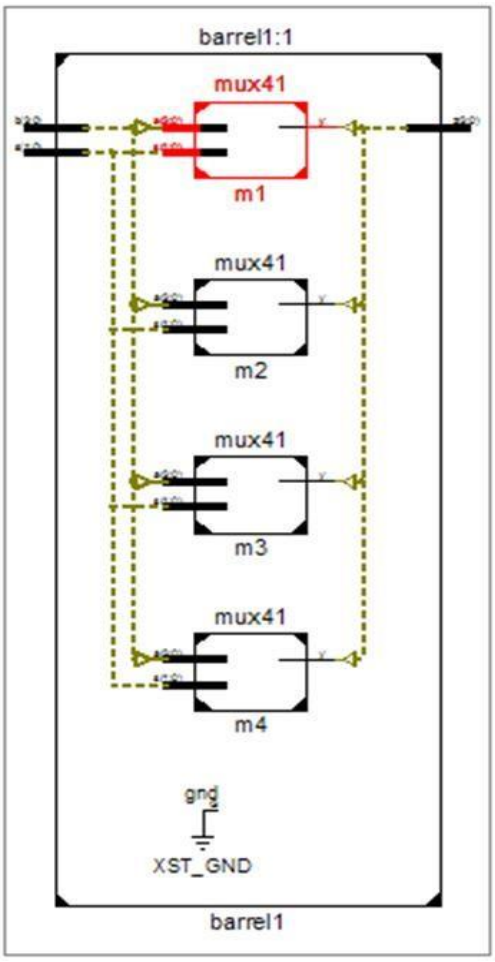


Figure 9*:* RTL Schematic of 1-Bit Barrel Shifter

8-Bit Barrel Shifter

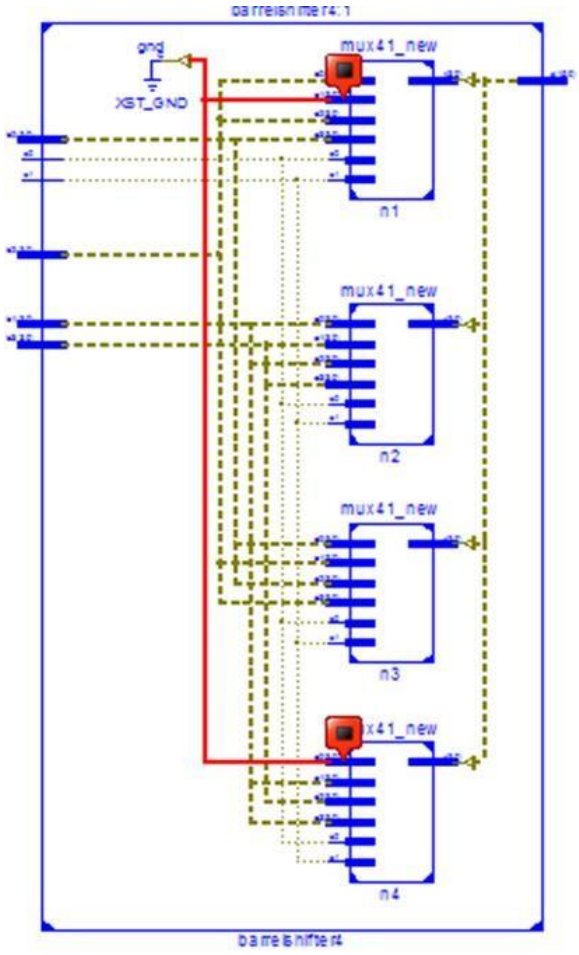


Figure 10: RTL Schematic of 4-BitBarrel Shifter

16-Bit Barrel Shifter

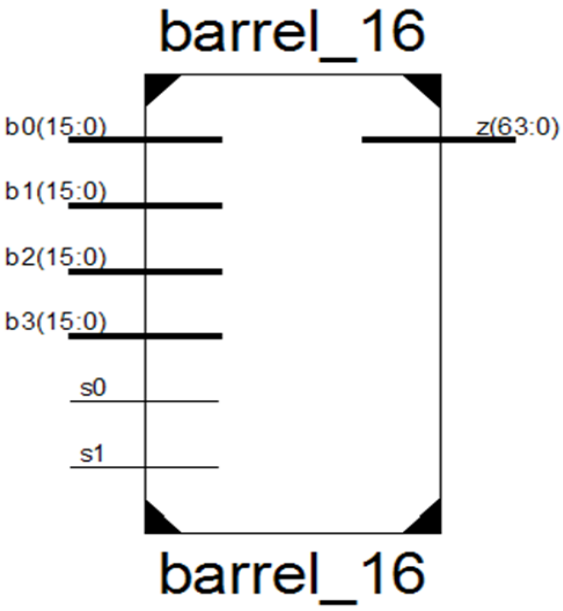


Figure 11: Block diagram of 8-Bit Barrel Shifter.

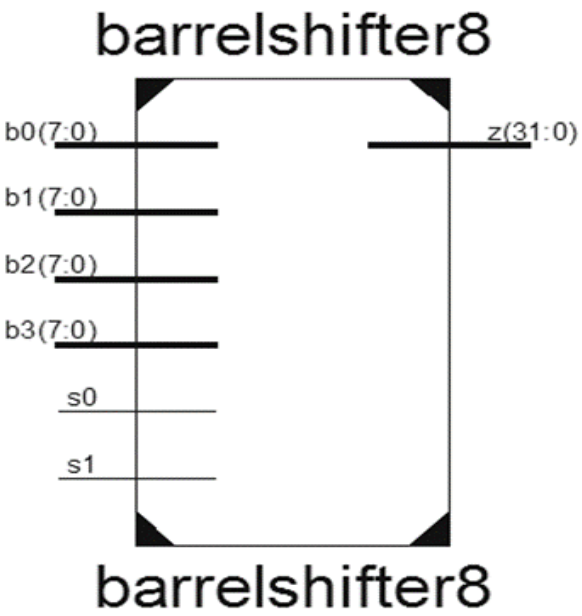


Figure 12: Block diagram of 16-Bit Barrel Shifter

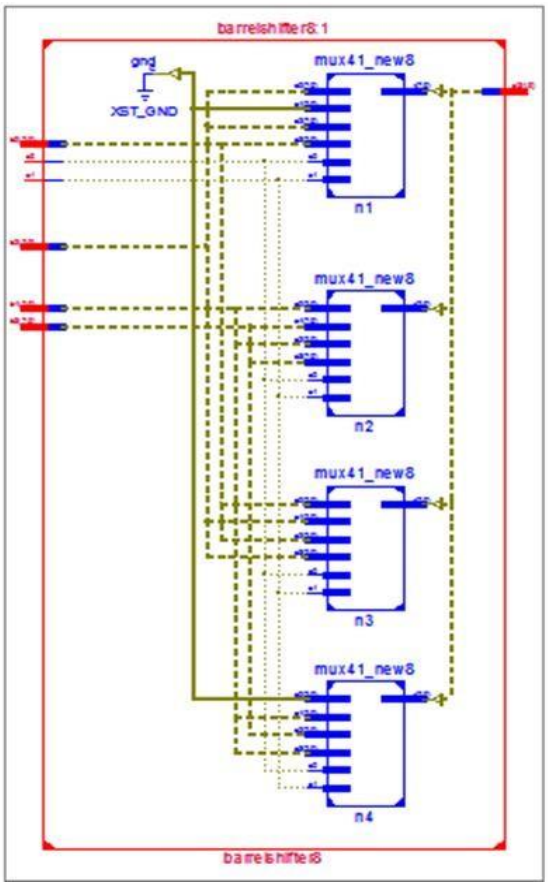


Figure 13: RTL Schematic of 8-Bit Barrel Shifter

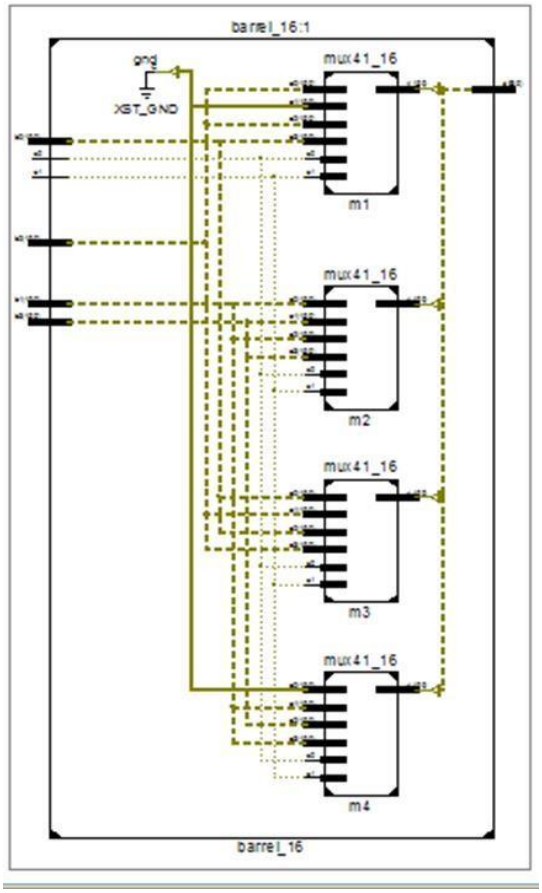


Figure 14: RTL Schematic of 16-Bit BarrelShifter

Simulation Results

1-Bit Barrel Shifter:

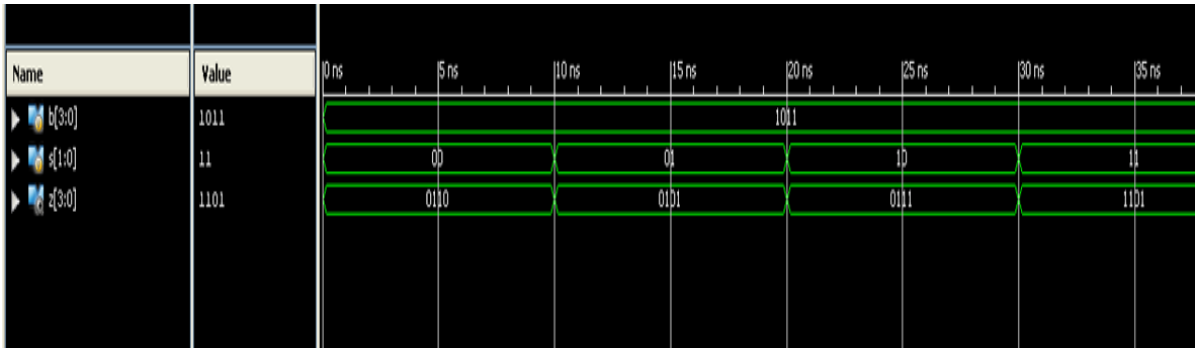


Figure 15: Simulation results of 1-Bit BarrelShifter

Selection line	Operation	
00	Logical Left Shift	I/P: 1 0 1 1 O/P: 0 1 1 0

01	Logical Right Shift	I/P: 1 0 1 1 O/P: 0 1 0 1
10	Rotate Left Shift	I/P: 1 0 1 1 O/P: 0 1 1 1
11	Rotate Right Shift	I/P: 1 0 1 1 O/P: 1 1 0 1

4-Bit Barrel Shifter:

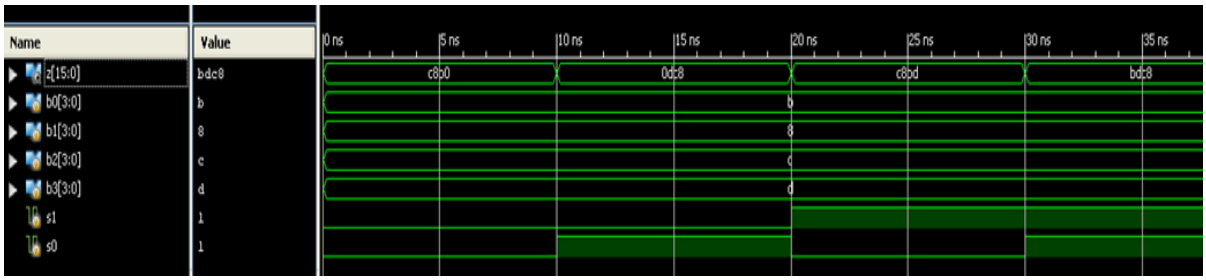


Figure 16: Simulation results of 4-Bit BarrelShifter

Selection Line	Operation	
00	Logical Left Shift	I/P: d c 8 b O/P: c 8 b 0
01	Logical Right Shift	I/P: d c 8 b O/P: 0 b c 8
10	Rotate Left Shift	I/P: d c 8 b O/P: c 8 b d
11	Rotate Right Shift	I/P: d c 8 b O/P: b d c 8

8-bit Barrel Shifter:

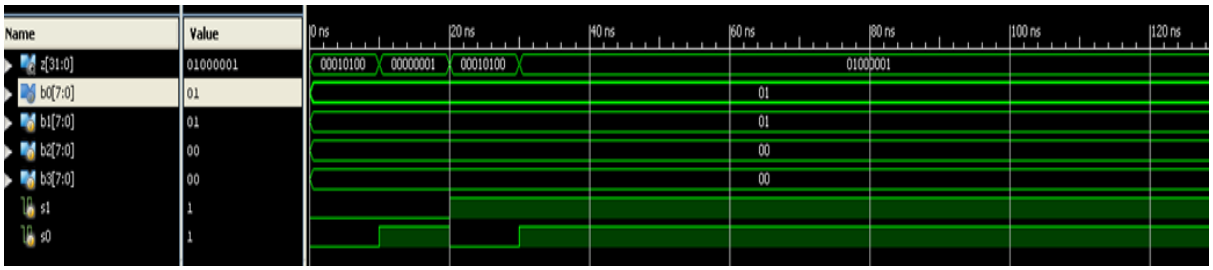


Figure 17: Simulation Results of 8-bit Barrel Shifter

Selection line	Operation	
00	Logical Left Shift	I/P: 00 00 01 01 O/P: 00 01 01 00
001	Logical Right Shift	I/P: 00 00 01 01 O/P: 00 00 00 01
10	Rotate Left Shift	I/P: 00 00 01 01 O/P: 00 01 01 00
11	Rotate Right Shift	I/P: 00 00 01 01 O/P: 01 00 00 01

16-Bit Barrel Shifter:

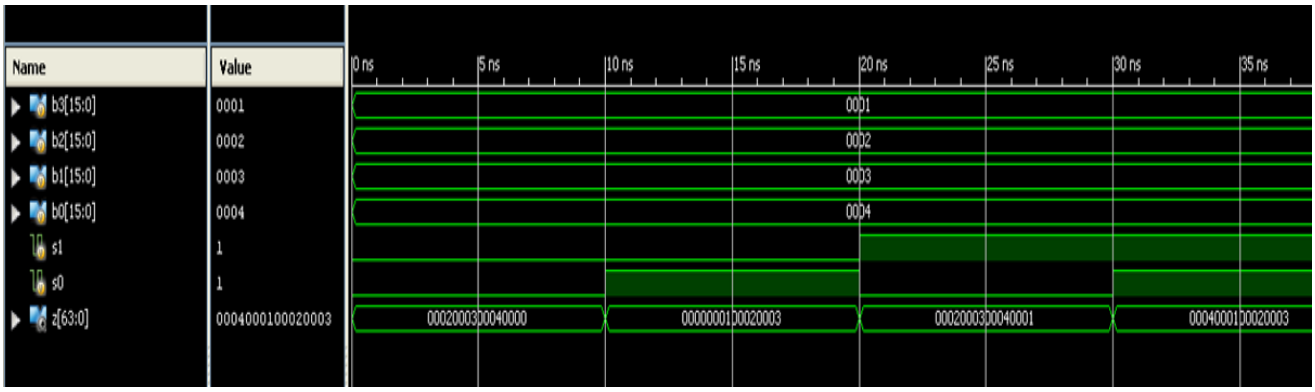


Figure 18: Simulation results of 16-Bit BarrelShifter

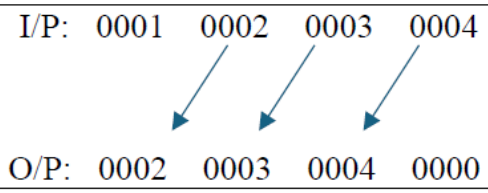
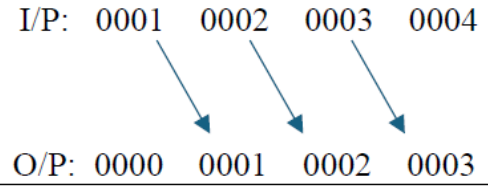
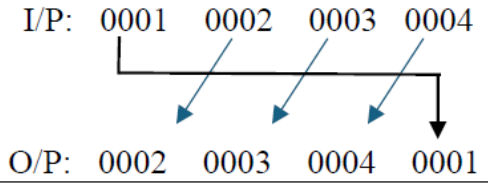
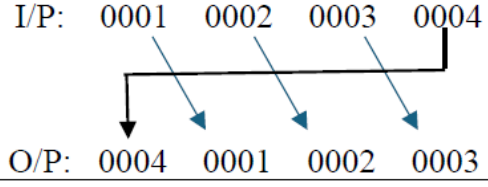
Selection line	Operation	
00	Logical Left Shift	
01	Logical Right Shift	
10	Rotate Left Shift	
11	Rotate Right Shift	

Table 2: Device Utilization Summary

n-bit Barrel Shifter	Number of Slices	Number of LUTs	Number of IOBs
1-bit	2	4	10
4-bit	9	16	34
8-bit	18	32	66
16-bit	37	64	130

From above comparison table 2, it can conclude that the total number of LUTs = n*4 The number of IOBs = (number of LUTs * 2) + 2

Table 3: Summary of Time delays for Barrel shifters

N-bit Barrel Shifter	Total time delay (ns)
1-bit	7.858
4-bit	8.130
8-bit	8.654
16-bit	8.810

4. Conclusions :

This paper presented the design and implementation of 1, 4, 8, and 16-bit barrel shifters using Verilog. The designs utilized 4:1 multiplexer to achieve efficient shifting operations. The key finding of this work is the exchange between hardware usage and performance. As the barrel shifter size increases (1-bit to 16-bit), the number of slices, LUTs, and IOBs required also increases. This is expected to be due to the growing complexity of the multiplexer. However, the timing delay for all barrel shifters remains almost constant, ranging from 7.858ns to 8.810ns. To process lot of data at once and have enough space on the chip, a bigger shifter might be better. But if space is limited, a smaller shifter can be chosen. In the future, it will be used further to design 32-bit ,64-bit barrel shifters that use resources more efficiently or with increased performance or low power consumption.

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