International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

THREE-PHASE SYMMETRICAL FAULT ANALYSIS AND IMPROVEMENT IN THE POWER SYSTEM PARAMETERS USING INTERLINE POWER FLOW CONTROLLER ALONG WITH FOPID AND PR CONTROLLER IN AN IEEE – 14 BUS SYSTEM

Dr.N. Ashokkumar[1], Dr.K. Anisha[2] ,R.S. Charrusmitha[3]

[1]Assistant Professor, Department of Electrical and Electronics Engineering, SCSVMV UNIVERSITY, Kanchipuram, India.
[2]Assistant Professor, Department of Electrical and Electronics Engineering, SCSVMV UNIVERSITY, Kanchipuram, India.
[3]PG Student, Department of Electrical and Electronics Engineering, SCSVMV UNIVERSITY, Kanchipuram, India

ABSTRACT :

A power system represents an interconnected network, where the generation, transmission, and distribution of electrical energy take place. They are complex systems constituting various components like synchronous generators, motors, transformers, circuit breakers, etc. There are various types of faults, Open Circuit fault, ground fault, symmetrical fault, and Asymmetrical fault. Types of faults are 3-phase fault, L-L fault Short Circuit fault, LL-G fault, and 3-phase Open Circuit fault. Symmetrical fault works severely though, but occurrence is quite rare. During this fault, all the 3-phase of the input are short-circuited with each other, or all of them are grounded. During this fault, a huge Short Circuit current will flow from all 3-phase to the ground. This will cause loss of equipment due to high current passing through it causing damage. It could burn insulators and wires of motors and transformers. Symmetrical Fault Analysis is planned to be conducted on Bus 13 (close to Load 1), on the test system (IEEE 14-Bus System). The study of the system and tabulation of the parameters during fault is done. Then, an Interline Power Flow Controller (IPFC), one of the FACTS devices, is suitably connected to the Power System to create betterment in the result, by aiding the improvement in the system stability. This fault analysis is crucial for protective device coordination and aids in determining voltage and current during fault conditions. It is versatile – as it provides critical information about fault locations, their impact on the system, and management of faults, thus ensuring efficient and stable operation of the system.

Keywords: Fault Analysis, Symmetrical fault, Power system protection, IPFC controller, FOPID controller ,PR controller

1. INTRODUCTION :

The reason for choosing this particular fault for our analysis is because symmetrical fault is the most severe one, although its occurrence is not very common, leading to highest fault currents, causing the maximum damage. This fault, if not analyzed properly and timely action if not taken, may even result in cascaded fault and result in blackout, thus causing hardship to critical loads.

II. METHODOLOGY ADOPTED :

The Symmetrical Fault was simulated on Bus 1(close to generator 4), on the test system (IEEE-14 Bus System). The transmission lines 9 and 10 are connected to this bus. The generator 4 is also connected to the shorted Bus 1. So, these two transmission lines and generator 4 will be facing the maximum effect of the fault created. The symmetrical fault is induced at 2 secs, in Bus 1, of the given test system. The fault is set to stay for 200 milliseconds. The fault current in Bus 1, is plotted. Also, the voltage versus time graphs are plotted, in bus 1 and buses 1 to 5 (buses closer to bus 1), and in bus 13 (bus away from bus 1), prior fault, during fault, and post fault. Observing these, we get to understand how the Power system behaves once it is struck with three three-phase short circuit symmetrical faults. It is also found that the whole test system is affected by one fault being simulated at bus 1. The reason for this is that the power system is an interconnected power system, and the fault gets transmitted and affects the whole system. Thus, we can clearly understand the need for detecting the fault quickly and rectifying it soon, to protect all the equipment and the system itself also as a whole.

This effort deals with the design, analysis, and simulation of Open-loop and Closed-loop IPFC-14 bus system with FOPID (Fractional Order Proportional Integral Derivative) & PR (Proportional Resonant) controller and outcomes are presented. (i) Open loop 14 bus IPFC system with disturbance is simulated (ii) Closed loop 14 bus IPFC system with FOPID is simulated and (iii) Closed loop 14 bus IPFC system with PR is simulated.

The consequences are related in terms of time-domain parameters like rise-time, peak-time, settling time, and steady-state error. The consequence denotes the superior performance of the closed-loop IPFC-14bus system with a PR controller. This work proposes a closed-loop IEEE 14-bus system incorporating IPFC with PR/FOPID control.

III TOOL USED – ETAP

In this work, we have used ETAP [Electrical Transient and Analysis Program], for simulation purposes. This software was chosen because it provides a wide range of tools specifically designed for power system analysis, including detailed short circuit analysis features tailored for three-phase systems. These comprehensive capabilities help in accurate simulation. It is known to provide reliable results for short-circuit system fault analysis. Its automation capabilities streamline the analysis process, reducing the time required to perform complex calculations and simulations. This software typically provides comprehensive reporting features, allowing engineers to generate detailed reports and documentation of the short-circuit analysis, which would be crucial for decision-making requirements.

IV SIMULATION RESULTS

CLOSED-LOOP 14-BUS IPFC SYSTEM WITH FOPID &PR

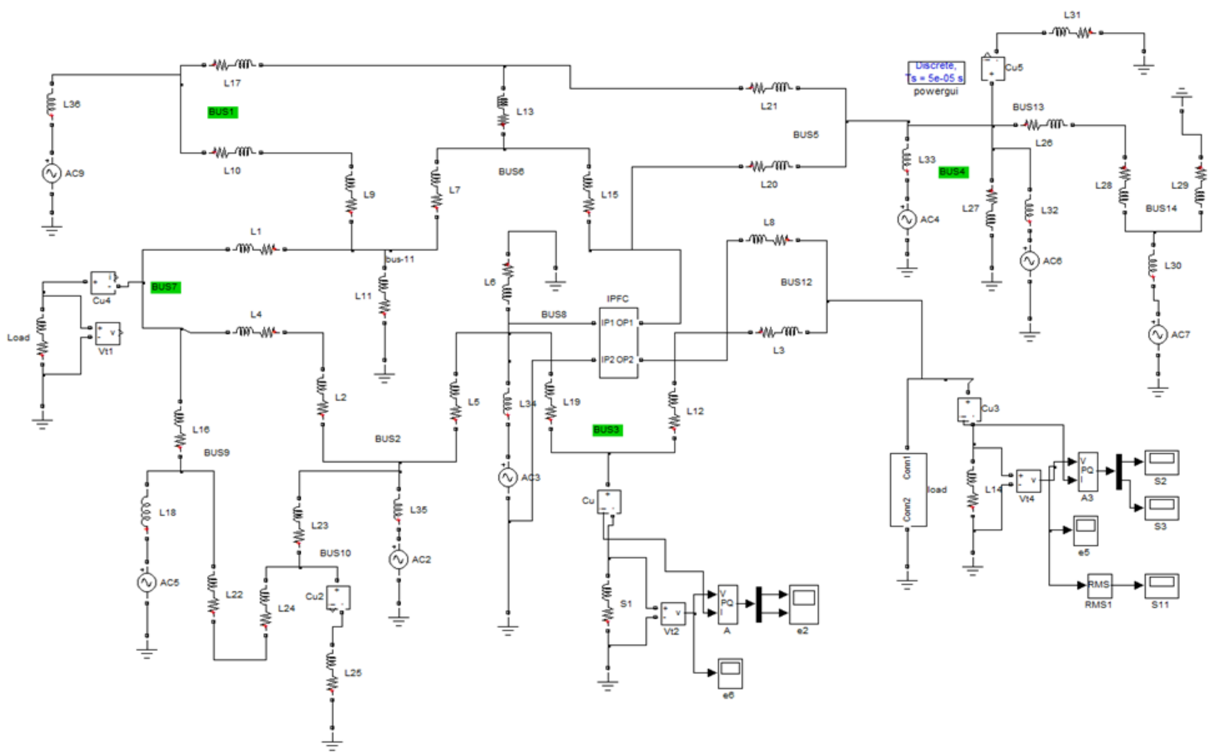


Fig 1. CIRCUIT MODEL OF 14-BUS IPFC SYSTEM WITH LOAD DISTURBANCE

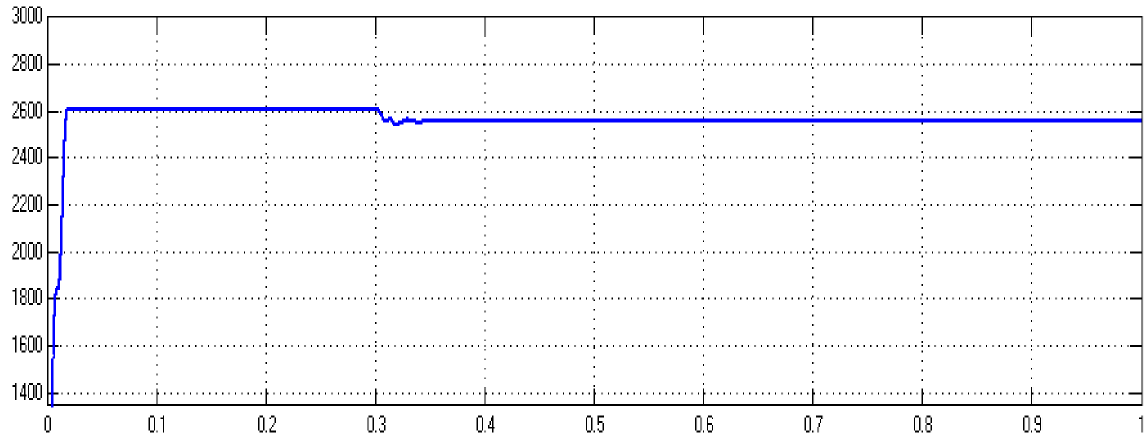


Fig.2. RMS VOLTAGE AT BUS-12 WITH LOAD DISTURBANCE

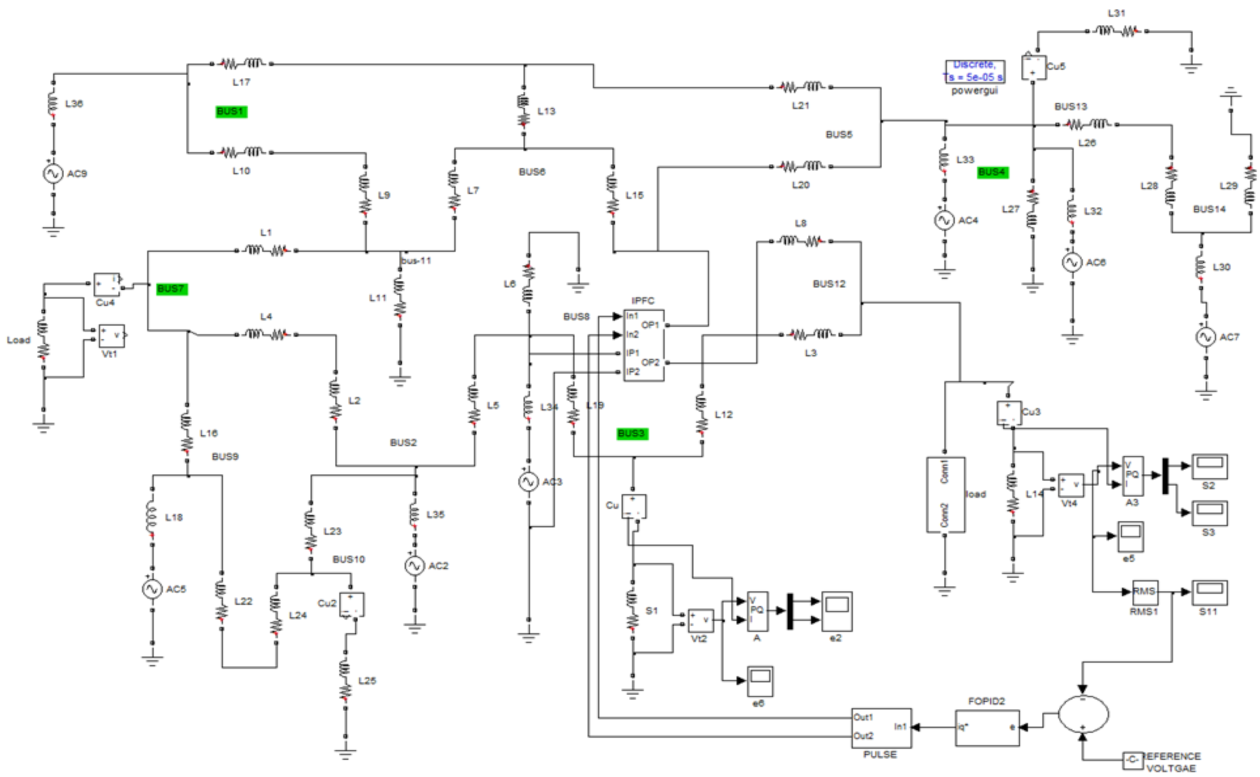
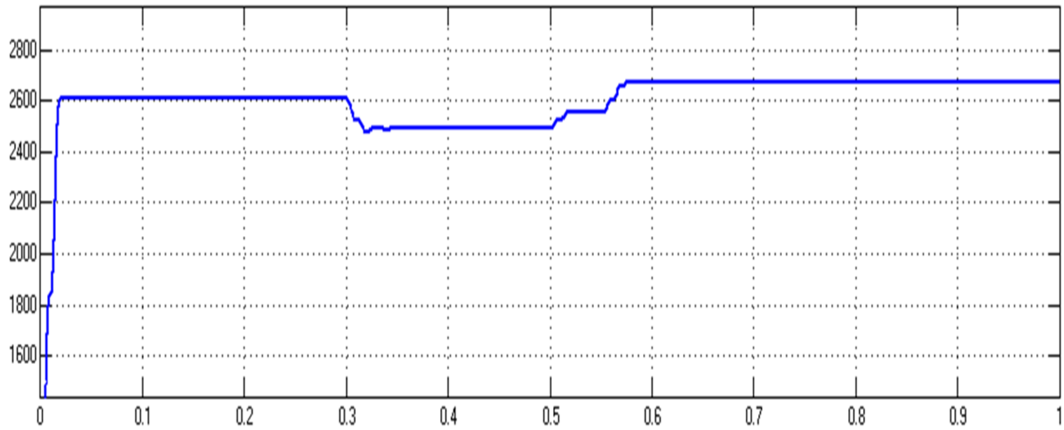


Fig.3. CLOSED LOOP 14-BUS IPFC SYSTEM WITH FOPID CONTROLLER



Fig,4, RMS VOLTAGE AT BUS-12 WITH FOPID CONTROLLER

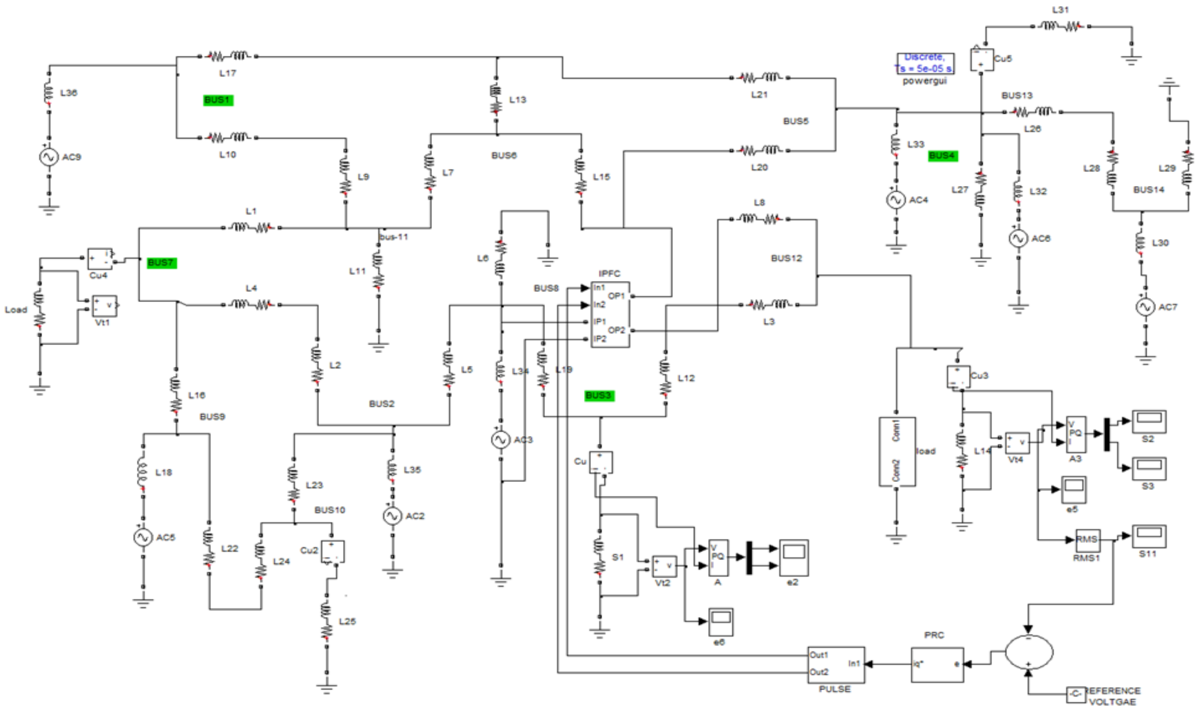


Fig.5. CLOSED LOOP 14-BUS IPFC SYSTEM WITH PR CONTROLLER

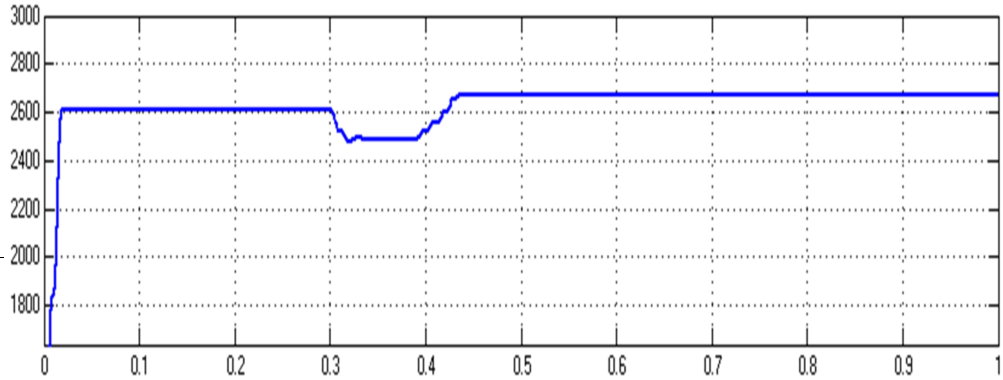


Fig.6. RMS VOLTAGE AT BUS-12 WITH PR CONTROLLER

Controller	Rise time (s)	Peak time (s)	Settling time (s)	Steady state error (V)
FOPID	0.32	0.41	0.57	1.85
PRC	0.31	0.37	0.43	1.17

Fig.7. COMPARISON OF TIME DOMAIN PARAMETERS

CONCLUSION :

Thus a Three Phase Symmetrical Fault Analysis was done on an IEEE 14 bus system with IPFC. By using PR, Rise time is reduced from 0.32Sec to 0.31Sec, Peak time is reduced from 0.41Sec to 0.37Sec, Settling time is reduced from 0.57Sec to 0.43Sec, Steady state error is reduced from 1.85V to 1.17V. Hence, the outcome represents that the Closed-loop IPFC-14 bus system with PR is superior to the Closed-loop IPFC-14 bus system with a FOPID controller.

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