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Carbon Nanotube Field Effect Transistor Technology for Power Reduction

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ABSTRACT

CMOS is the preferred technology choice for silicon-based high-performance digital circuits. Although silicon-based technology continues to expand and explore materials and models for future technologies. Carbon nanotube field-effect transistors (CNTFET) use carbon nanotubes to swap silicon as the channel material. Here 2X1MUX and 4X1MUX are used and compared with CMOS technology. When working with CNTFETs, you will notice that the change in voltage will affect the leakage current and change the process negatively, while the supply voltage will affect the performance of the generator. Use the cadence virtuoso tool for simulation. For CNTFET transistors, periodic analysis shows that the best CNT diameter to provide high power performance for high-speed digital applications is around 1 nm. CNTFETs have the potential to increase efficiency and provide good results.

Index Terms: carbon nanotube field-effect transistor (CNTFET), power consumption, Leakage current

I. INTRODUCTION

New technologies require faster processes, smaller connections and lower power consumption. Technological advancements such as 5G networks are advancing to improve smartphone battery life, spectrum efficiency, and more. One solution is the use of carbon nanotube field-effect transistors (CNTFETs).

CNTFET is a nanoscale device that provides low voltage with high efficiency and high power density. CNTFET uses carbon nanotubes (CNTs) between the surface and drain of the MOSFET structure instead of the silicon material used in metal oxide semiconductor field effect transistors (MOSFETs). This makes the carrier current stronger, allowing the CNTFET to provide better current driving.

Like MOSFETs, CNTFETs have three components: source, gate, and drain. When the gate is open, current is transferred from source to drain via the semiconductor carbon nanotube channel. The edge between the source and gate is too heavy to provide minimal protection. CNTFETs have very reliable I-V and switching characteristics.

The main features of CNTFET are:

Since carbon nanotubes are single-sided, they contain a small amount of dust. This feature enables the device to operate ballistically.

All chemical goods are flooded and steady in the CNT. So there is no essential for suspicious passivation of the edge among the nanotube channel and the gate dielectric.

Metal-Nanotube contact Schottky barrier represents the dynamic switching section.

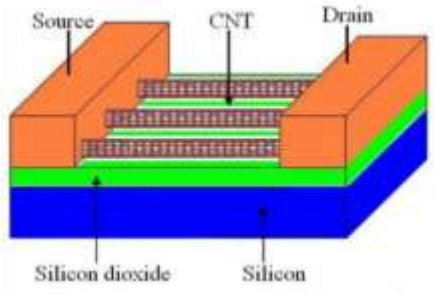

Fig.1:The structure of a carbon nanotube field-effect transistor

As new technology advances, integration requires high performance, low power consumption and small size. Transistors have been reduced in size to comply with Moore's Law, but there are also some disadvantages such as direct connection due to the effect of short channels and increased gate leakage current. CNTFET addresses this deficiency.

II. BACKGROUND

Silicon technology continues to evolve, and the path forward in line with Moore's Law faces many challenges, hurdles, and hurdles. Meanwhile, equipment, technology and circuit scientists are exploring other ways to leverage Moore's Law for the future of the semiconductor industry. Efforts are currently being made to develop flexible electronic devices (such as III-V compound semiconductors) using organic compounds and weak methods to increase carrier mobility. At the same time, new one-dimensional models are being investigated. Although many challenges remain, carbon nanotubes, due to their better portability, have emerged as potential candidates to help advance silicon technology in the post-2015 era. Therefore, Carbon Nanotube Field Effect Transistors (CNFETs) enable research in the device and field in the circuit/system.

The role of diameter and electrical properties in noise and voltage oscillation of CNFET-based digital circuits has been examined. was evaluated meticulously. DC simulations. However, a periodic analysis is required to evaluate the economic performance of CNFET-based digital logic.

In this article, we will demonstrate the role of diameter and performance of digital CNTFET circuits and evaluate the role of packing speed in the fabrication of transistor CNTFETs.

Higher drive current under the same extreme drive voltage, CNTFET can provide than Si MOSFET. CNTFET has higher conductivity compared to MOSFET. The average carrier speed in CNTFET is higher than that in MOSFET. Owing to the large mean free path, carriers in CNTFETs can be considered close to conduction. CNTFETs have a better switching angle compared to Si-MOSFETs.

III. PROPOSED DESIGNS

In this paper proposed the implementation of multiplexer(MUX) with the benefit of cadence virtuoso software. A multiplexer (or MUX) is a device that selects one of many analog or digital input signals and sends the selected message onto a line. In a multiplexer with 2^n inputs and n select lines that select the input line to the output. Multiplexers are often used to growth the amount of data that can be sent over a network in a given time and bandwidth. Multiplexers are also known as data selectors.

A.2X1 MULTIPLEXER

The 2-to-1 multiplexer has a Boolean equation; where A and B are two inputs, Input selector is S and Z is the output:

$$OUT = (I_0.\overline{S}) + (I_1.S)$$

Table 1-Truth table of 2x1MUX

Input(S)	Output
0	I_0
1	I_1

This truth table shows that when S=0 then Z=A but when S=1 then Z=B. A straightforward realization of this 2-to-1 multiplexer would need 2 AND gates, an OR gate, and a NOT gate.

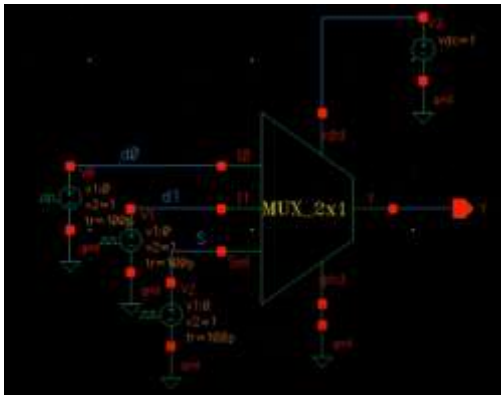

Figure 2: Schematic of 2X1 MUX

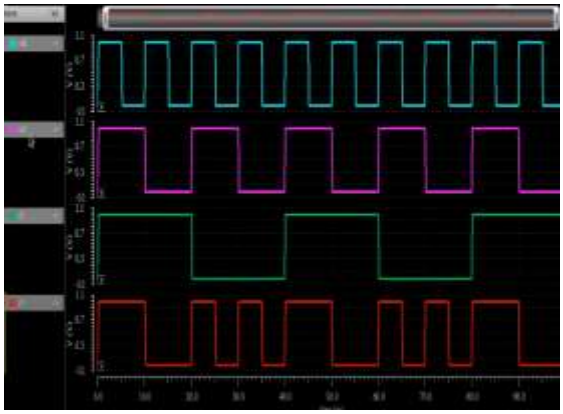

Figure 3:Timing Diagram of 4X1 MUX

B.4X1 MULTIPLEXER

The Boolean equation for a 4-to-1 multiplexer is:

$$F = (I_0.\overline{S_0}.\overline{S_1}) + (I_1.S_0.\overline{S_1}) + (I_2.\overline{S_0}.S_1) + (I_3.S_0.S_1)$$

Where

I_0, I_1, I_2, I_3 = Input

$S_0.S_1$ = selection line

Table 2-Truth table of 4x1MUX

Input($S_0.S_1$)	Output
00	I_0
01	I_1
10	I_2
11	I_3

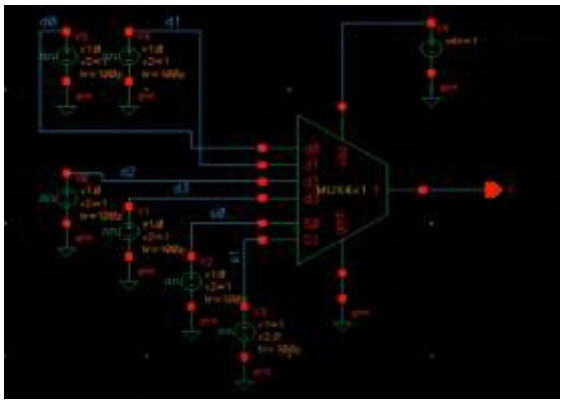

Figure 4:Schmatic of 4X1 MUX.

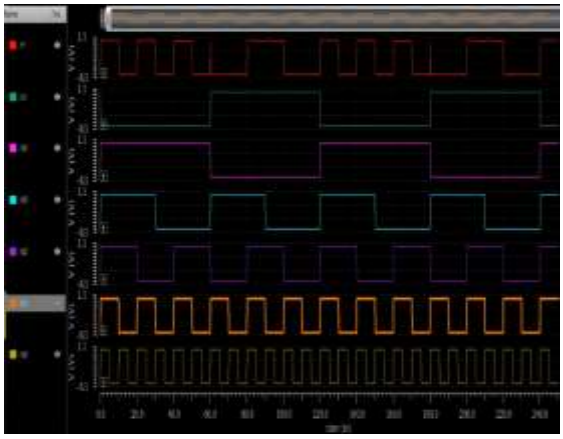

Figure 4:Timing Diagram of4x1 MUX.

The result is better by using CNTFET comparison to CMOS.

IV. SIMULATION RESULTS

A. *Simulation Environment*

Simulations were performed using the Standard CNTFET model in Cadence virtuoso .

The Standard CNTFET model is a circuit-compatible compact model for the intrinsic channel region of the MOSFET-like single-walled CNTFETs. This model is valid for CNTFET with diameters.

The circuits were simulated at room temperature, at 1 Volts power supply. CNTFETs used in this design are configured to have three tubes, a channel length of 28nm and a pitch value of 20nm.

B. Results and Discussion

A new design for MUX proposed in this paper, which is implemented using Cadence Virtuso. The simulation results obtained are as shown in Table 3 and 4.

Table 3

Implementation	Threshold voltage(V)	Diameter(nm)
2X1 MUX	0.429	1.01
4X1 MUX	0.548	0.79

The diameter of the CNTFET vary with threshold voltage. This gives number of benefits in the decrease of the power and delay. Major effects of this change is to get the result in power and area consideration. Diameter of CNT is vary but find the problem when considering less than of 1nm.

Conductivity of Carbon nanotubes (CNTs) are high and gives the advantages in to growth the strength. Carbon nanotubes are given the advantage to reduce power and this result is also benefited to utilize in energy storage.

Table 4 represent the power consumption and delay in the 2X1 MUX and 4X1 MUX. Delay play very important role in this.

Table 4

Implementation	Power consumption	Delay
2X1 MUX	1.74	30.05
4X1 MUX	5.25	35.45

V. CONCLUSION

In this paper implement a two different types of multiplexer by using cadence virtuoso software with the diameter of 1.01nm and 0.79 nm. Take the threshold voltages 0.429V and 0.548V of 2X1 MUX and 4X1 MUX. When calculate and analyse this got the result that 40% improvement in the power consumption and 32% improvement in the delay with supply voltage of 1V.

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