WWW.IJRPR.COM

International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

Implementation of 16 Bit RISC CPU at 1 GHz Clock Speed in 45nm PDK

Mr. S. R. Naresh [1], Mr. K. Rishikesh[2], Mr. P. J. Mukesh Babu[3]

[1] (Associate Professor), *Electronics & Communication Engineering, K.L.N College of Engineering, India*
[2,3] (UG Scholar) *Electronics & Communication Engineering, K.L.N College of Engineering, India*

ABSTRACT:

The escalating intricacies in CPU design within Complex Instruction Set Computers (CISC) and a noticeable performance gap, engineers sought alternative solutions. The Reduced Instruction Set Computer (RISC) architecture, executing concise and similar instructions within comparable time limits. The primary aim was to curtail power consumption, paving the way for the development of low-power systems. The design workflow spans from designing processor architecture and represents the hardware portion of the implementation in the Register-Transfer Level (RTL). RTL which then transformed into gate-level netlist and then transformed it into physical layout as the GDSII file format, a prerequisite for foundries in the Integrated Circuit (IC) manufacturing process. Leveraging the best process node alongside industry-standard tools such as Cadence Innovus and Genus promises a substantial reduction in power requirements and a notable enhancement in processor performance. The processor's architecture incorporates fundamental elements like an Arithmetic Logic Unit (ALU), accumulator, instruction register, and a program counter. This strategic approach holds potential for advancing both processor efficiency and power optimization

Keyword: Reduced Instruction Set Computing (RISC); VLSI; Cadence; 45nm

1. Introduction

According to the recent study India's semiconductor market to soar, potentially reaching more than $11 billion by 2027 and $60+ billion by 2030, capturing 10% of global consumption. PPA (power performance area) is a major factor in VLSI industry. Reduced Instruction Set Computing (RISC) processors excel in executing a smaller set of instructions more quickly compared to Complex Instruction Set Computing (CISC) processors. This efficiency is valuable in applications where speed and responsiveness are critical, such as in data centers, edge computing devices, and high-performance computing clusters. With the increasing demand for energy-efficient computing solutions to reduce carbon footprints and operational costs, RISC processors offer an advantage. Their simplified instruction sets, and architectural designs often consume less power compared to their CISC counterparts, making them suitable for battery-powered devices, IoT (Internet of Things) devices, and mobile computing platforms. RISC architectures can be advantageous for enhancing security and mitigating vulnerabilities. By simplifying the instruction set and reducing the attack surface, RISC processors can be more resilient against certain types of cyber threats, making them attractive for applications requiring robust security measures, such as data encryption, secure communications, and critical infrastructure. Overall, the need for RISC processors in 2024 remains robust, driven by their performance efficiency, power efficiency, customization capabilities, scalability, and security advantages, making them a preferred choice for a wide range of computing applications in various industries.

2. Procedure methodology

In the realm of VLSI design, methodologies and tools serve as indispensable companions, guiding designers through the intricate journey of crafting intricate integrated circuits that power our digital world. These methodologies encompass a spectrum of strategies, from architectural planning to physical implementation, each tailored to address specific challenges encountered during the design process. Complementing these methodologies are the sophisticated electronic design automation (EDA) tools, which serve as the digital workbenches of modern designers. These tools provide a comprehensive suite of functionalities, ranging from synthesizing abstract design concepts into tangible hardware descriptions to meticulously verifying design correctness and optimizing performance metrics. From the synthesis of RTL descriptions to the intricate choreography of physical layout, these tools empower designers to navigate the labyrinthine landscape of chip design with finesse and precision.

Moreover, methodologies such as hierarchical design and register transfer level (RTL) design advocate for structured approaches, allowing designers to partition complex designs into manageable modules and abstracting implementation details to foster design reuse and scalability. These methodologies encompass a spectrum of strategies, from architectural planning to physical implementation, each tailored to address specific challenges encountered during the design process. Concurrently, methodologies such as design for manufacturability (DFM) and design for testability (DFT) embed

considerations for manufacturability and testability directly into the design process, ensuring that the resulting chips are not only functional but also viable for mass production and reliable operation.

In essence, the symbiotic relationship between methodologies and tools forms the cornerstone of modern VLSI design, facilitating the seamless translation of abstract design concepts into tangible silicon realities. Armed with these powerful resources, VLSI designers can navigate the intricate intricacies of chip design with confidence, unleashing their creativity to push the boundaries of innovation and shape the technological landscape of tomorrow.Design flow, also known as the design methodology, is a systematic approach used in VLSI design to ensure the efficient and effective development of integrated circuits. These methodologies encompass a spectrum of strategies, from architectural planning to physical implementation, each tailored to address specific challenges encountered during the design process.

3. Significance and Impact

The significance and impact of VLSI design flow resonate across various facets of modern society, propelling technological advancement, economic growth, and societal transformation. At its core, VLSI design flow serves as the engine driving innovation in the semiconductor industry, enabling the development of increasingly complex and sophisticated integrated circuits that power the devices and systems we rely on daily. From the microprocessors driving computing devices to the specialized chips fueling advancements in healthcare, transportation, communication, and beyond, VLSI technology underpins the fabric of our interconnected world.

Moreover, VLSI design flow has been instrumental in pushing the boundaries of miniaturization and integration, ushering in an era of compact, energy-efficient electronic devices with unprecedented levels of functionality. This relentless pursuit of miniaturization has not only revolutionized consumer electronics but has also paved the way for transformative technologies such as artificial intelligence, autonomous vehicles, and smart infrastructure. The impact of VLSI design extends beyond technological innovation, contributing significantly to economic growth and job creation worldwide. The VLSI industry forms a vibrant ecosystem encompassing design firms, EDA tool vendors, research institutions, and more, driving economic activity, fostering entrepreneurship, and creating employment opportunities across the globe.

4. Statistical analysis

The realm of 16-bit RISC processors encapsulates a delicate balance between simplicity, efficiency, and functionality. Despite their narrower word size in comparison to contemporary architectures, these processors are adept at performing a wide array of computing tasks with notable versatility and speed. At the core of their design philosophy lies the principle of Reduced Instruction Set Computing (RISC), advocating for a streamlined instruction set that prioritizes simplicity and efficiency over complexity.

A hallmark of 16-bit RISC processors is their concise instruction set architecture (ISA), consisting of a limited number of fundamental operations that execute swiftly within a single clock cycle. This minimalist approach to instruction design not only simplifies the processor's control logic but also enables efficient pipelining, allowing for the concurrent execution of multiple instructions. As a result, 16-bit RISC processors can achieve commendable performance even with their modest word size.

In the realm of embedded systems and microcontrollers, the 16-bit RISC architecture has found widespread adoption due to its combination of performance, simplicity, and power efficiency. For instance, the Microchip PIC24 series exemplifies the prowess of 16-bit RISC processors, offering a versatile platform for a myriad of embedded applications. These processors excel in scenarios where low power consumption, compact footprint, and real-time responsiveness are paramount, making them ideal for applications ranging from consumer electronics to industrial automation.

In the realm of 16-bit RISC processors, speed stands as a fundamental pillar dictating the overall performance and efficiency of computing systems. The importance of speed reverberates across various domains, ranging from industrial automation to consumer electronics, where timely execution of tasks and responsiveness are paramount.

5. Result

Designing a 16-bit RISC processor in a 45 nm technology node using Cadence tools represents a significant achievement in the field of VLSI design. The utilization of a cutting-edge fabrication process like the 45 nm node enables the integration of millions to billions of transistors on a single chip, offering improved performance, power efficiency, and cost-effectiveness.

The choice of a 16-bit architecture reflects a commitment to simplicity and efficiency, aligning with the principles of Reduced Instruction Set Computing (RISC). By employing a streamlined instruction set, the processor can execute instructions swiftly within a single clock cycle, maximizing throughput and performance. This design approach is particularly well-suited for applications requiring fast and responsive computing, such as embedded systems, IoT devices, and consumer electronics.

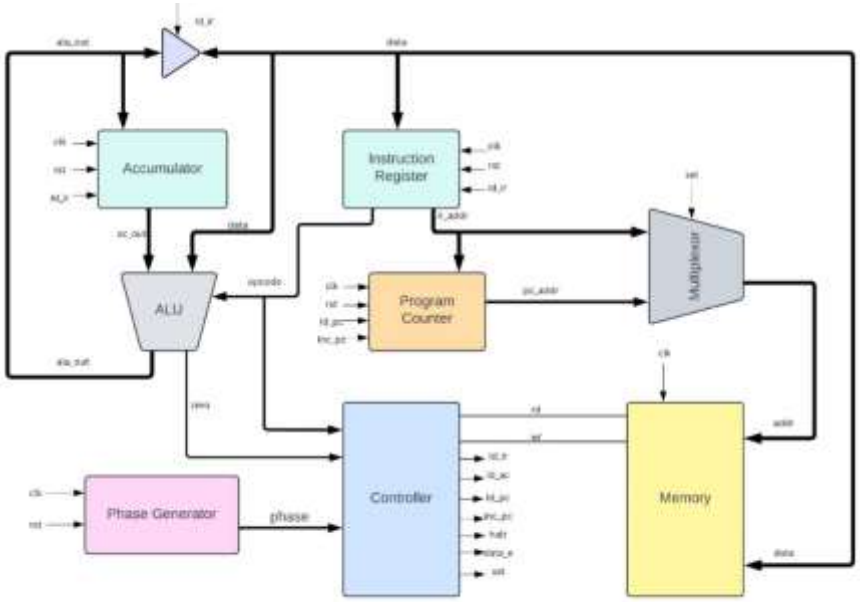
Operating at a frequency of 1 GHz further underscores the processor's capability to deliver high-performance computing in real-time applications. The 1 GHz operating frequency enables rapid data processing, enabling the processor to handle complex tasks with ease and efficiency. This level of performance opens doors for a wide range of applications, including digital signal processing, multimedia processing, and high-speed communication systems..The use of Cadence tools for the design process adds another layer of sophistication to the project. Cadence tools are renowned for their

robustness, versatility, and comprehensive features, empowering designers to tackle the intricacies of VLSI design with confidence. From logic design and simulation to physical layout and verification, Cadence tools provide a holistic platform for the entire design flow, ensuring a seamless and efficient development process.

Table 1 - Specification of the CPU

Parameters/ Blocks	RISC Module	ALU
Power	Leakage Power:196.64nW	Leakage Power:11.78nW
	Dynamic Power:1606787nW	Dynamic Power:81233nW
Performance	1 Giga Hertz	1 Giga Hertz
Area	3519 uM	97 uM
Cells	975	97

5.1 Architecture and Block Diagram:



5.2 Blocks:

ALU

ALU performs arithmetic operations on numbers depending upon the operation encoded in the instruction. This ALU will perform 8 operations on the 8-bit inputs (see table in the Specification) and generate an 8-bit output and single-bit output. In_a, in_b and alu_out are all 8bit long. The opcode is 3-bit value for the CPU operation code.

Controller:

The controller generates control signals for various components based on the current opcode, phase, and other conditions. It facilitates the execution of instructions and manages the flow of data within the processor. Control signals include sel (select instruction address), rd (read from memory), ld_ir (load instruction register), inc_pc (increment program counter), halt (halt machine), ld_pc (load program counter), data_e (enable accumulator output), ld_ac (load accumulator), and wr (write to memory).The controller logic is based on the instruction phase (phase) and the current opcode (opcode), with different actions taken in each phase.

Register:

This module implements a register with synchronous loading capability, storing data (data_in) when the load signal is active. The WIDTH parameter determines the bit width of the input and output data. On the positive edge of the clock signal (clk), the stored data is updated (data_out) based on the input data (data_in) and the load signal.

Memory:

The memory module simulates a memory unit, capable of reading and writing data based on the address provided. The AWIDTH parameter determines the bit width of the address, while the DWIDTH parameter determines the bit width of the data. Data is stored and retrieved from an internal array based on the address (addr) and the read/write (rd/wr) signals. Memory operations are synchronized with the clock signal (clk).

Counter:

This module implements a counter with synchronous loading and counting capability. The WIDTH parameter determines the bit width of the counter. The counter value (cnt_out) is updated based on the clock signal (clk), reset signal (rst), load signal (load), and enable signal (enab).The counter can load a new value, count up, or remain idle based on the control signals.

RISC:

The top-level module that integrates all other modules to create a complete 16-bit RISC processor. It orchestrates the operation of the processor, including instruction fetching, decoding, execution, and data manipulation. The processor's behavior is determined by the interactions between its constituent modules, controlled by the clock signal (clk), reset signal (rst), and other control signals.

5.3 Synthesis:

Logic Synthesis is the Process of Converting the RTL code into a Gate Level netlist using Logic Library, In this case the logic library is given in the 45nm Process Design Kit (PDK)

5.4 Scan Insertion:

Scan Insertion is the testing circuit that used to test the manufacturing faults in the circuits such as stuck-at fault, Transition fault, short or Open Circuit and Logical fault, this step comes under the process of DFT(Design for Test)

5.5 Physical Design

Physical Design is the process of designing the layout the desired circuit that has to be fabricated in the silicon, this process include Floor Planning, Power Planning, Placement, Clock tree Synthesis, Routing and GDSII(Graphic Data System Information Interchange).

5.6 Verification and Signoff:

Verification of the system includes Physical verification and Timing Verification,

- Physical Verification includes DRC, LVS, Antenna Violation, Connectivity and IR drop
- Timing Verification includes Setup Violation, Hold Violation, Signal Integrity

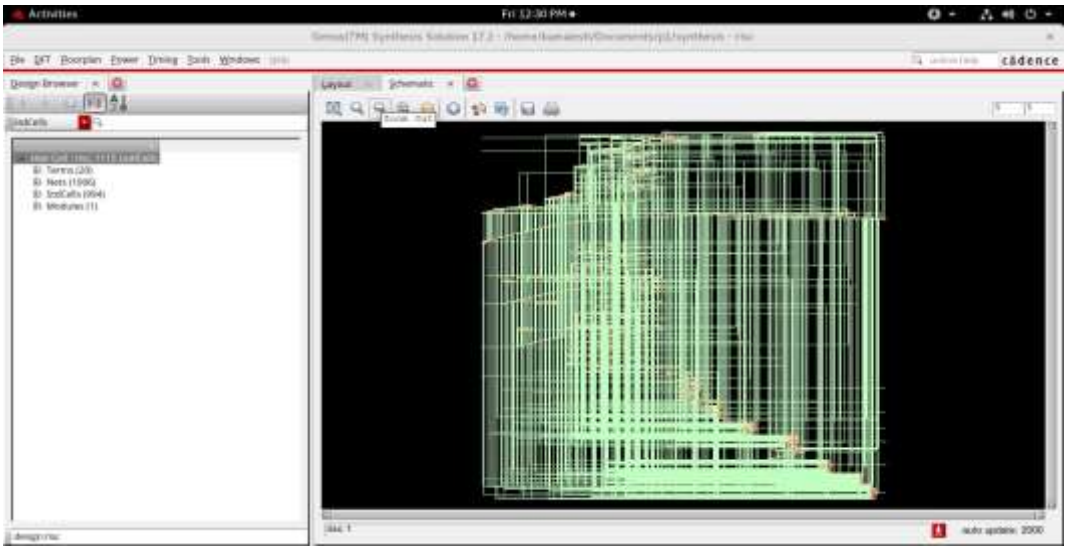


Fig. 1 - Schematic with CPU and Scan Chains

Desired Design Constraints (SDC):

```
create_clock -name clk -period 1 -waveform {0 0.5} [get_ports "clk"]

set_clock_transition -rise 0.1 [get_clocks "clk"]
```

```
set_clock_transition -fall 0.1 [get_clocks "clk"]

set_clock_uncertainty 0.01 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "rst"] -clock [get_clocks "clk"]

set_output_delay -max 1.0 [get_ports "hlt"] -clock [get_clocks "clk"]
```

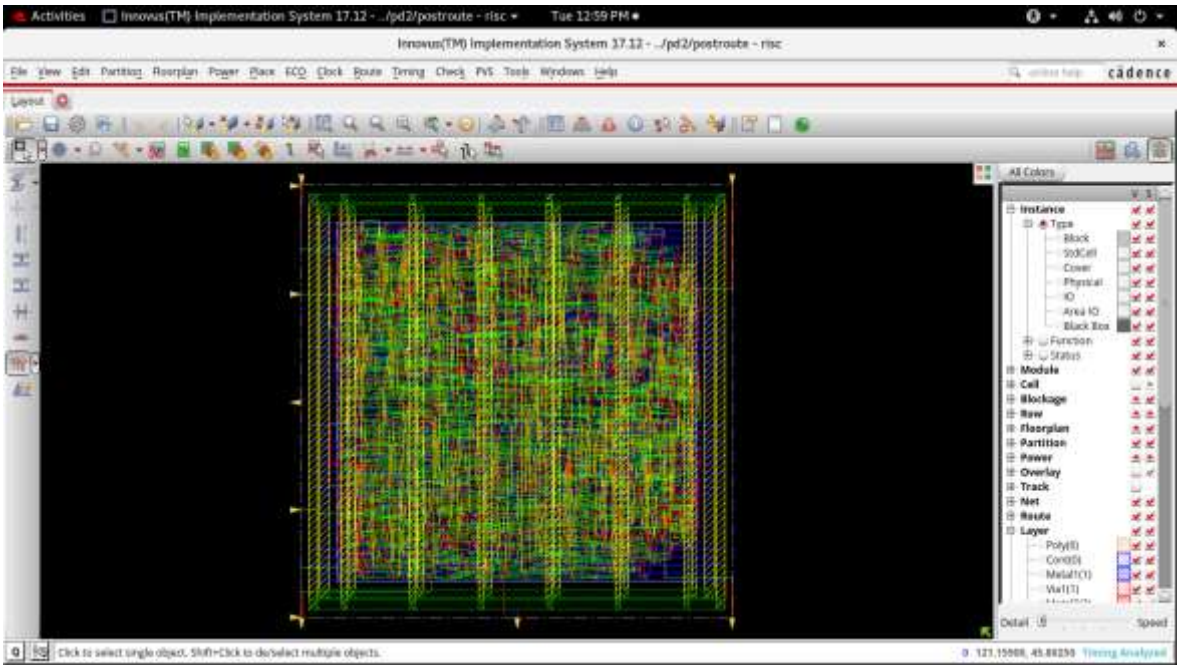


Fig. 2 - Physical Layout

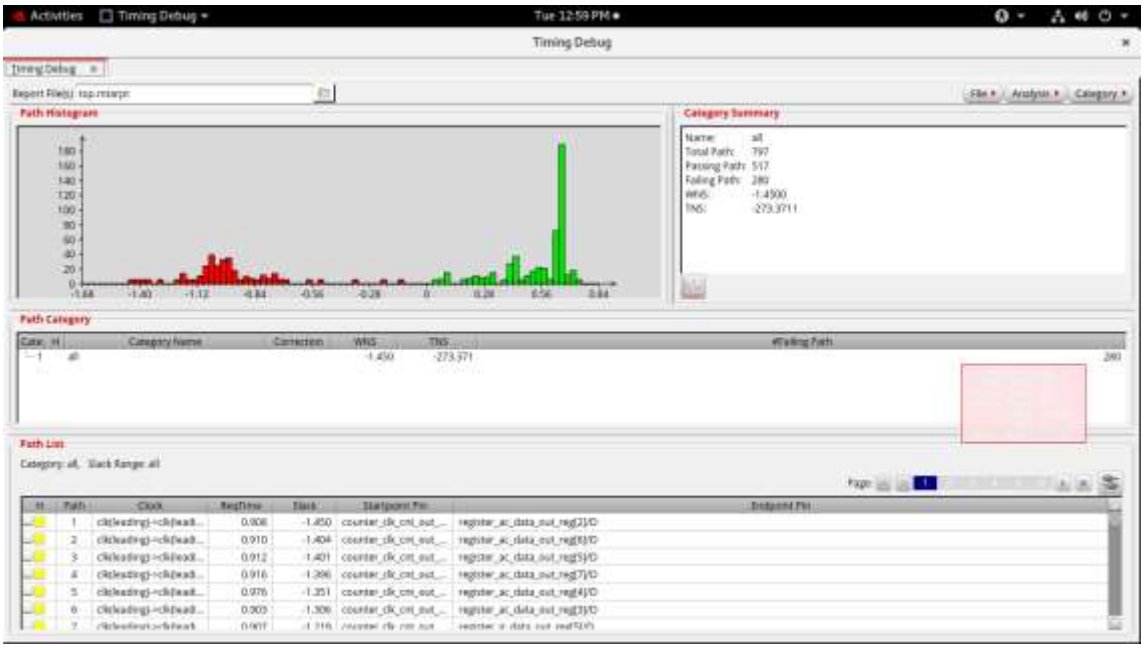


Fig. 3 - Timing Verification Before Fixing Errors

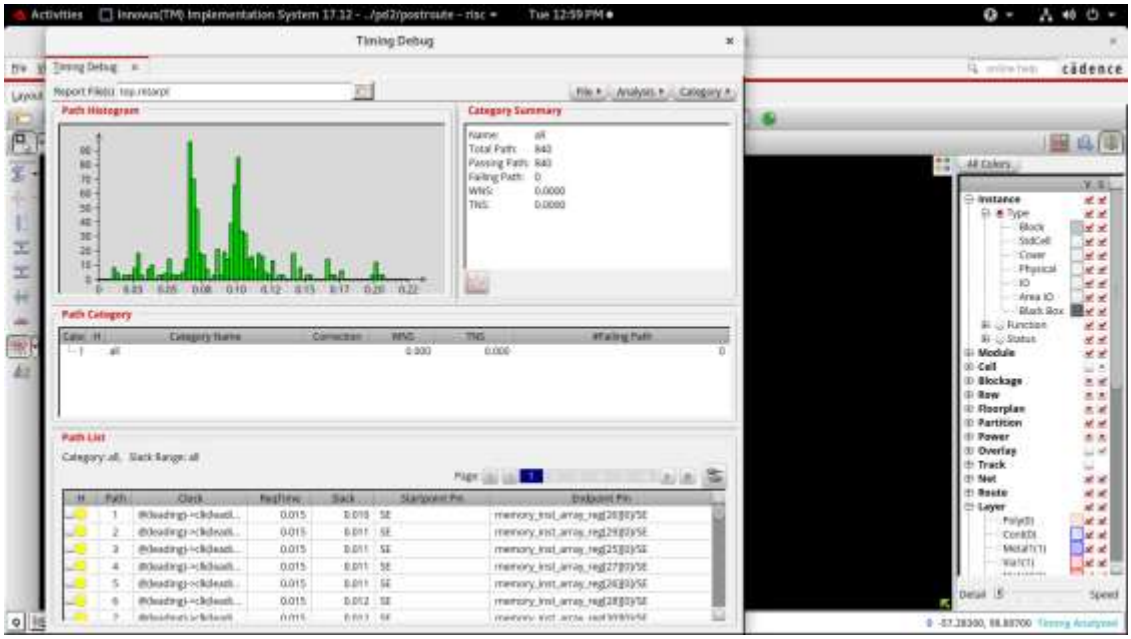


Fig. 4 - Timing Verification after Fixing Errors

6. Conclusion

In conclusion, the development of the 16-bit RISC processor utilizing Cadence tools and targeting the 45nm technology node marks a significant achievement in the realm of VLSI design. This project embodies the synergy of innovative architectural concepts, meticulous design methodologies, and advanced EDA tools to realize a high-performance computing solution

Expanding the project scope to a dual core processor introduces complexities related to inter-core communication, memory consistency, and software parallelization. Addressing these challenges while maintaining performance, scalability, and power efficiency will be key objectives in the development of the multi-core processor.

References:

[1] Arif Ahmed, Arnab Das, Iqbalur Rahman Rokon and Md. Abu Obaidah, "RISC(16-bit) Processor Design using Verilog and FPGA", International Conference on Computer Science and Information Technology (ICCSIT'2016), Jan. 12–13, 2016.

[2] Sidheeq. V. M Aboobacker, "Four Stage Pipelined 16 bit RISC on Xilinx Spartan 3AN FPGA", International Journal of Computer Applications (0975888), vol. 48, no. 6, June 2012.

[3] Ramesh Gaonkar,“Microprocessor architecture, programming and applications with the 8085”, Penram International Publishing,1989

[4] Virendra S. and Michiko I,“Instruction Based SelfTesting of Delay Faults in Pipelined Processors”, IEEE Transaction on VLSI systems, vol. 14, no.11,pp.1203-1215