International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

Analytical Modeling of parasitic Capacitance using Complementary Field Effect Transistor (CFET)

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Doi: https://doi.org/10.55248/gengpi.5.0524.1265

ABSTRACT :

New techniques Developed to reduce circuit level work of the devices and also benefits for the efficiency of transistors Complementary field effect transistors (CFETs) is used with stacked N-type FETs (NFETs) and P-type FETs (PFETs). By using this technique basically difference in the geometry of the design Compared to the conventional MOSFET design. To represent the inverter structure of CEET in this paper for a test model to quantify capacitances in the parasitic way. This gives benefits in terms of speed and accuracy of the circuit.

For reducing parasitic capacitance in CFET-based circuit designs this model play important role. The impact of device failure on the total investment was also evaluated. The weld design model is integrated into the BSIM model and can be used for 3D TCAD simulations. The proposed model will help reduce interference in CFET device design and CFET-based power generation.

Index Terms—Analytical model, Power generation, complementary field-effect transistor (CFET), parasitic capacitance.

I. INTRODUCTION :

Complementary FET is a transistor design that can spread CMOS beyond the N3 technology node. Due to its vertically stacked nMOS and pMOS structure, CFET is attractive for machine nodes that scale above 1 nm. CFETs offer advantages over other types of transistors, such as nanosheet FETs (NSFETs), including reduced area, power consumption, bus length, and full wafer-scale cell size. CFET has also demonstrated the potential of static random access memory (SRAM) cell designs, achieving area measurements of up to 58% and 42% compared to nanosheet (NS) and fork-sheet (FS) technology, respectively. Optimal solutions and interface design methods are provided to overcome challenges such as communication difficulties and power constraints in CFET design. Overall, CFETs provide a great way to bridge CMOS over N3, with advantages in all aspects of transistor design and whole-chip IC design.

CFET is an eye-catching option for the growth of 3D CMOS device technology, bringing significant differences in devices with more complex geometries [1]–[3].For high frequency concerned as technology continues to grow, connecting different electronic devices is effective to prevent interference of advanced systems. The intrinsic capacitance and parasitic capacitance is the total transistor input capacitance. Parasitic capacitances arise due to coupling capacitances between the transistor, gate and channel capacitances and connectivity of the wire in the systems.

Figure 1 shows that the structure of the CFET inverter. This diagram helps to understand the how shared drain, stacks N/PFETs with multiple gates and embedded power rail (BPR) is connected. Figure 2 shows the schematic of the inverter and electrode structure of the CFET. The color presentation match with their generator as a fig.2(a) and fig.2(b). here four terminal inverters are deliberated.In the Junction capacitance, intrinsic part indicates capacitance in the channel with the gate and jumper in the system indicate the parasitic part when used the CFET Transistor.Total parasitic capacitance is large compare with intrinsic capacitance in the 3D simulation with CFET inverter. In this work, we calculate the entire test model for all relevant parasitic capacitances. The results show that the numerical simulation of the test model and layout is good. We examine the change of parasitic capacitance with the sample, aiming to reduce the parasitic capacitance.

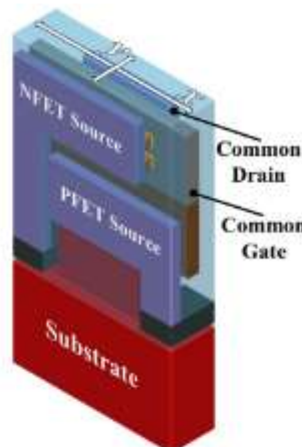

Fig. 1. Structure of the CFET inverter[5].

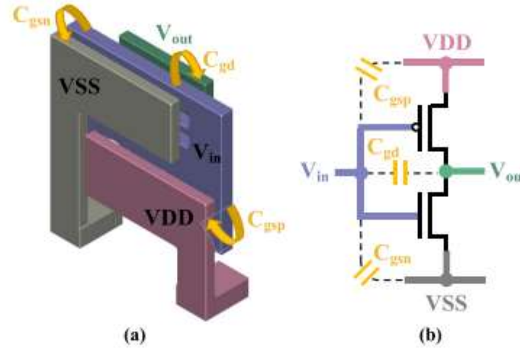

Fig. 2. (a) Electrode structure of the CFET inverter. (b) Schematic of the inverter.[5]

The CFET inverter model, although difficult due to its 3D presence (especially the connection points), still shows great potential over the FET companion due to its unique compact geometry overall advantage.

II. CALCULATION OF CAPACITANCE

The capacitive coupling model calculation are presented in the model.

For all parasitic capacitances a complete series of connected models has been created of CFET inverter units based on the devices. The change in the model is measured by the simulation, calculation and analysis of the model.

Here considers a parasitic capacitance in the design is gate-to-drain capacitance (CGD), gate-to-source capacitance (CGS), capacitance field for large capacitor (CSB), gate-to-body capacitance (CGB), and bulk capacitor (CDB).By taking CGB, switching region of the transistor consider and determine all existed potential. In these region have linear, nonlinear properties are discussed in the calculation with dimensions (W/L) of the transistor, the value of each parasitic capacitance can be calculated.

$$C_G = C_{ox}LW + 2C_0$$
$$C_{GD} = C_{GS} = \frac{1}{2}C_{ox}WL + C_0$$
$$C_{DB,bot} = K(V_l)C_{j0}A_D$$
$$C_{DB,SW} = K_{1/3}(V_l)C_{jsw}l_D$$
$$C_{DB} = C_{DB,bot} + C_{DB,SW}$$
$$C_{SB,bot} = K(V_l)C_{j0}A_S$$
$$C_{SB,SW} = K_{1/3}(V_l)C_{jsw}l_S$$
$$C_{SB} = C_{SB,bot} + C_{SB,SW}$$

Where:
L = channel length
W = channel width
C_o = overlap capacitance
C_{j0} = zero bias capacitance per unit area
C_{jsw} = zero-bias sidewall capacitance per unit perimeter
A_D = Area of drain
l_D = perimeter of drain
A_S = Area of source
L_S = perimeter of source

III. MODEL CIRCUIT AND SIMULATION

The total parasitic capacitance is the addition of Cgd, Cgsn, and Cgsp. CFET inverter have a perpendicular plate, parallel plate and with offset.

In the Figure 3 shows that the Transistor-level representation with capacitance in two inputs. Giving the inputs A and B and takes the output from the drain of the circuits. Capacitance are considered in every transistor in the logic circuits with bulk capacitance model in external nodes. Every transistors capacitances are calculated.

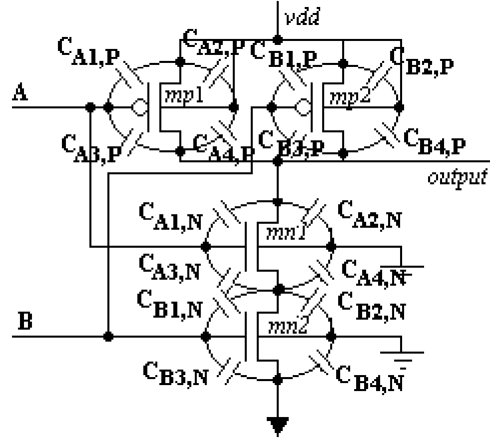

Figure 3: Transistor-level representation with capacitance in two inputs

Two inputs combination are 00, 01, 10 and 11. Input "a":

When input is applied 0(00) and 2(10), in this case the "mn2" transistor is OFF and the capacitance node (Ca1) is equal to:

$$C_{a1} = 0.5(C_{A1,N} + \frac{C_{A3,N} * C_{T,N}}{C_{A3,N} + C_{T,N}})$$
$$C_{T,N} = C_{A4,N} + C_{B1,N} + C_{B2,N}$$

When input is applied 1(01) and 3(11), in this case the "mn2" transistor is ON and the capacitance node (Ca2) is equal to:

$$C_{a2} = 0.5(C_{A1,N} + C_{A3,N})$$

Then

$$C_{A,N} = C_{a1} + C_{a2}$$
$$C_{A,N} = 0.5\left(C_{A1,N} + \frac{C_{A3,N} * C_{T,N}}{C_{A3,N} + C_{T,N}}\right) + 0.5(C_{A1,N} + C_{A3,N})$$

In terms probabilistic:

$$C_{A,N} = p_0\left(C_{A1,N} + \frac{C_{A3,N} * C_{T,N}}{C_{A3,N} + C_{T,N}}\right) + p_1(C_{A1,N} + C_{A3,N})$$

and C_{Agate} is:

$$C_{Agate} = p_0\left(C_{A1,N} + \frac{C_{A3,N} * C_{T,N}}{C_{A3,N} + C_{T,N}}\right) + p_1(C_{A1,N} + C_{A3,N}) + C_{A1,P} + C_{A3,P}$$

Where

p_0 = probability (second input =0)

p_1 = probability (second input =1 ($p_0 + p_1 = 1$).

Same analysis done for the input B.

When input is applied 0(00) and 1(01), in this case the "mn1" transistor is OFF and the capacitance node (Cb1) is equal to:

$$C_{b1} = 0.5(C_{B3,N} + \frac{C_{B1,N} * C_{T1,N}}{C_{B1,N} + C_{T1,N}})$$

When input is applied 2(10) and 3(11), in this case the "mn1" transistor is ON and the capacitance node (Cb2) is equal to:

$$C_{b2,N} = 0.5(C_{B1,N} + C_{B3,N})$$

Then

$$C_{B,N} = 0.5(C_{b1,N} + C_{b2,N})$$
$$C_{B,N} = 0.5\left(C_{B3,N} + \frac{C_{B1,N} * C_{T1,N}}{C_{B1,N} + C_{T1,N}}\right) + 0.5(C_{B1,N} + C_{B3,N})$$
$$C_{T1,N} = C_{A4,N} + C_{A3,N} + C_{B2,N}$$

The probabilistic representation is:

$$C_{B,N} = p_0\left(C_{B3,N} + \frac{C_{B1,N} * C_{T1,N}}{C_{B1,N} + C_{T1,N}}\right) + p_1(C_{B1,N} + C_{B3,N})$$
$$C_{Bgate} = p_0\left(C_{B3,N} + \frac{C_{B1,N} * C_{T1,N}}{C_{B1,N} + C_{T1,N}}\right) + p_1(C_{B1,N} + C_{B3,N}) + C_{B1,P} + C_{B3,P}$$

Where:

C_{Agate} = Equivalent capacitances for input A .

C_{Bgate} = Equivalent capacitances for input B.

The output is:

$$C_{out} = C_{A1,N} + C_{A2,N} + C_{A3,P} + C_{A4,P} + C_{B3,P} + C_{B4,P}$$

IV. RESULTS AND DISCUSSIONS

By changing the parameter of the design, accuracy of the model is verified.

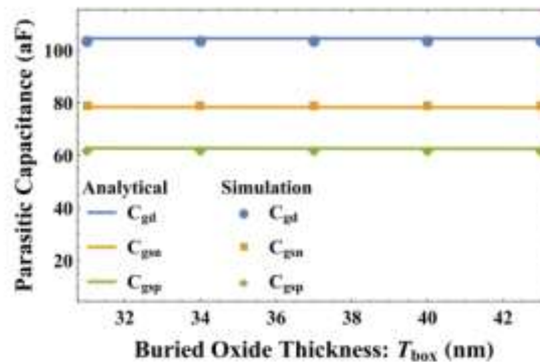

Figure 4 The parasitic capacitances vary with buried oxide thickness

As shown in Figure 4, Cgsp < Cgsn in all cases.in the graph shows that the BPR (Tbox) buried depth increased but the number of parasitic not change expressively. This shows that negligible parasitic capacitance between BPR and gate.

Figure 5 shows that the metal spacing of the gate vary with parasitic in which present the distance between the gate and other terminals as Tsp. Distance shows the transmission capacity.

In N/PFET HDdev , Cgd and Cgsn increase with the vertical distance. The Cgsp doesn't change with HDev because bottom of the device is a core of the PFET. this is not able to do switching in HDev as shown in the figure 7.

Biasing the plates of the capacitance is in effect on extension of the gate with Cgd. The change in gate and drain capacitance is due to the offset the plates of the capacitance as shown in the figure 8.If you focus on the other side in the gate extension changes, polarization is also changed. No change done in these capacitances Cgsn and Cgsp .

In the figure 9 shows that the parasitic capacitance increases due to increases of Wsheet.

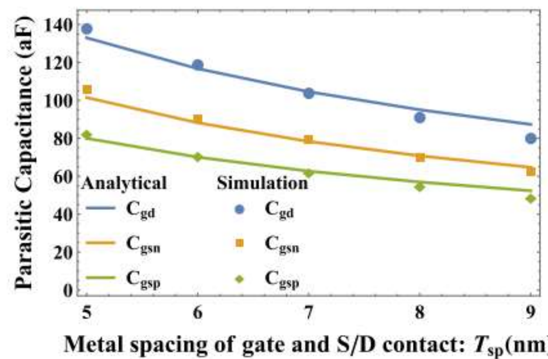

Figure 5 The parasitic capacitances vary with with metal spacing of gate

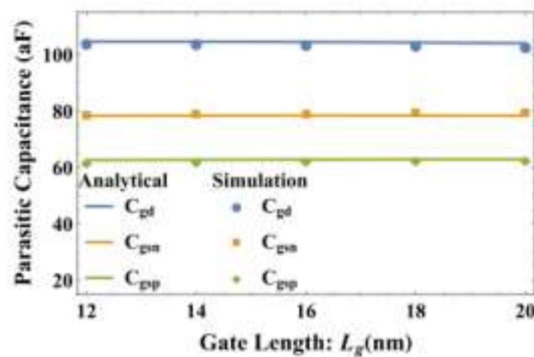

Figure 6 The parasitic capacitances vary with gate length

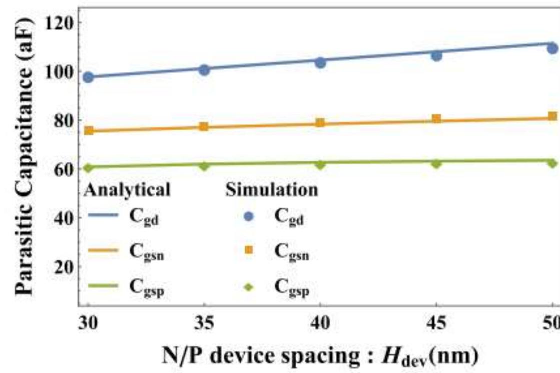

Figure 7 The parasitic capacitances vary with N/P device spacing

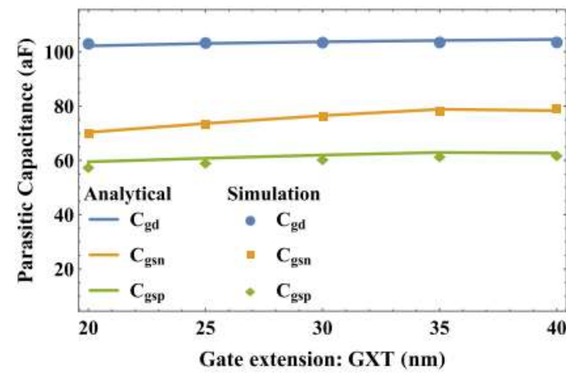

Figure 8 The parasitic capacitances vary with gate extension

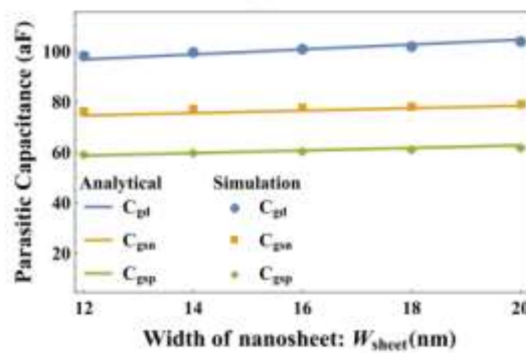

Figure 9 The parasitic capacitances vary with width of nanosheet

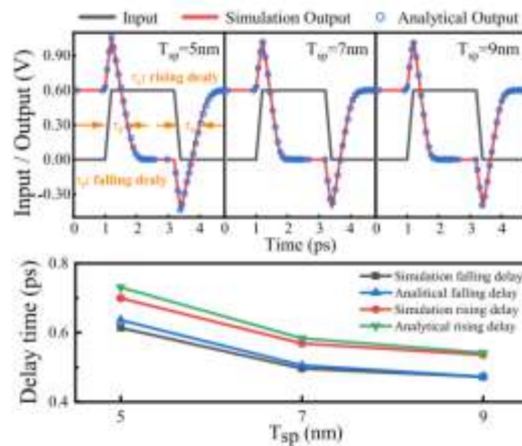

Fig.10.The square wave signal output signal CFET

External power supply is removed and take the structure of CFET in the whole analysis.The parasitic capacitance Cgd, Cgsn and Cgsp are found in this model and all the capcitances replaced by a compressed model. In the time response, output is constant with 3D simulations.

In Figure 10 shows that the transistor cutoff frequency against for different Tsp plotted for the inverter delay. Due to small parasitic capacitance, the delay time decreases as Tsp increases.

V. CONCLUSION

In the whole paper discussed about the design calculation of the parasitic capacitances of the CFET inverters. The parasitic capacitance Cgd, Cgsn and Cgsp are used for the simulations and calculations. After all of these find out their accuracy, geometric parameters and the transient Response of the capacitance models with the difference of parasitic capacitance, Cgsn, Cgsp and Cgd

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