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A Review of Serdes CMOS Transceiver for High Speed Data Transmission

Ravi Kumar M[1], Sanjai S[2], Shilpashree S[3], Shreyas N Kulal[4] and Tinu M[5]

[1]Assistant Professor, Department of Electronics and Communication Engineering, Cambridge Institute of Technology (CI Tech), Bengaluru, India
[2,3,4,5] Student, Department of Electronics and Communication Engineering, CITech, Bengaluru, India
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ABSTRACT

The development of specialized hardware components to expedite image processing activities is the main goal of the VLSI implementation. These parts consist of memory structures designed for image data, processors tuned for particular algorithms, and specialized accelerators for operations like feature extraction, image filtering, and convolution. In order to enable real-time and resource-efficient applications, high-throughput and low-latency image processing on hardware is the aim.

Keywords: SerDes, Image processing, VLSI, Cadence, Hspice, serialiser, Deserialiser, FPGA

Introduction

It gets harder to match the timing restrictions of serializers in transmitters due to increasing data rate of serial links. Clock buffers with delay correction can mitigate this problem by synchronizing the clock and data time. Nevertheless, these buffers become sources of noise in the transmitter output and draw a lot of power. The issue is more severe for serializers other than 2^n:1, and relying solely on 2^n:1 serializers may restrict the design of the system.

SerDes technology is used for high-speed data transfer between various modules and subsystems to provide seamless connection between these VLSI components. The effective serialization and deserialization of data made possible by SerDes integration allows for quick information flow between image sensors, processing units, and memory modules. This method minimizes power consumption, simplifies interconnects, and supports the high data rates required by contemporary image processing applications. Using coaxial or insulated twisted pair cables, serialization and deserialization, long-distance transmission, and other techniques, the SerDes methodology tackles the issues of bandwidth and distance in data transfer.

[This paper also discusses image pre-processing methods like noise reduction and contrast enhancement, as well as image collection devices, their dynamic range, calibration, real-time capture, and data output.]

Numerous studies have been conducted on the foundations of image processing and picture processing, and the results of these studies have demonstrated a wide range of potential applications in a number of scenarios. Very large scale integration (VLSI)-based solutions are limited, according to a review of the literature. The FPGA offers broad capability that enables programming to your specifications.

NOTE: Can be added to introduction or design challenges

But, like with most things in life, the FPGA's flexibility comes with drawbacks. In this instance, the increased cost, greater internal latency, and reduced analog usefulness are the trade-offs for this versatility.

Methodology

Using a SerDes transceiver to create a serial link instead of a parallel bus is a viable alternative. Since serial link based designs have many benefits over traditional parallel implementations—fewer pins, lower power consumption, smaller connectors, reduced complexity, lower electromagnetic interference, and improved noise immunity—they have been used in off-chip communications for decades. Major SerDes components and basic principles are presented, along with the design flow of a 45nm CMOS process Serializer from unit block design in Cadence Virtuoso to simulation in HSPICE. The process begins with the OV7670 camera sensor module, which captures images in the FPGA image processing device. It involves interfacing the OV7670 camera sensor module with the FPGA to receive the raw image data. The raw data is collected and serialized using a SerDes (Serializer/Deserializer) module. The SerDes module converts parallel data from the camera sensor into a serial stream, which is more efficient for processing and transmission within the FPGA. The serialized image data undergoes various image processing algorithms implemented in the FPGA. These algorithms can include tasks such as filtering, edge detection, and object recognition. Once the image processing is complete, later involves using PCIe (Peripheral Component

Interconnect Express) for the output interface. The processed image data is transferred through PCIe to an external device or host system for further analysis or display. Finally, the output display module receives the processed image data and presents it on a display device for visualization or analysis by the user.

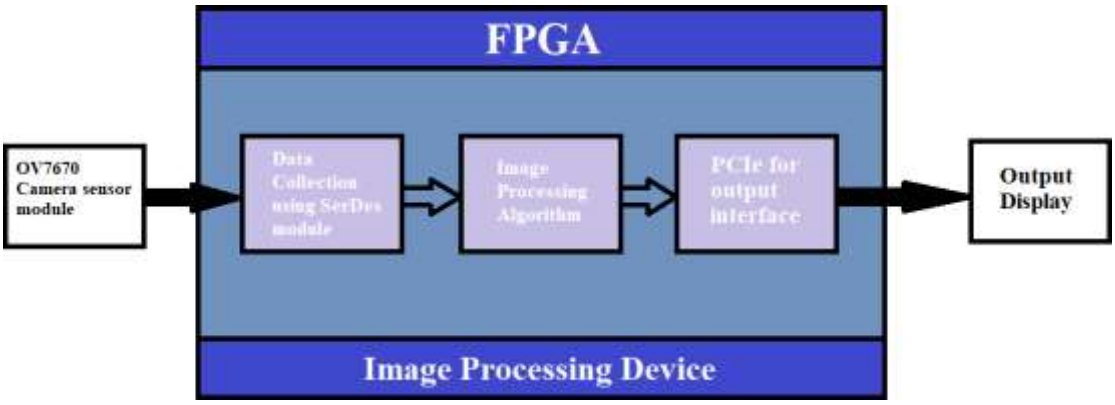

Fig 1: Block diagram

Literature review

[1] Eung-ju Kim Member IEEE, Kwan-Jae Lee and Sukki Kim Senior Member IEEE Dept. of Electrical Engineering Korea University, Seoul, Republic of Korea "A HIGH RESOLUTION SERIALIZER AND DESERIALIZER ARCHITECTURE FOR MOBILE IMAGE SENSOR MODULE"

In mobile display applications, the design of high speed interface circuit with low power consumption and small area are the very important technical issues for good system performance. Conventional parallel interface method is less attractive because of pin numbers, electromagnetic interference (EMI) radiation, signal-integrity concerns at higher bus speeds and higher power-consumption profiles. In addition, parallel buses add complexity to routing on the small printed-circuit-board (PCB) footprints in mobile devices. To solve these problems in mobile display applications, special interface technique so called Mobile Display Digital Interface (MDDI) was introduced and used widely now in mobile display applications. Our proposed serializer was designed using multiplexing method. The previous conventional method needs 8 clocks for one 8-bit data packet to make serialized data. But our proposed serializer needs only four clocks by proposed serializer timing controller. To achieve half rate frequency serialization, multiplexing switch should be selected every four cycle of the input clock.

[2] Taha Mehrabi1 and Kaamran Raahemifar2 Electrical and Computer Engineering Department Ryerson University Toronto, Canada "Design of a Time Mode SerDes using Differential Pulse Position Modulation (DPPM)" 2017 IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE)

Time mode signal processing (TMSP) is the implementation of analog signal processing functions using the most basic element available, namely, propagation delay. Moreover, a time to digital converter (TDC), an important block of time mode circuits, could be used to convert the time difference between two edges of two signals into a sequence of digital numbers.

In this paper, a new time mode SerDes for high data rate chip to chip communication utilizing differential pulse position modulation (DPPM) as the primary method of data encoding was proposed. The proposed design substantiates an improvement in the bandwidth and simplifies the circuit complexity of the currently used serializer de-serializers (SerDes). The complete proposed design was tested in TSMC 65 nm Complementary metal–oxide–semiconductor (CMOS) technology; it achieved a data rate of 5 Gbps running at the input clock frequency of 1.25 GHz.The authors of this paper however, believe that by using a DPPM module only the difference between the original clock and the delayed clock could be sent. This would result in less circuit complexity, greater improvement in bandwidth and further minimization of ISI occurrence. Additionally, there has been abundant research in designing pre-emphasis circuits and decision feedback equalization (DFE) which could be used for reviving the differential pulse position modulated signal at both transmitter and receiver sides respectively

[3] Image Processing Using FPGAs Donald G. Bailey Department of Mechanical and Electrical Engineering, School of Food and Advanced Technology, Massey University, Palmerston North 4442, New Zealand;

The primary objective of the above mentioned paper is to examine the feasibility and benefits of employing FPGAs for image processing tasks. FPGAs offer the advantage of hardware-level parallelism and reconfigurability, making them suitable for real-time and computationally intensive applications. Discusses how FPGAs provide an opportunity for hardware acceleration of image processing algorithms. Unlike traditional software implementations running on general-purpose processors, FPGAs allow for the parallel execution of tasks, leading to potential performance gains.The paper emphasizes the inherent parallelism in FPGA architectures, enabling the concurrent execution of multiple operations. This parallelism is particularly advantageous

for image processing algorithms that involve repetitive and independent computations on pixel data.The author discusses challenges associated with FPGA-based image processing, including design complexity, resource constraints, and the need for specialized knowledge in FPGA programming. Considerations for overcoming these challenges are likely addressed [6].

[4] A low-noise and fast transient response LDO design for high-speed SerDes Shengyu Song*, Jianjun Chen, Hengzhou Yuan, Haiyuan Xing and Yi Wen Collage of Computer, National University of Defence Technology, Changsha, 410073, China

The paper emphasizes achieving low-noise characteristics in the LDO design. Noise in the power supply can impact the signal integrity of high-speed SerDes interfaces, and the authors address this challenge by implementing noise reduction techniques in the voltage regulator. A significant focus of the research is on achieving a fast transient response in the LDO design. Fast transient response is essential for quickly adapting to load variations in SerDes circuits, ensuring signal stability during rapid changes in current demand. The LDO design is tailored for applications involving high-speed SerDes interfaces commonly used in data communication, including applications such as high-speed data transmission, communication between links. The potential drawbacks in the paper may include limitations in generalizability, complexity, and cost if the proposed LDO design is highly tailored to specific SerDes requirements, potentially hindering its applicability to diverse scenarios. Trade-offs in performance, insufficient comparison with existing designs, and a narrow scope of validation might affect the overall robustness and practicality of the proposed solution. Additionally, a reliance on simulations without real-world testing and incomplete performance metrics could limit the comprehensiveness of the study, raising concerns about the reliability and applicability of the proposed LDO design in practical high-speed SerDes applications.

Summary of Literature review

TABLE: Survey summary of serdes implementation

Serial No.	Author & Year	Description	Objective	Methodology	Speed & Power	Problems
1	F. Tobajas et al. (2006)	Proposes a low-power, high-resolution SerDes architecture for mobile display applications using multiplexing and DDR.	Achieve high data rate and low power Consumption for mobile displays.	Multiplexing + LVDS	2.5 Gbps, Low power	Increased complexity, cost.
2	Taha Mehrabi et al. (2017)	Explores time mode signal processing and DPPM for chip-to-chip communication, for improved bandwidth and reduced complexity.	Enhance bandwidth and simplify circuit design for chip-to-chip communication.	Time mode + DPPM	High data rate, Low circuit complexity	Minimizing ISI, limitations With data transmission.
3	Shengyu Song et al. (2015)	Designs a low-noise & fast transient response LDO for high-speed SerDes applications, focusing on signal stability.	Ensure signal stability and fast response in high-speed SerDes applications.	LVDS optimization	Low noise, Fast transient response	Generaliz-ability, lack of comprehensive validation.
4	Chen, F., Wu, J., & Chang, M. F. (2015)	Proposes a 40-Gb/s SerDes interface using transformer-coupled technique for 2:1 MUX and 1:2 DEMUX.	Achieve 40 Gb/s data transmission with Improved signal integrity using transformer-coupled technique.	Transformer-coupled technique	40 Gb/s, Improved signal integrity	Circuit complexity, potential crosstalk issues.
6	Lee, J. et al. (2015)	Designs 56 Gb/s NRZ and PAM4 SerDes transceivers in CMOS.	Design versatile SerDes transceivers capable of high speed (56 Gb/s) and supporting both NRZ and PAM4 formats in CMOS technology.	PAM4 TX: & NRZ encoding	56 Gb/s, best operation.	High end tool requirement, high power consumption.

7	Eung-ju Kim et al. (2014)	Proposes a low-power, high-resolution SerDes architecture for mobile display applications using multiplexing and DDR.	Enhance data rate and reduce power consumption for mobile display applications compared to parallel interface.	Multiplexing + DDR	Higher data rate, Lower power consumption compared to parallel interface	Increased complexity, cost.

Conclusion & future scope

Successful integration of SERDES technology into VLSI design for enhanced data communication in image processing applications. Improved performance metrics such as data transfer rates, latency reduction, and overall system efficiency demonstrated through experimental results. Validation of the proposed methodology for VLSI-SERDES integration in real-time image processing tasks, showcasing its potential for high-performance applications. Future work includes completing other core components of the SerDes, integrating all major blocks into a functioning SerDes system, exploring alternative designs for sub-circuits, optimizing transistor sizing for increased operating frequency, and conducting signal and power integrity analysis to reduce unwanted effects. Validate the VLSI-SERDES integration through simulations and hardware testing to ensure functionality and performance. Measure the data transfer rates, latency, and overall efficiency of the system for image processing tasks.

The use of SerDes technology plays a crucial role in enabling dependable and fast communication among various system components. In designing a Low Dropout (LDO) voltage regulator specifically for high-speed SerDes applications, the paper emphasizes the need of attaining low-noise characteristics and quick transient reactions. The report's case studies and experimental validations offer insightful information on the real-world applications and performance improvements made possible by this integrated methodology. All things considered, the research advances image processing systems by demonstrating how VLSI and SerDes integration may be used to provide real-time, low-latency technologies, and resource-efficient answer for a range of areas.

By sampling input on both positive and negative clock edges, the Deserializer provides a more precise and efficient serialization process. There is no longer a need for an extra latch or 2:1 MUX because to the more precise and efficient design of the proposed Serializer and Deserializer. The significance of comprehending the fundamental elements of a SerDes system and the serialization process for effective high-speed circuit design and execution is emphasized in the thesis' conclusion.

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