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Design of High Speed and Low Power Carry Select Adder

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A B S T R A C T

VLSI system design extensively focuses on developing data path logic systems that are both power-efficient and capable of high-speed operation. Carry propagation delay limits the speed of addition in digital adders. To address this, the Carry Select Adder (CSLA) is commonly used. The CSLA employs multiple pairs of Ripple Carry Adders (RCA) to generate partial sums and carries independently, selecting the final sum and carry using multiplexers (mux).To further improve speed and power consumption compared to the existing CSLA with RCA, this work proposes two enhancements. Firstly, a Binary to Excess-1 Converter (BEC) replaces the RCA, simplifying the addition process and reducing logic gate usage. Secondly, the Kogge-Stone (KS) adder replaces the RCA, utilizing a parallel prefix structure for efficient carry propagation and high-speed operation. By integrating the BEC and KS adder into the CSLA architecture, the design achieves faster speeds and lower power consumption. These modifications optimize carry generation and propagation, resulting in enhanced performance for digital adders.

Keywords: CSLA, BEC-1, KS, high speed, low power.

1. Introduction

The addition operation, which is vital in digital systems' arithmetic computations, is executed using a binary adder. A few instances of the components that constitute into binary adders are memory address units, dividers, multipliers, and arithmetic and logical units (ALU). The speed of the adder exerts an influence on the way digital systems perform collectively. The propagation delay is an essential obstacle in binary word addition, and the carry length is affected by the input data width. In contrast with serial adders, parallel adders tend to have larger delays. Implementing an advanced digital system necessitates taking into aspects of account like area, power, and latency. The challenge of building a high-speed adder impacts the processor performance of a system. Computerised systems,In order to generate partial sums and carries that are eventually selected using multiplexers (mux), the CSLA (Carry Select Adder) is frequently utilised to address the carry adders (RCAs). The response to this challenge is a modernised CSLA method that replaces RCAs with n-bit Binary to Excess-1 code converters (BEC) and a kogge-stone (ks) adder to increase addition speed. Comparing to a Full Adder (FA) structure, this particular version employs fewer logic gates, which lowers space and power. The revised design's performance has been evaluated in terms of delay and power. The evaluation process involves evaluating the basic adder blocks' delay and power. The BEC and KS adder logic's organisation and operation are also presented, and a comparison is performed between the CSLA, the modified design, as well as the upgraded design.

1.1 Binary to Excess-1 Converter(BEC-1)

The suggested work involves the use of n-bit binary to excess-1 converters (BEC) alongside carry select adders to increase adding speed. The suggested 32-bit Carry Select Adder achieves better power and area efficiency than Kogge-Stone adders. With the aim of generating partial sums and carrying, the traditional Carry Select Adder uses multiple ripple carry adders (RCA), which use additional space. Contrarily, the suggested method reduces the number of logic gates and achieves lower power consumption by substituting binary-to-excess-1 converters for RCAs. The 4-bit BEC structure and the truth table are depicted in Figure :1 and Table :1, respectively. The 4-bit BE1C's boolean representation is shown below(take note of the functional symbols for (~)NOT, (&)AND, and (^)XOR.)

X0 = ~ B0

X1 = B0 ^ B1

X2 = (B0 & B1) ^ B2

X3 = (B0 & B1 & B2) ^ B3

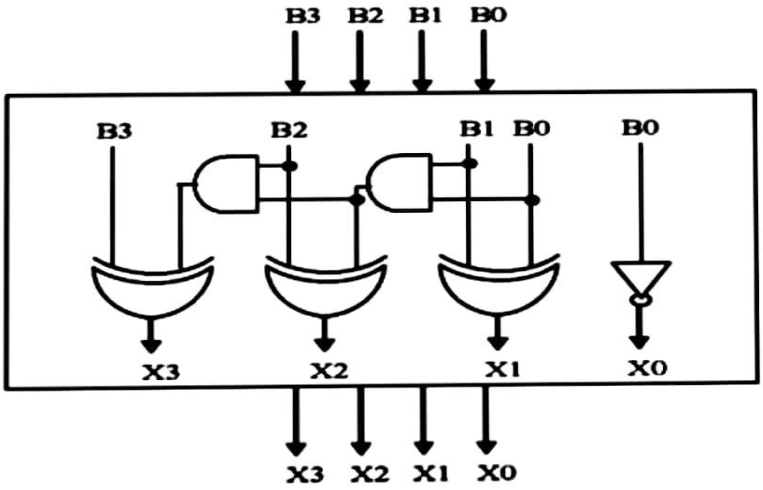

Figure :1 4-bit BEC-1 structure

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

Table :1 Functional table of 4-bit BEC-1

1.2Kogge-Stone Adder(KS)

The Kogge- Stone adder is also known as a parallel prefix adder that performs fast logical addition. Kogge-Stone adder is used for various adders because it gives the less delay among other architectures. The Kogge–Stone adder takes large area to implement but has a lower fan-out at each stage. The 4- bit Kogge- Stone adder as shown in Figure :2.

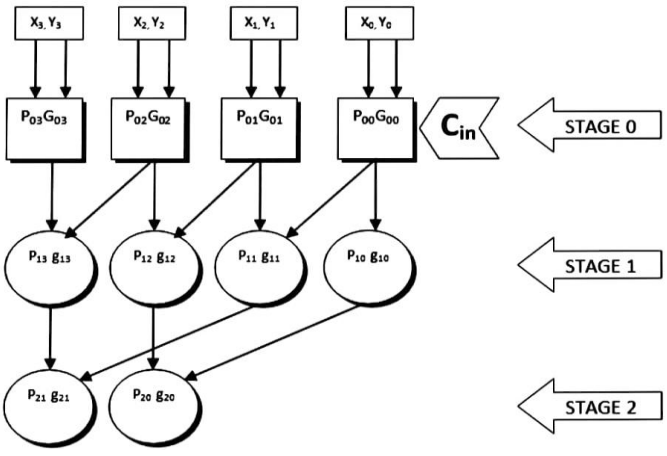

Figure:2 4-bit KS adder structure

Each cell in figure:2 has a specific operation to perform.

Stage-0:

P=Ai^Bi

G=Ai.Bi

Stage-1:

P=Pi.Pi-1

G=Gi|(Gi-1.Pi)

Stage-2:

Si= Pi^Ci

Ci= Gi

1.3Carry Select Adder(CSLA)

A Carry-Select Adder (CSA) is a adder that uses multiple Ripple Carry Adders (RCAs) to perform parallel additions and select the correct sum based on the carry input. Here's how a CSA can be implemented using RCAs shown in Figure :3 (+ indicates RCA)

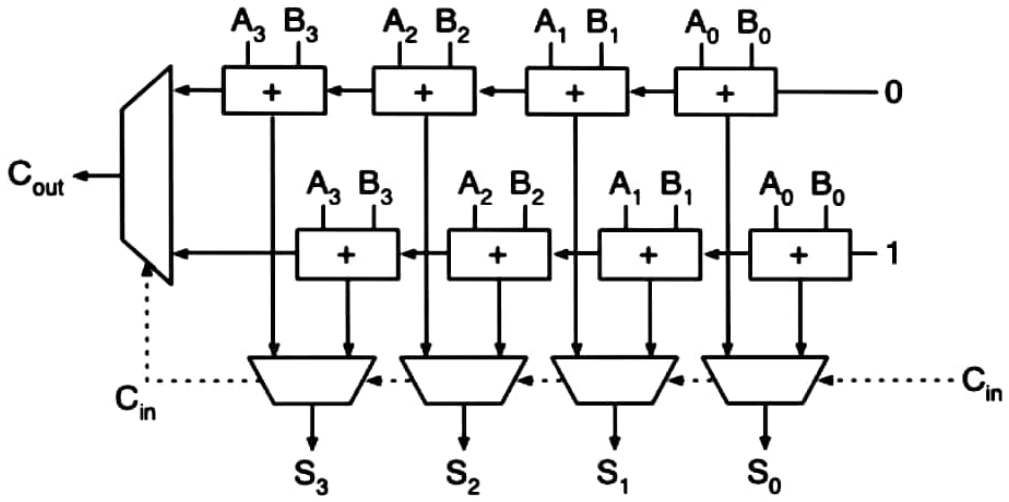

Figure:3 4-bit csla structure

2. Methodology

The CSLA uses multiple pairs of Ripple Carry Adders (RCA) to generate intermediate sum and carry by considering carry input Cin = 0 and Cin = 1 , then the resultant sum and carry are selected by using the multiplexers (mux) which is why it is not area efficient.To overcome the area and power consumption, Binary to Excess-1 Converter (BEC) is used instead of RCA with Cin = 1 in the regular CSLA

2.1 Regular Carry Select Adder

The 32-bit Carry Select Adder shown in Figure :4, has five various groups of Ripple Carry Adders and Multiplexers with different sizes, multiplexers are used to select the correct sum based on the carry-in for each group of bits. The multiplexer inputs are connected to the outputs of the RCA adders, and the selection lines are the carry-in bits.

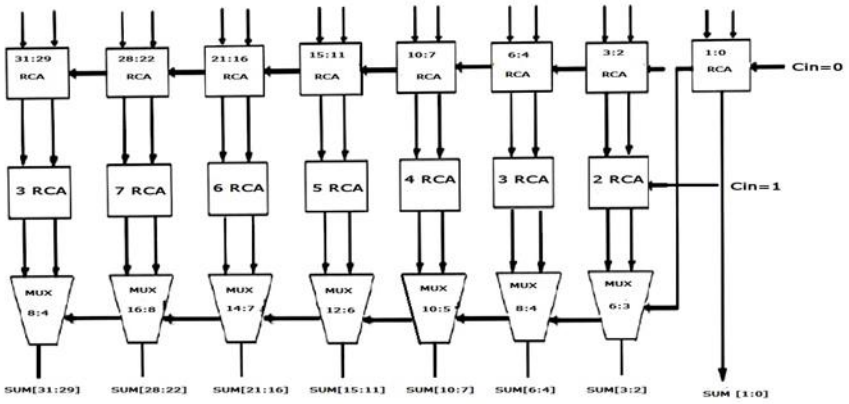

Figure:4 32-bit Regular CSLA Architecture

2.2Carry Select Adder with KS adder

The Kogge-Stone adder have a larger area requirement, but has benefits in terms of reduced fan-out at each stage. Fan-out refers to the number of inputs that a gate drives. In a ripple-carry adder, each stage has a high fan-out because the carry output of each stage is connected to multiple carry inputs of the subsequent stages. This high fan-out can cause issues such as increased delay and power consumption. Kogge-Stone adder provides fasteroperation through parallelism and efficient carry propagation. However, it requires more area due to its increased hardware complexity. Due to this increased hardware complexity, the Kogge-Stone adder requires more space or area to implement compared to a ripple-carry adder. The additional components and wiring needed to achieve the parallelism and efficient carry propagation contribute to the larger area. The architecture is shown in Figure :5.

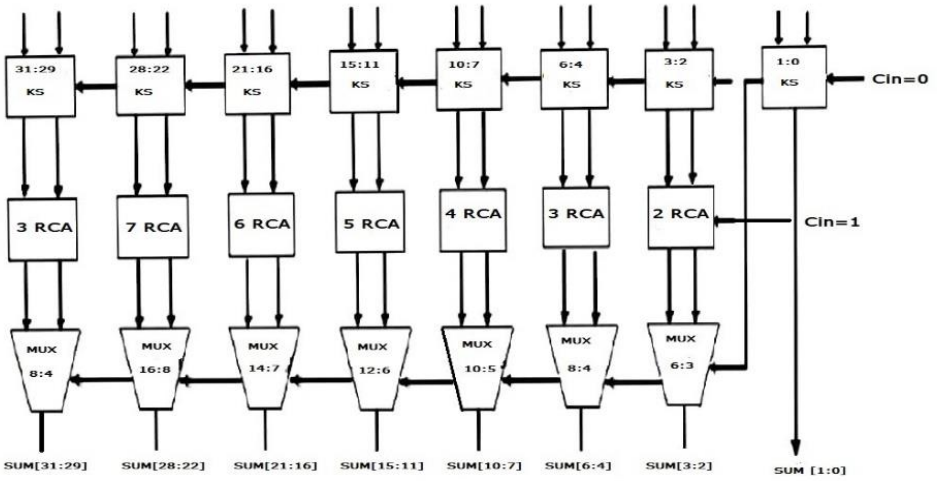

Figure:5 32-bit CSLA with KS adder Architecture

2.3 Carry Select Adder with BEC-1

In Regular CSLA, one from two RCA is replaced by BEC-1. It contributes to achieving reduction in area and power, as BEC-1 has less number of logical gates than the RCA structure. BEC-1 replaces RCA with Cin= 1 in the Regular CSLA. The addition operation becomes simpler with excess-1 representation, addition can be performed using standard binary addition, without the need for complex sign extension. Shown in Figure :6

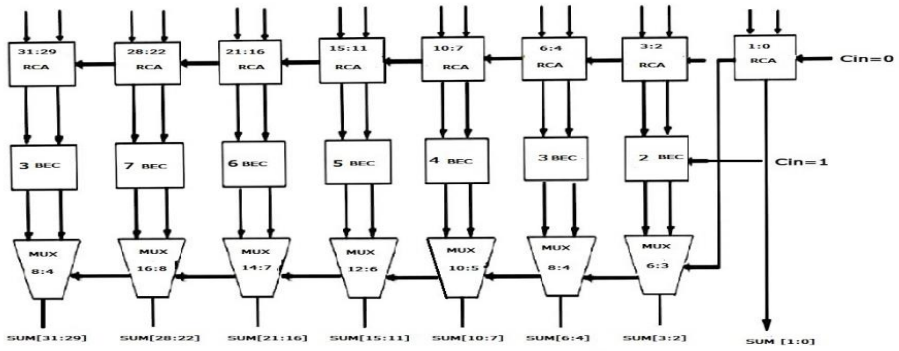

Figure 6. 32-bit CSLA with BEC-1Architecture

3. Simulation Results

The Xilinx software has been used to synthesize the proposed design methodology for a 32-bit Carry Select Adder circuit with the use of BEC. The simulation results using XılınxVivado are shown in the Figure :7, Figure :8, Figure :9.

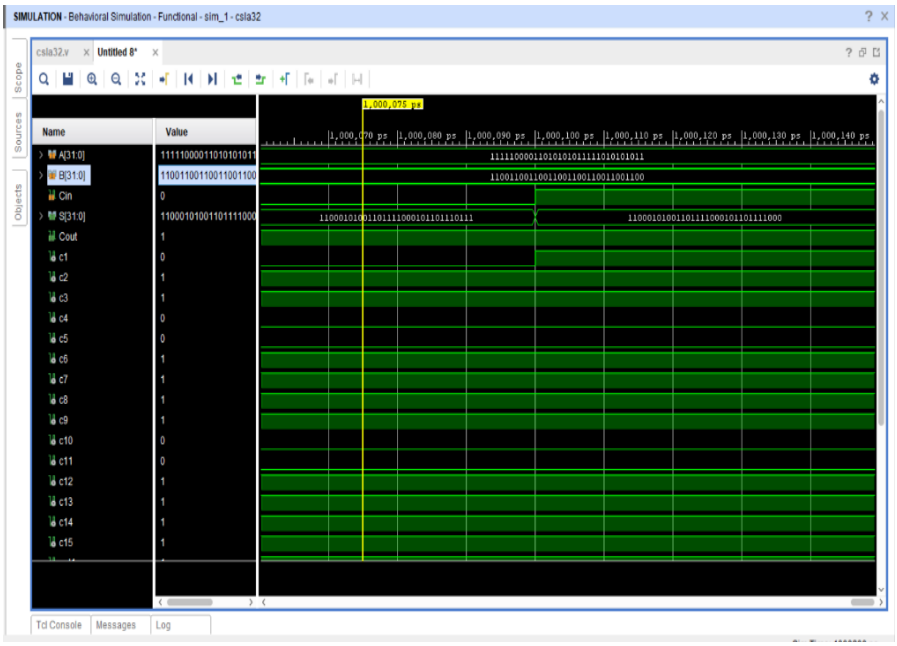

Figure :7 Simulation result of 32-bit Carry select adder

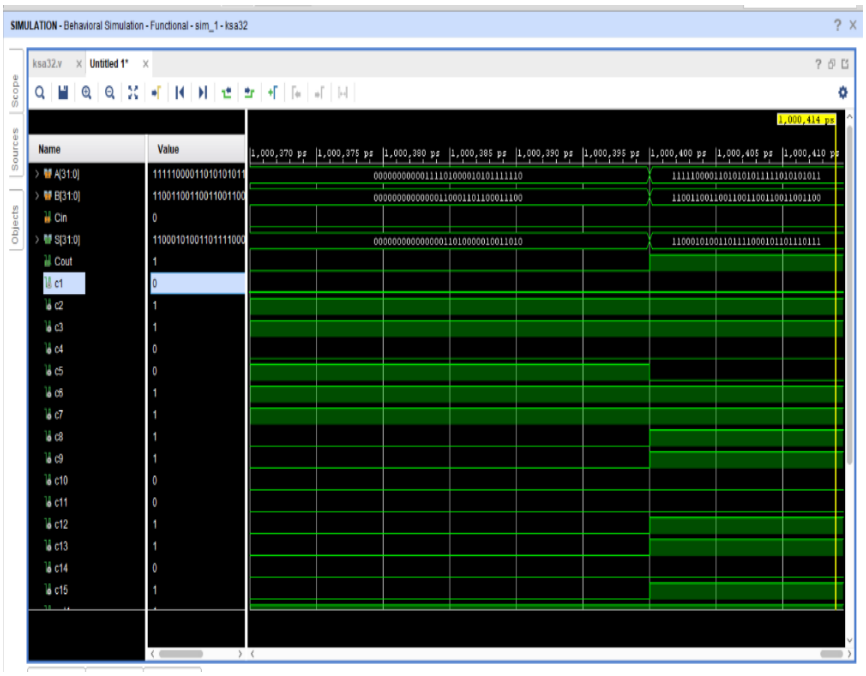

Figure :8 Simulation result of 32-bit CSLA using KS adder

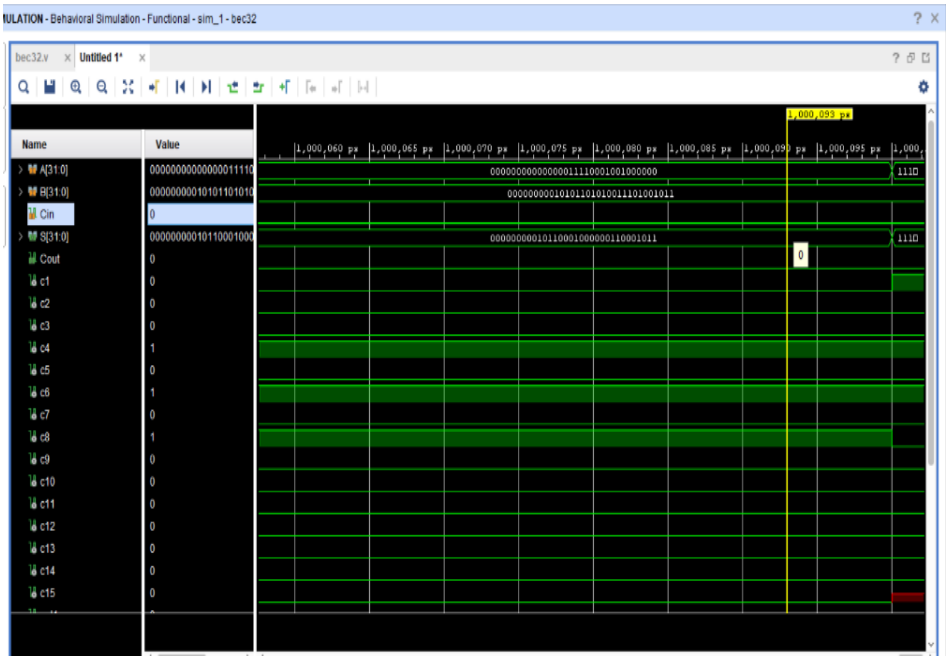

Figure :9 Simulation result of 32-bit CSLA using KS adder

Table :2 Comparison table between CSLA adders with RCA along with KS and BEC-1

SNO	ADDER	POWER	DELAY
1	CSLA	24.768W	12.91ns
2	KS	24.167W	12.73ns
3	BEC-1	23.299W	11.459ns

4. Conclusion

The proposed enhancements of integrating a Binary to Excess-1 Converter and a Kogge-Stone adder into the Carry Select Adder (CSLA) architecture present a significant advancement in VLSI system design for digital adders. By optimizing carry generation and propagation, the enhanced CSLA achieves faster speeds and lower power consumption compared to traditional approaches. These improvements make the modified CSLA architecture well-suited for applications that require high-speed, power-efficient arithmetic operations. Carry Select Adder (CSLA) include replacing the Ripple Carry Adder (RCA) with a Binary to Excess-1 Converter (BEC) Kogge-Stone (KS) adder. These modifications aim to improve speed and reduce power consumption in VLSI system design. The BECsimplifies the addition process and reduces logic gate usage, while the KS adder employs a parallel prefix structure for efficient carry propagation and high-speed operation. By integrating these enhancements into the CSLA architecture, the design achieves faster speeds and lower power consumption, optimizing carry generation and propagation for digital adders. In this, we have implemented various CSLA architectures in Xilinx ISE and Xilinx Vivado for simulation using Verilog HDL. From the analysis of different architectures, the 32-bit CSLA with BEC-1 architecture is best in terms of power and delay. This architecture can utilize power up to 23.299w and a delay of 11.452ns.

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