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Ternary Circuit Simulation & Design

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ABSTRACT—

The logical data density of contemporary binary digital electronics can barely be further enhanced due to the physical restriction as Moore's Law, which states that the number of transistors in a compact electronic circuit increases every two years, is about to come to an end. Due to its greater variety of logic states than binary, ternary logic is a viable alternative in this regard. In this work, we conduct a thorough analysis of the newly developed ternary logic, ranging from small-scale ternary integrated circuits to individual ternary logic devices. By utilizing the new ternary cycle inverter and the optimized ternary logic, we construct various gates with extremely simple circuits. This study opens new possibilities for the design of ternary integrated circuits and suggests future possibilities for increased logic data density and a reduced chip size

Keywords— Ternary logic, Ternary Logic gate, Ternary system architecture

I. INTRODUCTION

Traditionally, digital computations are performed on two-valued logic named binary logic. The problem with binary logic is interconnection and problem with chip complexity. Multi-valued logic (MVL), however, was first introduced in 1964 and is now recognized as a crucial enabler for high-information-density, next-generation digital electronics. The initial developments of multi-valued logic highlight the major applications of multi-valued logic across various domains.

Multi-valued logic systems lead to saving in the number of interconnections. Due to the availability of the additional bits (logic levels), the wires convey more information. It ultimately reduces the number of pins and leads to their saving. The information stored per memory cell also increases with the use of multi-valued logic. These advantages of multi-valued logic directly contribute to the reduction in the memory and thus the hardware cost.

The significant advantages offered by multi-valued logic of reduced complexity in the design, the smaller on-chip area leading to increased density of fabrication, and high-bandwidth parallel and serial data transfer make it an attractive and a thrust area of research. Ternary logic is a specialized multi-valued logic that demonstrates the use of three significant logic levels 0, 1, and intermediate.

II. Literature Survey

This section discusses some of the current ideas for ternary logic.

[1] The study by **G. V. B. Naidu and N. K. Reddy** in the year **2014** on Ternary logic and multi-valued logic design using nanotechnology devices provides an overview of the advantages and challenges of using ternary logic and multi-valued logic design in the context of nanotechnology devices. The authors argue that ternary logic can provide advantages over binary logic, such as increased information density and reduced power consumption, and that multi-valued logic can provide advantages over binary and ternary logic, such as increased fault tolerance and reduced circuit complexity. The authors then discuss different nanotechnology devices that can be used for ternary and multi-valued logic design, including quantum-dot cellular automata (QCA), carbon nanotube field-effect transistors (CNFETs), and spin-based devices. They also discuss specific design methodologies for implementing ternary and multi-valued logic circuits using these devices, such as the use of threshold logic and majority logic. Finally, the authors provide a comparison of different ternary and multi-valued logic design approaches in terms of power consumption, area, and delay, and highlight some of the remaining challenges in this area, such as the need for efficient synthesis and optimization tools.

[2] The study **by S. Bhattacharya, S. Roy, and S. Chattopadhyay** in the year **2017** on the Design of Ternary Logic Circuits Using Quantum-Dot Cellular Automata presents a design methodology for ternary logic circuits using Quantum-Dot Cellular Automata (QCA) technology. The authors argue that ternary logic can provide advantages over binary logic in terms of reduced circuit complexity and improved power

consumption and that QCA technology can provide a promising platform for implementing ternary logic circuits due to its inherent tolerance to defects and low power consumption. The authors then present a methodology for designing ternary logic circuits using QCA, including the design of ternary gates such as ternary inverters, ternary majority gates, and ternary minority gates. They also present a design methodology for ternary adders and multipliers using QCA technology. The authors evaluate the performance of the proposed ternary logic circuits using QCA technology in terms of power consumption, area, and delay and compare the results with existing binary and ternary logic circuits. The results show that the proposed ternary logic circuits using QCA technology can provide significant improvements in terms of power consumption and area while maintaining comparable performance in terms of delay. Overall, this paper presents a promising approach for designing ternary logic circuits using QCA technology and provides a comprehensive evaluation of the proposed methodology in terms of power consumption, area, and delay.

[3] The study **by S. P. Maity and A. K. Mandal** in the year **2018** on A Comparative Study of Binary and Ternary Adders for Low Power Applications presents a comparative study of binary and ternary adders for low-power applications. The authors argue that ternary adders can provide advantages over binary adders in terms of reduced power consumption and area, and present a design methodology for ternary adders using threshold logic. The authors evaluate the performance of binary and ternary adders using different metrics such as power consumption, area and delay and compare the results using simulation and experimental analysis. The results show that the proposed ternary adder designs can provide significant improvements in terms of power consumption and area while maintaining comparable performance in terms of delay. The authors also evaluate the effect of different factors such as the number of digits, the type of adder, and the input patterns on the performance of binary and ternary adders, and provide insights into the design trade-offs for different applications. Overall, this paper provides a comprehensive comparative study of binary and ternary adders for low-power applications and highlights the potential advantages of ternary adders in terms of reduced power consumption and area.

III. Proposed Methodology

In this architecture using both binary (base-2) and ternary (base-3) representations, the system is built to process input and carry out calculations using ternary logic. The ternary inputs and outputs, however, must be transformed to and from binary form to be compatible with current technology because a majority of modern computers are based on binary logic.

Ternary ALU is useful compared to conventional binary systems as it might improve computing efficiency. Because each ternary digit may represent more states than a binary digit, ternary logic provides a higher information density. This may lead to more efficient execution of specific sorts of calculations and more condensed representations of data. The conversion process between the binary physical addresses used by the binary memory subsystem and the ternary virtual addresses utilized by the ternary logic is handled by the MMU.

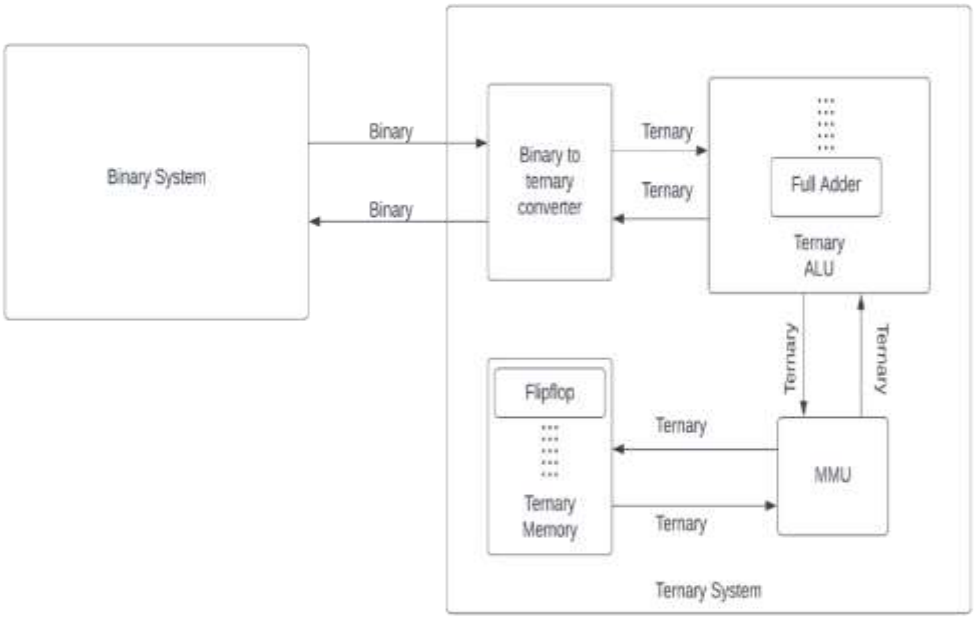

Fig 3.1 System Architecture Diagram

IV. CONCLUSION

Entity	Comparison			
	Parameter	Binary	Ternary	Comments
Clock Signal	Edges	2	4	2 rising edges 2 falling edges
Not gate	Types	1	3	STI, PTI, NTI
Flipflop	Values stored	2	3	(Instead of bit in binary, it is trit in ternary)
Ternary coded decimal	Digits required	4	3	Digits required to store 0-9
Memory	Address Locations	8	9	For example, 8 bits and 9 trits
	Address digits	3	2	
Efficiency	Data stored x = no. of digits	2^x	3^x	2 values for bit, 3 values for trit
	Operating speed	Low	High	Depends on no. of operations
	No. of gates	High	Low	More operations can be done in ternary with less gates.

Fig 4.1 Comparison Table

Traditional digital electronics uses binary logic based on the radix system of 2 while ternary logic uses the radix system of 3. Which has a greater radix economy. In this study, we studied the basic ternary algebra. We implemented this ternary algebra in Ternary circuits. We have successfully simulated the ternary components like Full-Adder, encoder, decoder, multiplexer, and d-flipflop. The motivation behind the simulation of basic ternary circuits is to design and simulate more complex circuits.

V. FUTURE SCOPE

After implementing the above logic circuits in both binary and ternary, results for ternary logic seem promising. With evolving fabrication technologies and discoveries in chemical science ternary gates' benefits may outweigh its drawbacks. Multivalued logic can be also explored for quaternary logic and further, but the noise margin becomes thinner.

Specific applications of logical systems may greatly benefit from specific radix systems. Such applications can be explored.

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