WWW.IJRPR.COM

International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

A Survey on Signal Processing on FPGA Using Hardware Co-Simulation

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ABSTRACT—

The implementation of Signal processing required detailed knowledge of both hardware design and hardware description languages. The purpose of this work is to achieve a real time hardware implementation with higher performance in both size and speed. It focuses on the implementation of an efficient architecture for signal processing algorithms like segmentation (threshold) and contrast stretching by using the fewest possible system generator blocks for DSP tool, which integrates itself with the MATLAB based Simulink graphics environment and relieves the user of the textual HDL programming. The field of very large scale integrated (VLSI) signal processing concerns the design and implementation of signal processing algorithms using application-specific VLSI architecture, including programmable digital signal processors and dedicated signal processors implemented with VLSI technology. Next, one of these representations gets synthesized to its hardware counter- part. The hardware architecture is not only driven by the algorithm representation but also the sampling rate of input/ output signals. Due to limited hardware resources, operations and data of a particular algorithm can be scheduled at the right time and assigned at the right execution unit basis provided that the precedence and semantics are preserved.

Keywords - FPGA, VLSI, Hardware Co-Simulation, MATLAB.

INTRODUCTION

Signal processing techniques are used to optimize transmissions, digital storage efficiency, correcting distorted signals, subjective video quality and to also detect or pinpoint components of interest in a measured signal. The field of very large scale integrated (VLSI) signal processing concerns the design and implementation of signal processing algorithms using application-specific VLSI architecture,including programmable digital signal processors and dedicatedsignal processors implemented with VLSI. The purpose of this project is to achieve a real time hardware implementation with higher performance in both size and speed. It focuses on the implementation of an efficient architecture for signal processing algorithms like segmentation (threshold) and audio or video signal processing by using the fewest possible system generator blocks for DSP tool, which integrates itself with the MATLAB based Simulink graphics environment and Hardware Co-Simulation relieves the user of the textual HDL programming. Hardware Co-Simulation basically involves converting the MATLAB Model into theFPGA readable code with the help of Xilinx's System generator. Now, the FPGA will be programmed using generated the bit file produced by the system generator, and then filter the noisy real-world signal by sending it via the ADC, FPGA, and DAC to the measuring Instrument.

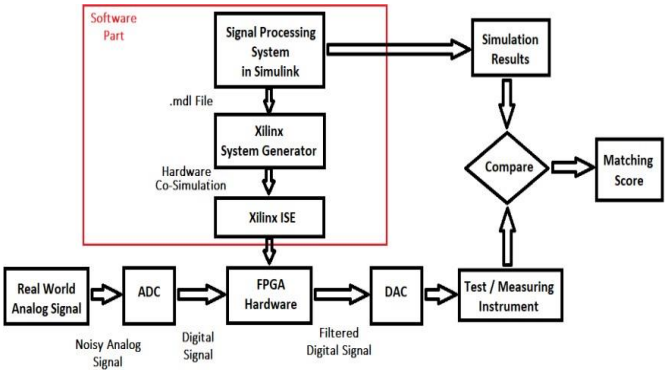

Fig. 1. Signal Processing on FPGA Using Hardware Co-Simulation

LITERATURE SURVEY

Bo Nian Yi [1] describes the implementation of a speech recognition system on an FPGA using hardware co-simulation. The paper presents a hardware/software co-design approachand evaluates the performance of the system using hardware co-simulation. A. L. Shafi et al. [2] presents an FPGA-based system for real-time image processing using hardware co-simulation. The paper describes the system architecture and presents the performance analysis of the system using hardware co-simulation. Owned by, M Mahmoud,[3] W.H. "A Design Methodology for Implementing DSP with Xilinx System Generator for MATLAB presents a survey of design methodologies for FPGA-based signal processing systems. The paper reviews several hardware co-simulation techniques such as HDL co-simulation and Transaction-Level Modeling (TLM) co-simulation and their applicability in FPGA-based signal processing systems. Installing Vitis, Vivado BoardFile [4] by Diligent Reference. This guide walks through the process of installing and configuring the Vivado and Vitis development environments. These applications are used to develop projects to run on Digilent FPGA Development Boards. In addition to the installation, Digilent's Board Support Files will be installed, which are used to make the process of creating a new project significantly faster. Vivado Design Suite User Guide:(UG897) [5] AMD Xilinx. This user guide contains comprehensive instructions and step-by-step guidance for applying and running projects in the Xilinx Vivado. Vitis Model Composer userguide by AMD Xilinx [6] this user guide covers Developing PL IP blocks for the hardware platform, as well as PL kernels, functional simulation, and analysing time, resource utilisation, andpower closure. It also entails creating the hardware platform for system integration. This document's topics that pertain to this design process include:

1)Hardware Design using the HDL Library
2)Designing a Model Composer
3)HDL Library Design

DESIGN FLOW

The Vitis model Composer is set up for an appropriate FPGA board. Any appropriate FPGA board, such as the Spartan7 XC7S50-CSGA324, may be used in this situation. I/O and clock planning have been completed, and the model has been put into practice for JTAG hardware co-simulation. The parameters for the Vitis model composer are chosen and produced. A draught of the model and programming file in Verilog HDL are generated during compilation and can be viewed using Xilinx ISE. The module is synthesized, implemented on an FPGA, and has its behavioral syntax validated. User constraints files (UCF), test benches, and test vectors can all be generated by the Xilinx System Generator itself to test an architecture. Although it has other uses related to this theme, such as signal processing, Xilinx System Generator was initially developed to deal with sophisticated Digital signal processing (DSP) applications. It is important to do bitstream compilation to produce an FPGA bit file that is acceptable for FPGA input.

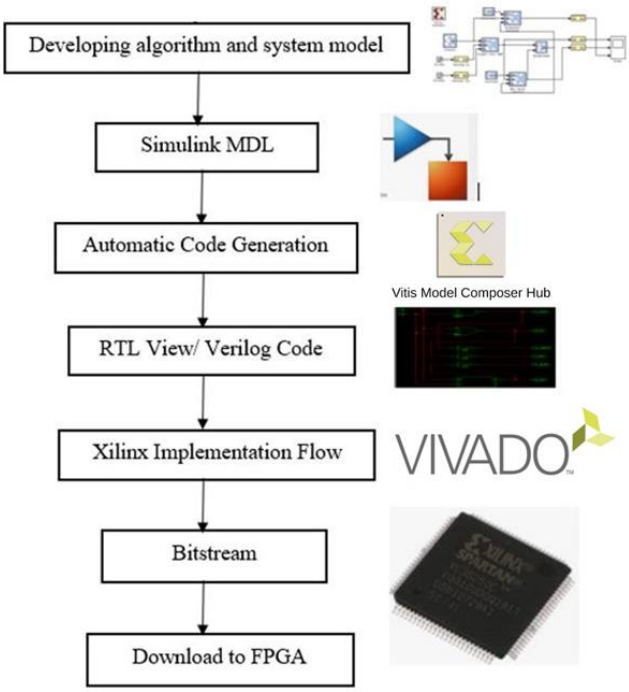

Fig. 2. Design flow for Signal processing with Vitis Model Composer.

FUTURE PROSPECTS

The upcoming technology is signal processing. Many young people worry about how technology may affect their ability to find employment in the future. Main aim is to design filter model and generate the VHDL program using Hardware co-simulation. VHDL code in MATLAB using the HDL compiler in system will be produced. Then, using the generated VHDL code to program the FPGA kit. The FPGA kit will then be used to filter noise from real-world analog signals. To do this, we will first send the noisy analog signal via the Analog to Digital Converter, and then apply the digital output to the Filter. This Filtered output will also be routed via a Digital to Analog Converter to produce a noise-free signal.

CONCLUSION

In this paper, we have reviewed the methods so far proposed by several authors for Signal Processing on FPGA Using Hardware Co-Simulation. We also reviewed various review papers for the hardware Co-simulation Techniques. Many papers suggested multiple approaches for performingHardware Co-simulation. This study leads us to the conclusion that the Xilinx Vitis Model composer is a flexible tool for both software- and hardware-based signal processing tasks. It offers quick ways to perform complicated signal processing algorithms on hardwarewith the least amount of time and resources. Due to this the implementation of Hardware is made simple and straightforward.

ACKNOWLEDGMENT

We take this opportunity to express our sincere thanks to our guide respected Mr. H. S. Thakar sir for their support and encouragement throughout the completion of this project. We are grateful to him for his constant support.

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