WWW.IJRPR.COM

International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

Ternary Gate Circuit Simulation & Design

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ABSTRACT —

The logical data density of contemporary binary digital electronics can barely be further enhanced due to the physical restriction as Moore's Law, which states that the number of transistors in a compact electronic circuit increases every two years, is about to come to an end. Due to its greater variety of logic states than binary, ternary logic is a viable alternative in this regard. In this work, we conduct a thorough analysis of the newly developed ternary logic, ranging from small-scale ternary integrated circuits to individual ternary logic devices. By utilizing the new ternary cycle inverter and the optimized ternary logic, we construct various gates with extremely simple circuit. This study opens new possibilities for the design of ternary integrated circuits and suggests future possibilities for increased logic data density and a reduced chip size.

***Index Terms*— Ternary logic, Ternary Logic gate, Ternary system architecture**

1. INTRODUCTION

Traditionally, digital computations are performed on two-valued logic named as binary logic. The problem with binary logic is interconnection and problem on chip complexity. Multi-valued logic (MVL), however, was first introduced in 1964 and is now recognized as a crucial enabler for high-information-density, next-generation digital electronics. The initial developments of multi-valued logic and highlights the major applications of multi-valued logic across the various domains.

Multi-valued logic systems lead to saving in the number of interconnections. Due to the availability of the additional bits (logic levels), the wires convey more information. It ultimately reduces the number of pins and leads to their saving. The information stored per memory cell also increases with use of multi-valued logic. These advantages of multi-valued logic directly contribute to reduction in the memory and thus the hardware cost.

The significant advantages offered by multi-valued logic of reduced complexity in the design, smaller on chip area leading to increased density of fabrication and high-bandwidth parallel and serial data transfer make it an attractive and a thrust area of research. Ternary logic is a specialized multi-valued logic that demonstrates use of three significant logic levels 0, 1 and intermediate.

Ternary logic, sometimes referred to as three-valued logic or the radix-3 number system, is one of the unique features of multi-valued logic. It indicates that it has three switching states: intermediate, zero, and one.Ternary logic has an advantage over binary logic in that it can answer majority of complicated problems. Ternary logic can be applied to boost data transmission across a specific number of lines, increase data storage for a specific register length, and reduce complexity.

The ternary gates are:

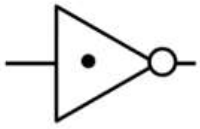

Fig 1.1 Standard Ternary Inverter (STI)

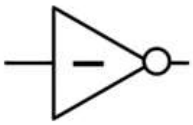

Fig 1.2 Negative Ternary Inverter (NTI)

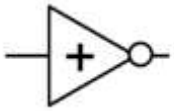

Fig 1.3 Positive Ternary Inverter (PTI)

INPUT X	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

Table 1.1 Truth table of STI, NTI, PTI

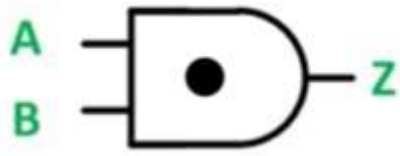

Fig 1.4 Ternary AND gate

A ^ B		B		
		0	1	2
A	0	0	0	0
	1	0	1	1
	2	0	1	2

Table 1.2 Truth table of Ternary AND gate

Fig 1.5 Ternary OR gate

A v B		B		
		0	1	2
A	0	0	1	2
	1	1	1	2
	2	2	2	2

Table 1.3 Truth table of Ternary OR gate

2. Methodology

2.1 System Architecture

In this architecture using both binary (base-2) and ternary (base-3) representations, the system is built to process input and carry out calculations using ternary logic. The ternary inputs and outputs however, must be transformed to and from binary form in order to be compatible with current technology because majority of modern computers are based on binary logic.

Ternary ALU is useful compared to conventional binary systems as it might improve computing efficiency. Because each ternary digit may represent more states than a binary digit, ternary logic provides a higher information density. This may lead to more efficient execution of specific sorts of calculations and more condensed representations of data. The conversion process between the binary physical addresses used by the binary memory subsystem and the ternary virtual addresses utilized by the ternary logic is handled by the MMU.

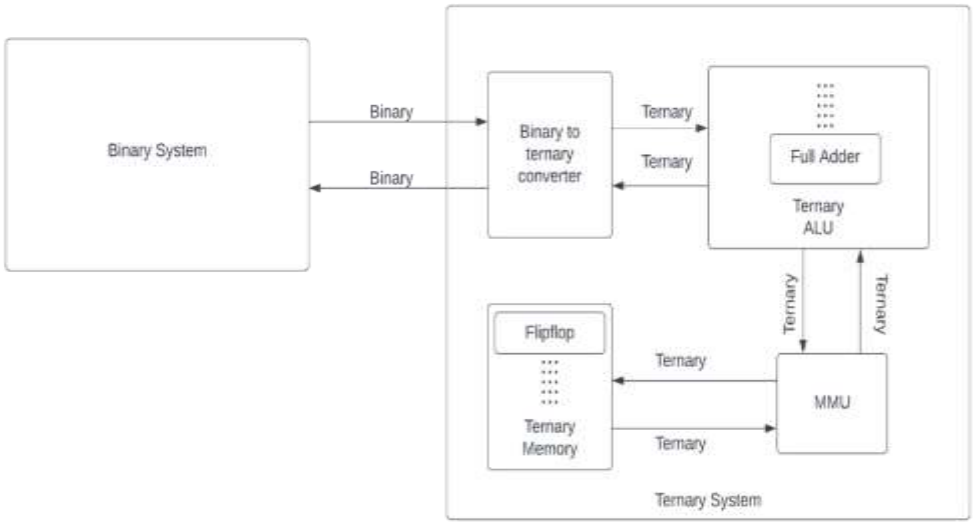

Fig 2.1 System Architecture Diagram

2.2 Binary to ternary Converter

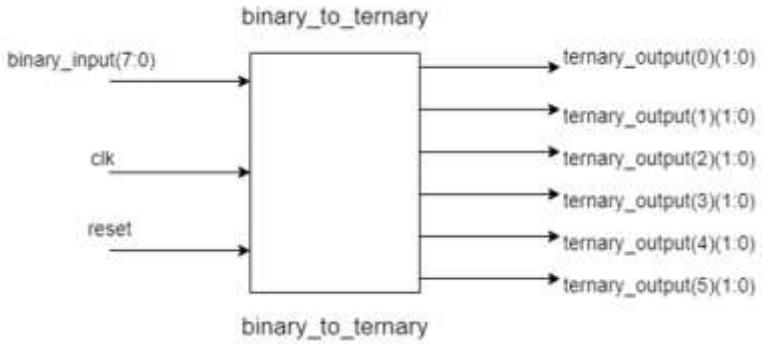

Fig 2.2 Block diagram binary to ternary converter

Signal	Binary_input	clk	reset	ternary_output
Description	8-bit Input data	Clock pulse (6.25 MHz) (std_logic)	This ensures that the system starts with a known value for decimal input	5-bits output data (T0 – Ternary 0) (T1 – Ternary 1) (T2 – Ternary 2)

Table 2.1 Table for binary to ternary converter

2.3. Ternary to binary Converter.

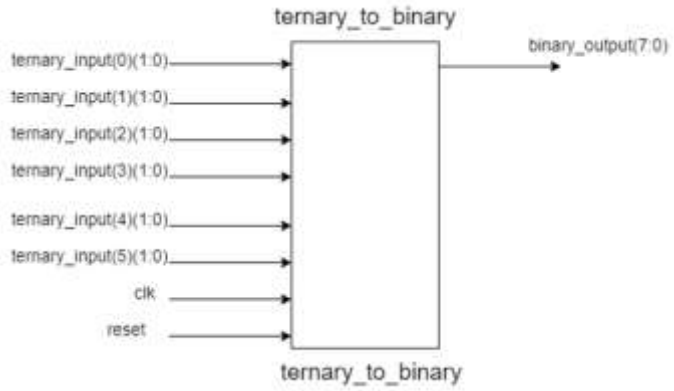

Fig 2.3 Block diagram ternary to binary converter

Signal	ternary_input	clk	reset	Binary_Output
Description	5-bits output data (T0 – Ternary 0) (T1 – Ternary 1) (T2 – Ternary 2)	Clock pulse (6.25 MHz) (std_logic)	This ensures that the system starts with a known value for decimal input	8-bit Input data

Table 2.2 Table for ternary to binary converter

2.4 ALU.

Signal	x	y	f	w	bc
Description	Input1 (Decimal)	Input2 (Decimal)	Operation (Decimal) (1=or,2=and,3=nor,4=nand, 5=xor,6=xnor,7=add,8=subtract)	Output (Decimal)	Borrow/ Carry

Table 2.3 Table of 4trit-ALU operation

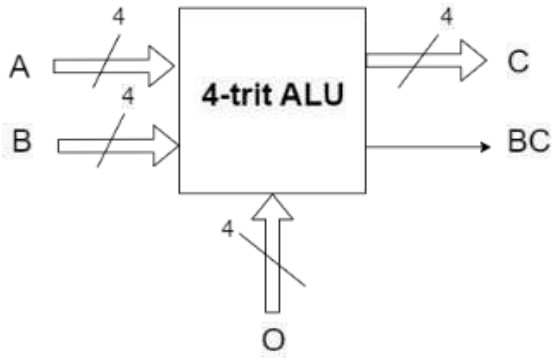

Fig 2.4 Block Diagram of 4trit-ALU

Signal	a	b	o	c	bc
Description	Input1 (4-Trit)	Input2 (4-Trit)	Operation (4-Trit)	Output (4-Trit)	Borrow / Carry (Trit)

Table 2.4 Table of 4trit-ALU

2.5 Implemented, tested & simulated ternary D-flipflop:

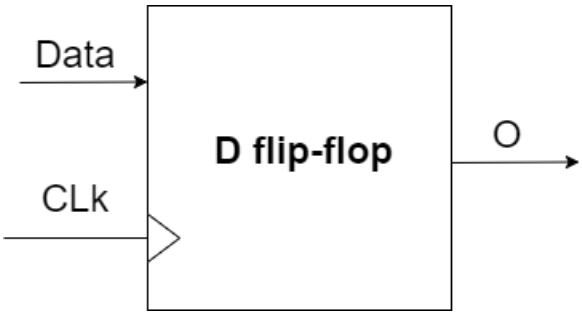

Fig 2.5 Block diagram of ternary D-flipflop

Signal	clk	data	o
Description	Clock pulse (6.25 MHz) (std_logic)	Input (trit)	Output (trit)

Table 2.5 Table of ternary D-flipflop

2.6 Implemented, tested & simulated Ternary Memory Management Unit

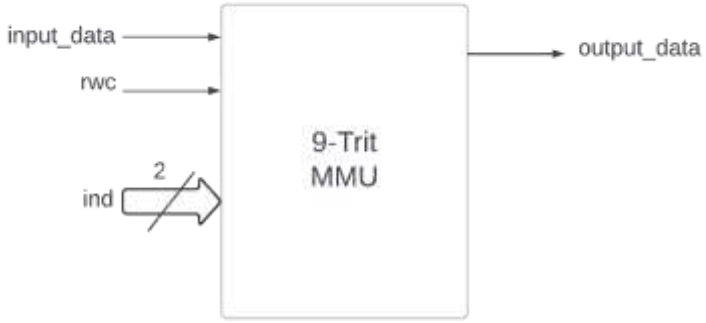

Fig 2.6 Block Diagram for Ternary Memory Management Unit

Signal	ind	input_data	memory	output_data	rwc
Description	index	index	storage	output	read/ write/ clear signal

Table 2.6 Table for Memory Management Unit.

3. Working

Binary system will send data in binary. Binary to ternary converter will convert the signal into ternary. The signal will be sent to ALU for processing. ALU will do the memory independent operations and work with MMU for operations on memory. MMU will use ternary address and use ternary memory with ternary flipflops. Finally, the result is converted back into binary and sent back to binary system.

4. Results and Discussions

4.1. Binary to Ternary Converter

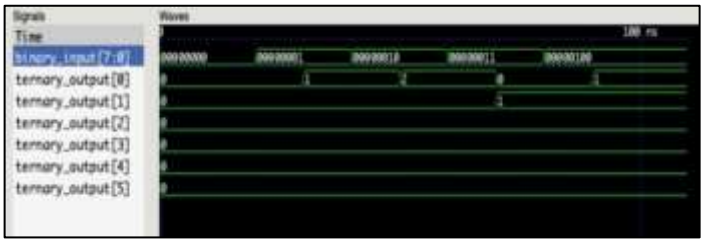

Fig 4.1 Waveform of Binary to Ternary Converter

4.2. Ternary to Binary Converter

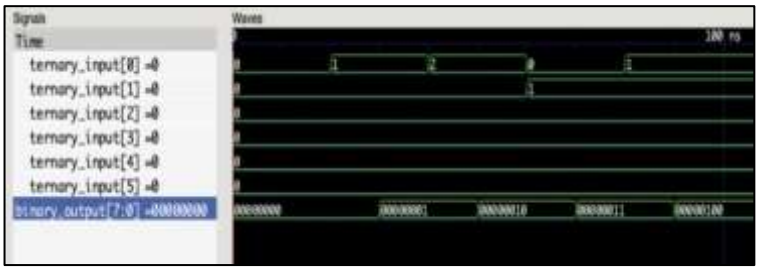

Fig 4.2 Waveform of Ternary to Binary Converter

4.3. ALU

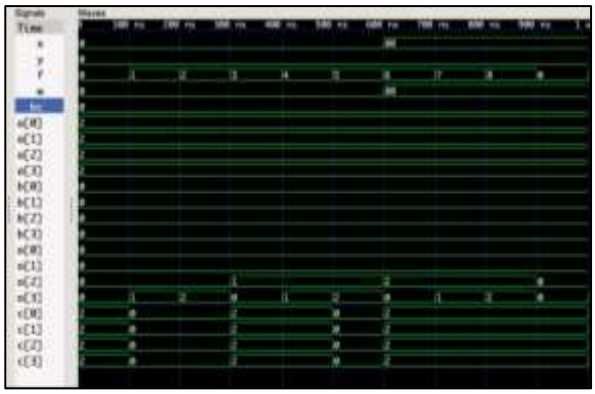

Fig 4.3 waveform of ALU

4.4. Ternary D-flipflop

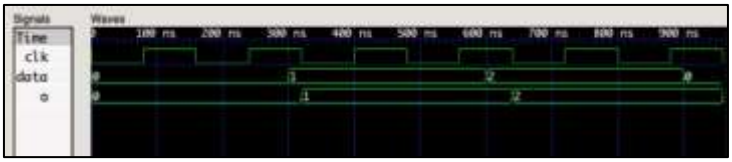

Fig 4.4 Waveform of Ternary D-flipflop

4.5. Ternary Memory Management Unit

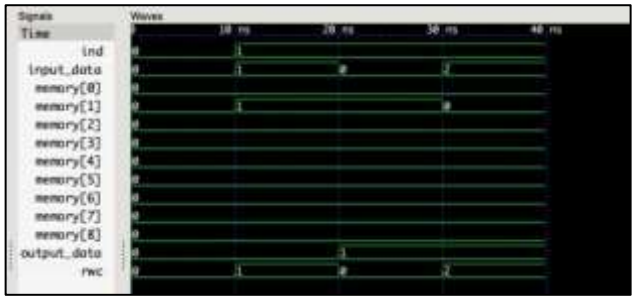

Fig 4.5 Waveform of Ternary Memory Management Unit

5. CONCLUSION

Entity	Comparison			
	Parameter	Binary	Ternary	Comments
Clock Signal	Edges	2	4	2 rising edges 2 falling edges
Not gate	Types	1	3	STI, PTI, NTI
Flipflop	Values stored	2	3	(Instead of bit in binary, it is trit in ternary)
Ternary coded decimal	Digits required	4	3	Digits required to store 0-9
Memory	Address Locations	8	9	For example, 8 bits and 9 trits
	Address digits	3	2	
Efficiency	Data stored x = no. of digits	2^x	3^x	2 values for bit, 3 values for trit
	Operating speed	Low	High	Depends on no. of operations
	No. of gates	High	Low	More operations can be done in ternary with less gates.

Fig 5.1 Comparison Table

The traditional digital electronics uses binary logics based on radix system of 2 while ternary logic uses radix system of 3. Which has greater radix economy.

In this study we studied the basic ternary algebra. We implemented this ternary algebra in Ternary circuits. We have successfully simulated the ternary components like ALU, Ternary to binary converter, binary to ternary converter D-flipflop. The motivation behind the simulation of basic ternary circuits is to design and simulate more complex circuits.

6. FUTURE SCOPE

After implementing above logic circuits in both binary and ternary, results for ternary logic seem promising. With evolving fabrication technologies and new discoveries in chemical science ternary gates' benefits may outweigh its drawbacks. Multivalued logic can be also explored for quaternary logic and further, but noise margin becomes thinner.

Specific applications of logical systems may greatly benefit from specific radix system. Such applications can be explored.

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