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IMPLEMENTATION OF GDS-2 LAYOUT FROM A DESIGNED NETLIST USING PHYSICAL DESIGN FLOW

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ABSTRACT—

The process of converting a circuit description into a physical layout, which specifies the locations of cells and the paths used for their connections, is known as physical design. Finding a layout with a small footprint and reducing overall wire length are the key goals in VLSI chip physical design. In order to meet design requirements like performance, power and area (PPA), the physical design is all about inserting instances defined in the net list and linking them through routing through the metal layer stack. Current IC designs feature has millions of interconnected instances that are joined by a number of metal layer stacks. It is impossible , extremely time consuming, and prone to error to carry out every step of the design process manually. Because of the enormous complexity involved in building a multi-million instance based IC, we require Specialized automation processes to carry out the specific duties required at each stage of the design , hence reducing design time and errors. These flows demand an understanding of familiarity with EDA technologies.

Keywords—Automation tool, Moore's law, Multi-million Instance, EDA technologies.

INTRODUCTION

There are several stages in the design cycle for VLSI- chips, from high level synthesis to manufacturing [1].The physical design is the first step in turning a circuit description into physical layout that specifies the locations of cells and the pathways used for their connections [2]. Finding a layout with a limited area and a minimum total wire length are the two fundamental goals in the physical design of VLSI-1 chips[3].To meet design requirements like performance, ower and area (PPA), physical design consists of installing instances specified in the netlist and linking them by routing across the metal layer stack [4].Current IC designs feature has millions of interconnected instances, each of them joined by a stack of metal layers [5]. It is not possible , takes a lot of time, and is mistake prone to carry out every step of the design process manually [6]. Because building a multi million instance based Ic is so complex . we need specialized automation flows to carry out the precise duties that must be done at each stage of the design, which cuts down on design time and mistakes [7]. These flows demand an understanding of and familiarity with EDA technologies [8]. According to Moore's law , a dense integrated circuit's transistor count doubles roughly every two years [9]. Gordon More , the co-founder of Fairchild semiconductor and CEO of intel, published a paper in 1965 that described the number of components per integrated circuit as doubling annually and predicted this rate of expansion would continue for at least another ten years. Moore's observation bears his name[10]. Expecting double every two years in 1975 [11]. Because of prediction made by Intel executive David House, the duration is frequently stated as 18 months [12].

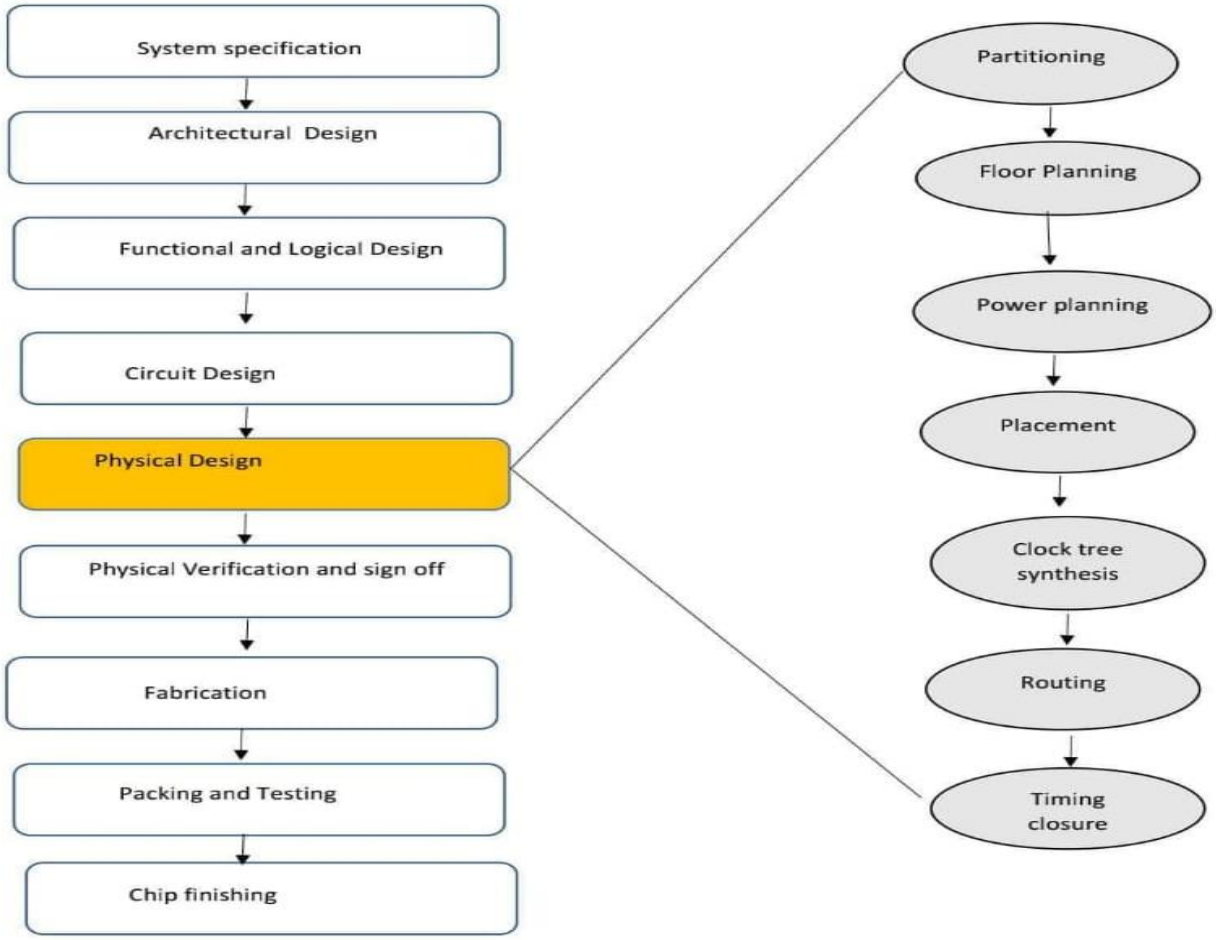

Fig:1 The Architecture Of The Physical Design

ARCHITECTURE

Physical Design

In the IC Design Cycle, Physical Design or Backend Design is the step which follows the circuit design. It is the process which transforms a digital circuit representation into a physical layout. The circuit representation are converted to geometric description of shapes with various metal layers and when manufactured, the metal layers will ensure the functioning of the circuit. The inputs to Physical Design are a netlist, library information of the cell the design, a technology file with the manufacturing and timing constraints.

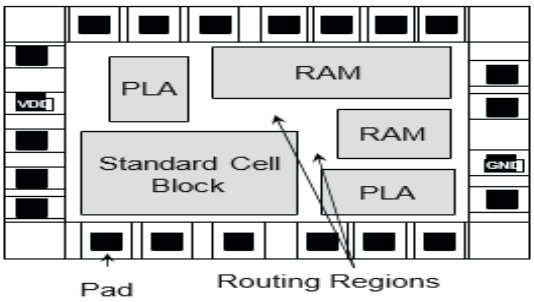

Fig 2. Example layout with macro cells

Significant Aspects of Physical design

The role of physical design significantly increased in 90s.The two main reasons for the dominant increases are .
Deep submicron scaling
Interconnect optimization

Steps in physical Design

The main steps in physical design are

- Floor planning & Power planning
- placement
- Clock Tree Synthesis
- Routing
- Static Timing Analysis
- Physical Verification

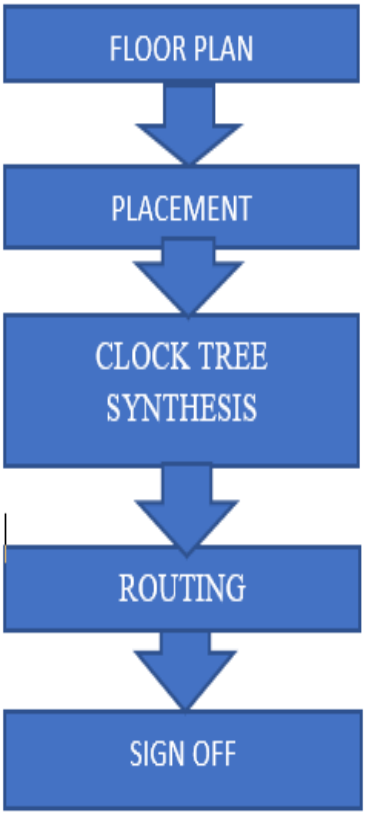

Fig 3: Physical Design Flow

Floor Planning

Floor planning is the critical and first step in physical design. It helps to define the size of the chip, determine macro Placement, I/0 pads placement ,etc. Objectives of Floor planning are to minimize the chip area and wire length. Modules which communicate very often should be placed closed to each other in order to reduce the routing resources. The other steps of physical design like placement, routability and timing closure depends on a well thought-out floorplan. A bad floorplan contributes to routing congestion and problems in timing closure, Which in turn results in increase of area and power.

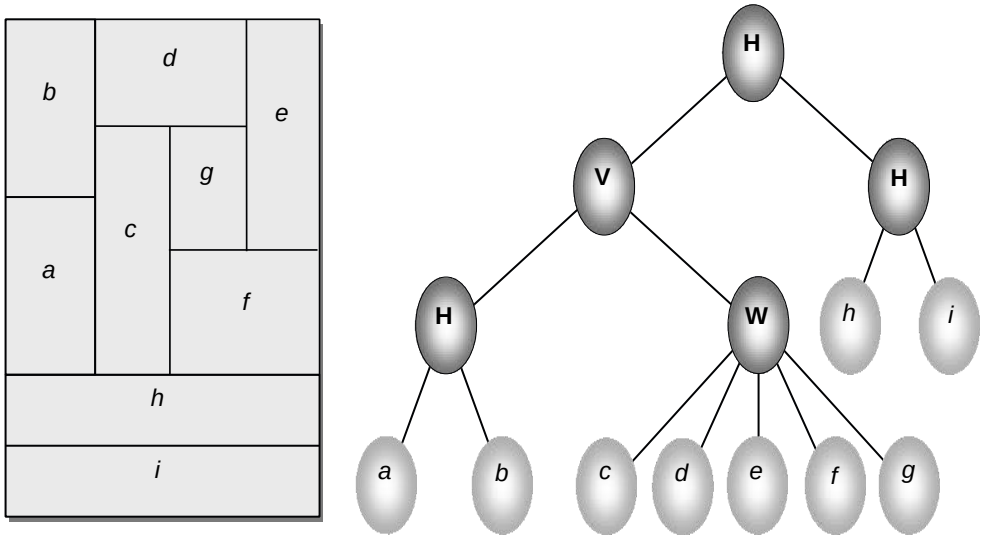

Fig 4: A hierarchical floorplan (left) and its corresponding floorplan tree of order five(right).The internal mode w represents a wheel with blocks c-g.

Power planning

Power planning is a step to be executed along with floor planning to create the power grid network and make sure that power is distributed evenly in the chip. The chip usually has power strips, block rings and power rails. Block rings connects VDD and VSS from the block rings across the chip(highest metal layer).Power rails connects VDD and VSS to the VDD and VSS of the standard cells (lowest metal layer).
Power planning involves

- The number and width of rings and stripes
- Proper connection of power stripes to the Power pins in the macros, standard cells, etc.
- Efforts to achieve low IR drop.
- Check all the cells are properly connected to power or not.
- Power plan metal layers do not have DRC
- Violations.

Power Calculations

- **Number of the core power pad required for each side of chip**=(Total core power) / {(number of side)*(core voltage)*Maximum allowable current For A I/O Pad)}
- **Core P/G Ring width** = (Total core current) / {(No.of sides)*(Maximum current density of metal layer used for Pg Ring)}
- **No.of Power Pads(Npads)**= Itotal /Ip
- **No.of Power Pins**= Itotal/Ip

Where,

Itotal=TOTAL Current

Ip obtained from Io Library specification

- **Total current** =Total Power consumption of chip(p)/voltage.

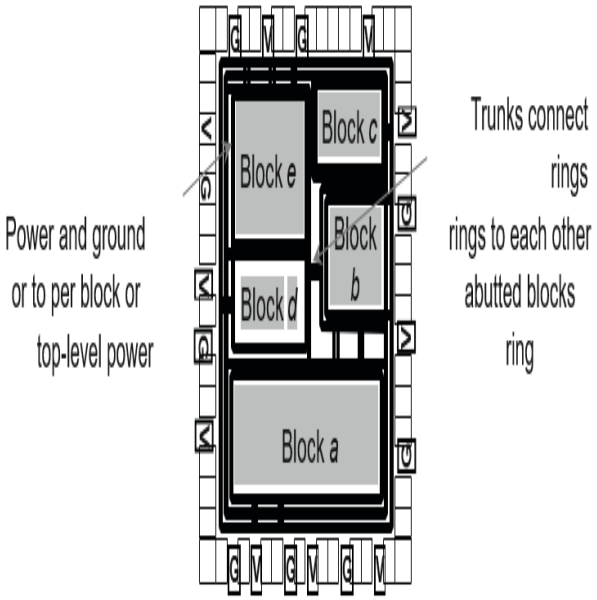

Fig 4. Custom style of power-ground distribution for a chip floorplan

Placement

Placement is very important for the following reasons:

- To determine the performance of the circuit
- To determine the power consumption of the design
- To determine the routing ability of the design
- To minimize the cell density
- To minimize timing DRC's
- Placement od standard cells takes place in this step
- Congestion and Timing are the two main constraints taken into consideration during placement of standard cells.
- Placement of standard cells should be aligned with the power rails drawn in floorplan step.

Clock Tree Synthesis

Clock Tree Synthesis (CTS) is one of the most important stages in PnR. CTS QOR decides timing convergence & power. In most of the ICs clock consumes 30-40 % of total power. So efficient clock architecture, clock gating & clock tree implementation helps to reduce power.

The process of distributing the clock and balancing the load is called CTS. Basically, delivering the clock to all sequential elements. CTS is the process of insertion of buffers or inverters along the clock paths of ASIC design in order to achieve zero/minimum skew or balanced skew. Before CTS, all clock pins are driven by a single clock source. CTS starting point is clock source and CTS ending point is clock pins of sequential cells.

CTS Quality Checks:

- Minimize insertion delay
- Skew Balancing
- Duty Cycle
- Pulse Width
- Clock Tree Power Consumption

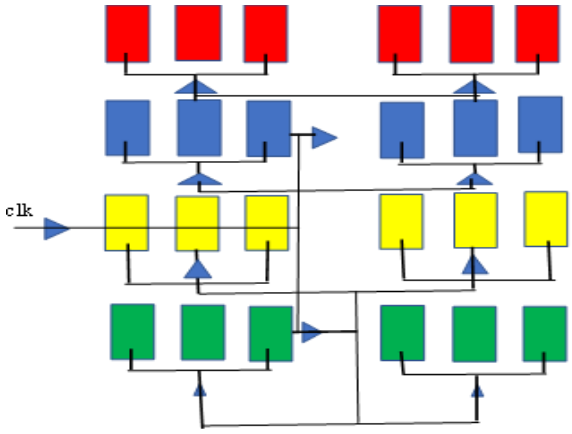

Fig 5: Clock Tree Synthesis

Static Timing Analysis (STA)

Static Timing Analysis is a process to check that the design is free from timing violations. Timing is very important in the design process ,as we need to know Fast a chip can operate ,how fast the input reaches the output and how well the chip can interact with other devices in the system Floor planning placement ,CTS and routing contribute to timing violations in the design. Hence, timing check is implement throughout the flow of physical design. The STA tool analyzes all the timing paths from their start point to the endpoint and compares it with the constraints of that particular path. The main goal of STA is to make sure that the all the signals propagate well through the circuit and the design can work at the required frequency without any timing violations. Types of Paths for timing analysis are Data path, clock path, clock gating path.

Routing

Routing is the process for allocating set of wires in the routing region which connects all the signal nets in the netlist using metal shapes and vias.The objective of routing is to minimize total wire length ,number of layer changes and number of vias. The routing channels should be well utilized and proper care should be taken to avoid congestion in the design. A good routed design will meet timing requirements and will have less number of violations in the physical verification checks.

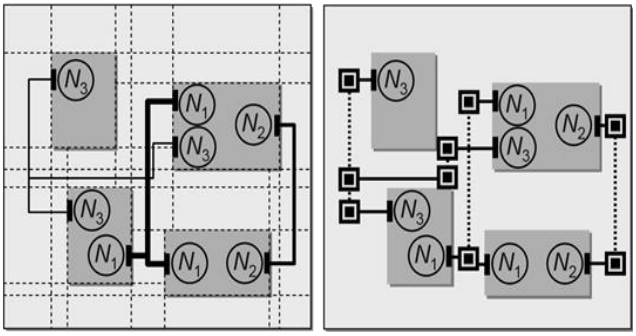

Fig 6. Global routing Detailed Routing

Physical Verification

Physical Verification is the final process to ensure that the design is ready for fabrication and all the design rules are met. Functionality checks should also be performed to ensure that the functionality of the design is not changed, during the flow of physical design . The layout should meet the spacing rules between metals, minimum width rules and also, should be clean from shorts and opens. Design Rule Check(DRC), layout vs Schematic check (LVS) , Electric Rule Checks(ERC),antenna, latchup, XOR check, logic equivalence check(LEQ) are some of the major physical verification checks. Any physical defects observed in the design will result in non-functionality of the product.

J. Power Analysis

The biggest challenge of the industry is power integrity closure. Shrinking of design in the recent technology nodes have contributed to this challenge. Power-Static and Dynamic

Static power is the power calculated when there is no activity in the design. Dynamic power is calculated when the design is active.IR (voltage drop) and Electro Migration (EM) are the two parameters to be met in power analysis. Power integrity issues can be usually fixed by either adding additional power stripes or by widening the width of metal layers . A good power grid results in faster power integrity closure.

CONSTRUCTION OF UNIT

This Visual Diagram visualizes the placement of all modules on the chip/core. It involves determining the shape and size of modules in a chip and estimates the chip area,delay and the wiring congestion and thereby providing a ground work for layout.

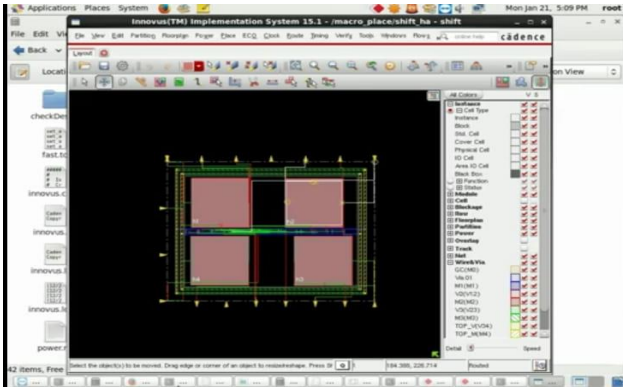

Fig 7: Floor Planning

Power grid network is created on the chip/core. It determines the layout of the power-ground network and the placement of I/O pads as shown in the fig.5

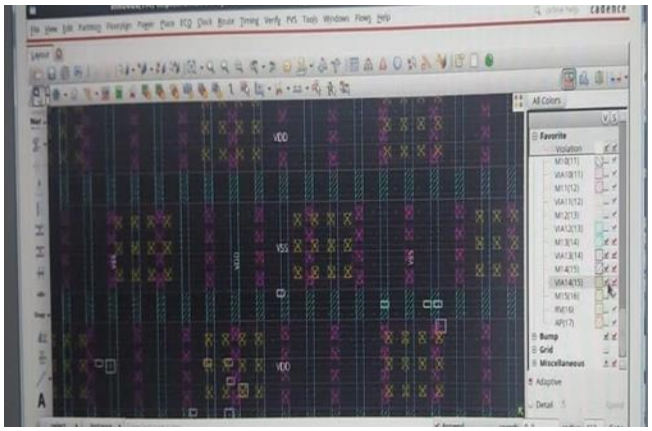

Fig 8. Power Planning

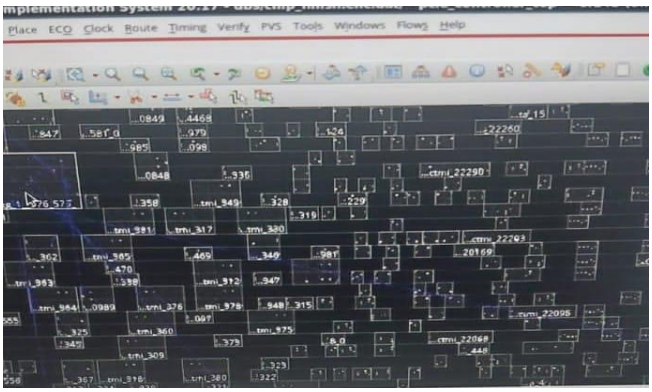

Fig 9. Placement

Arrangement of standard cells taken place in fig.9. The tool determines the location of each standard cell on the die. The tool places these based on the algorithms which it uses internally.

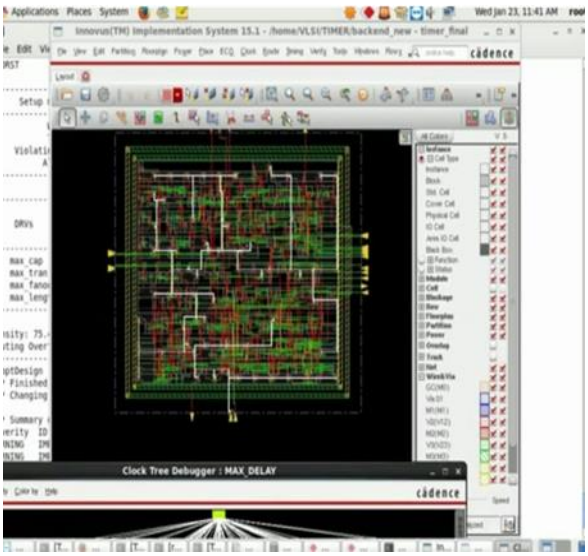

Fig 10. Clock Tree Synthesis

Fig .7 shows the distribution of clock equally among all flipflops on the chip/core. Buffers are getting added during clock tree synthesis.

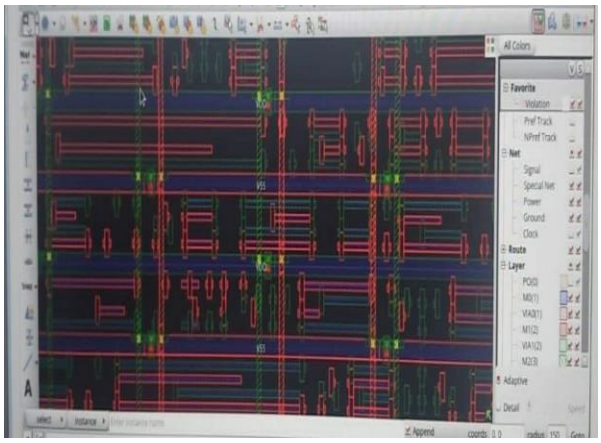

Fig 11. Routing

Making of connections between modules and standard cells using metal layers following CTS is depicted in fig.8.

RESULT

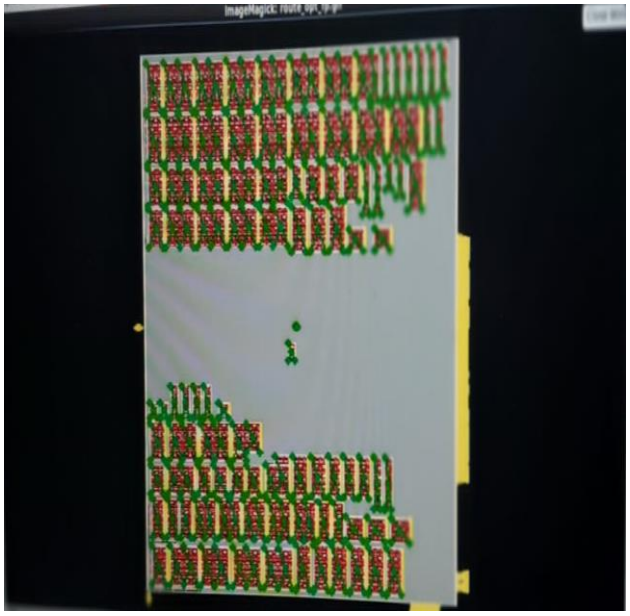

Fig 12. GDS 2 Layout

This picture shows the binary file format that represents the graphical data stream (GDS 2) layout as a result of physical design process.

CONCLUSION

Assuming that private industry will take the lead in mainstream product development and short term research ,the steering committee presents here recommendations for research agencies should encourage. Federal research agencies should encourage. Federal initiatives that emphasize long term goals beyond the horizon of most commercial efforts and that may thus entail added risk have the potential to move the whole information technology enterprise into new models of thinking and to stimulate discovery of new technologies for the coming century. Of Course, work should continue in current areas that have demonstrated promise ,but the emphasis here is on opening up new opportunities.

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