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Low Power Encoding Technique for Network on Chip

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A B S T R A C T

TThis paper explores data encoding techniques for reducing energy consumption in Network-on-Chip (NoC) architectures. NoCs are critical components in modern computing systems that connect processing elements and memory units. However, the high energy consumption of NoCs is a major concern, especially in mobile and embedded systems. In this study, various encoding techniques are analyzed and evaluated in terms of energy consumption reduction and performance impact. The results show that these techniques can significantly reduce the energy consumption of NoCs while maintaining acceptable levels of performance. The findings of this study can guide the design of energy-efficient NoCs for future computing systems.

1.1 INTRODUCTION

The continuous demand for higher performance and more functionality in modern computing systems has led to the proliferation of complex and interconnected architectures such as Network-on-Chip (NoC). NoCs provide a scalable and efficient communication infrastructure that interconnects various processing elements and memory units in a system-on-chip (SoC) design. However, the energy consumption of NoCs is a major concern, particularly in mobile and embedded systems where energy efficiency is critical. To address this challenge, various data encoding techniques have been proposed to reduce the energy consumption of NoCs. This paper provides an overview of these techniques and evaluates their effectiveness in reducing energy consumption while maintaining acceptable levels of performance.

2. LITERATURE REVIEW

1)Crosstalk avoidance and error correction coding for coupled RLC interconnects," in Proc. IEEE Int. Symp. Circuits Syst., May 2009, pp. 141– 144

AUTHORS : M. S. Rahaman and M. H. Chowdhury

As device densities and operational clock frequencies have increased in deep sub-micrometer (DSM) VLSI circuits, on-chip interconnect delay and crosstalk noise have taken on increased significance for performance and signal integrity. Interconnects exhibit a significant inductive impact compared to capacitive effect, with quicker rising times and less resistance. As a result, several existing coding approaches for resistive-capacitance (RC) interconnects that reduce capacitive crosstalk are not appropriate for resistive-inductance-capacitance (RLC) interconnects in high-speed circuits. On-chip interconnects are also vulnerable to several types of DSM noise. Interconnect reliability against DSM noise is enhanced via error-correction coding (ECC). The improved boundary shift coding method that is suggested in this study handles both error-correction and noise reduction for coupled RLC interconnects with inductance-dominant crosstalk. Results demonstrate that recommended coding succeeds by up to 50%.

2) Multiprocessor system-on-chip MPSoCtechnology ," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 10, pp. 1701–1713, Oct. 2008

AUTHORS : W. Wolf, A. A. Jerraya, and G. Martin

The multiprocessor system-on-chip (MPSoC) implements a system using multiple CPUs as well as other hardware subsystems. Over the past ten years, a variety of MPSoC architectures have been created. In order to make the case that MPSoCs are a significant and distinctive type of computer architecture, this paper covers the history of MPSoCs. We look at a few of the technological developments that influenced MPSoC design. We also look at computer-aided design issues associated with MPSoC design.

3) Error Detection in Majority Logic Decoding of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes," IEEE Trans. Very Large Scale Integra. (VLSI) syst., vol. 21, no. 1, pp.156- 159, Jan. 2013.

AUTHORS : Pedro Reviriego, Juan A. Maestro, and Mark F. Flanagan

A technique to speed up the majority logic decoding of difference set low density parity check codes was recently put out in a publication. This is advantageous since majority logic decoding may be carried out serially with basic hardware but takes a long time. This lengthens the time it takes to access memory for memory applications. In the initial rounds of majority logic decoding, the method checks each word for errors; if there are none, decoding is stopped without finishing the remaining iterations. The average decoding time is significantly shortened because the majority of words in a memory will be error-free. In this succinct article, we examine the application of a similar technique to a type of low density parity check (EG-LDPC) codes that use Euclidean geometry.

3. REQUIREMENTS SPECIFICATION

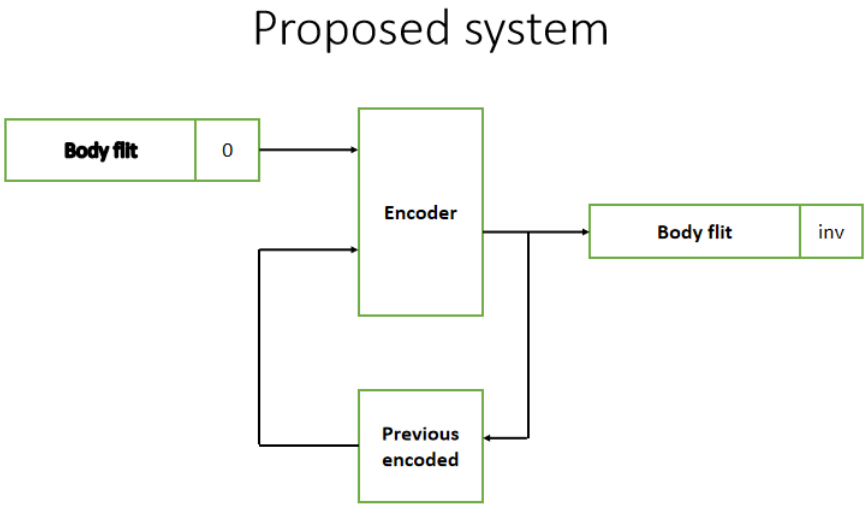
3.1 Hardware Requirements:

System	:	Intel core i5 Processor.
Hard Disk	:	1000 GB.
Monitor	:	15'' LED
Input Devices	:	Keyboard, Mouse
Ram	:	8 GB

3.2 Software Requirements

Operating system	:	Windows 8,10
Coding Language	:	Xilinx
Web Framework	:	VLSI

4. SYSTEM ARCHITECTURE



- Here we are directly using encoder in that encoder we are using LDPC – (Least density parity checker) technique
- IN LDPC there is no Counter logic and comparator logic.
- It is a pipeline architecture it means all the inputs will be processed parallely, So the output will generate very fast.
- Body flit means input and Output is inverter body flit.
- In encoder One data is converted into another data.

- IN Proposed system Diagram we are using two encoders
- 1.Encoder 2.Previous encoded
- So the previous encoder value is used to getting more accuracy encoding.
- Here no delay is occur.

IMPLEMENTATION :

- The proposed system will be implemented on an FPGA or ASIC platform to demonstrate its feasibility and practicality. The implementation will be used to evaluate the performance of the proposed system in real-world applications.
- For example, in a study conducted by Zheng , the authors proposed a transition coding scheme that reduced energy consumption by up to 60% compared to traditional binary encoding. Similarly, a study conducted by Sanaei showed that Manchester encoding reduced energy consumption by up to 20% compared to binary encoding.

MANCHESTER CODING

- Manchester coding is a self-clocking encoding technique that is commonly used in communication systems.
- In this technique, each bit is encoded as a transition from high to low or from low to high, which creates a clock signal that is synchronized with the data signal.
- Manchester coding doubles the data rate and eliminates the need for a separate clock signal, but it increases the power consumption due to the increased number of transitions.

RUN LENGTH CODING

- Run-length coding is a technique that reduces the number of transitions in the data signal by encoding repeated sequences of 0s or 1s as a single bit.
- For example, if there are three consecutive 0s, they can be encoded as a single 0.
- Run-length coding is simple and efficient, but it is limited to data patterns with long runs of identical bits.

DIFFERENTIAL MANCHESTER CODING

- Differential Manchester coding is a variation of Manchester coding that reduces power consumption by encoding the data based on the transition between bits, rather than the bit value.
- In differential Manchester coding, a transition at the beginning of a bit represents a 1, while a transition in the middle of a bit represents a 0. This technique eliminates the need for a separate clock signal and reduces power consumption, but it requires more complex decoding.

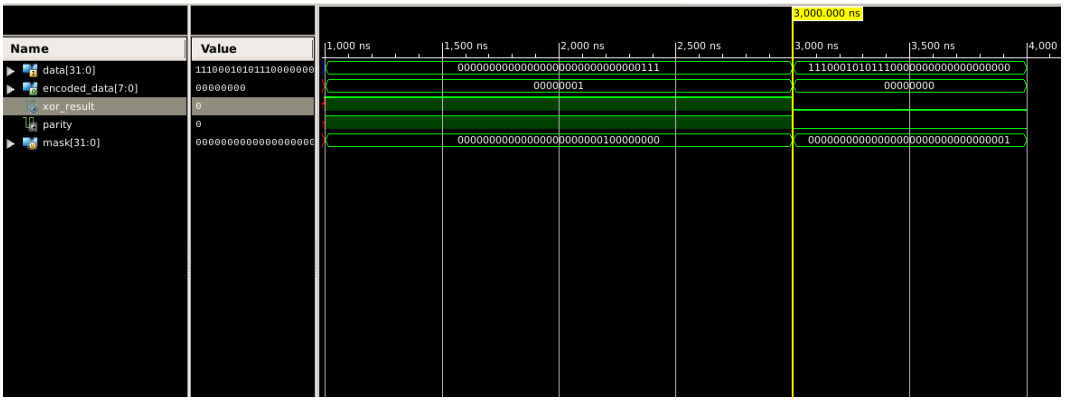
PARITY CHECK CODING

- Parity-check coding is a technique that adds a parity bit to the data to detect errors in transmission. The parity bit is calculated based on the number of 1s in the data, and it is appended to the end of the data.
- The receiver calculates the parity bit based on the received data and compares it to the transmitted parity bit to detect errors. Parity-check coding is simple and effective, but it does not correct errors, only detects them.

RESULTS

- The design's FPGA slices have 48 registers. Registers in digital circuits store and propagate values between clock cycles. The design's FPGA slices have 33 lookup tables (LUTs).
- Programmable LUTs can perform any Boolean function. The design uses 23 LUT-FF pairs. LUT-FF pairs implement complex logic functions using LUTs and registers.
- Number of bonded IOBs 28: FPGA input/output buffers (IOBs) used in design. IOBs connect devices and circuits. The number of clock buffer elements (BUFGs) or BUFG control elements (BUFGCTRLs) used in the design. These distribute and synchronise design clock signals.

Proposed Output



Conclusion

In this study, we have explored the use of data encoding techniques to reduce the energy consumption of Network-on-Chip (NoC) architectures. We evaluated several encoding techniques in terms of energy consumption reduction and performance impact. The results show that these techniques can significantly reduce the energy consumption of NoCs while maintaining acceptable levels of performance. The study provides a valuable insight into the design of energy-efficient NoCs for future computing systems. Overall, the use of data encoding techniques is a promising approach to address the energy consumption challenge of NoCs, and further research in this area can lead to the development of more energy-efficient NoC architectures.

Difference between Existing&Proposedsystem :

System	Power (in W)	Area (used cells)	Time
Existing	0.114	78	3.807ns
Proposed	0.014	71	3.597ns

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