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A Novel Low Power ALU Designed by Using Hybrid STT-MTJ/CMOS Circuit

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ABSTRACT —

Due to its ability to condition and regulate domestic energy usage, Smart Energy Control Systems (SECS) have become more and more prevalent in the context of smart homes. This helps to cut down on energy losses and needless electrical use. As embedded systems have developed in tandem with the Internet of Things (IoT), Smart Outlets (SO), and gadgets that support Users Indoor Identification (UII) environments, they have come to play crucial roles in gathering data from electrical devices and mapping each resident's unique daily consumption. This data is then provided to SECS Systems, which can use it to help maintain energy balance while having little to no effect on the everyday usability of electrical equipment. But the majority of the works that suggest these kinds of support for SECS based on SO and UII have a lot of sensors installed all over the house, misread the data that the inhabitants provide, and have trouble identifying different residents. In order to achieve a rebalanced residential energy consumption 87.3% of the time it was used, the current work proposes an evolution of an SECS architecture called Smart Com, with the implementation of accurate identification of electrical equipment through Near Field Communication (NFC)-based SO (data transfer between the appliance and the SO) and of multiple inhabitants through Wi-Fi handover using smartphones, with the least possible impact on user comfort and building structure.

Keywords— Smart Home, IOT architecture ,Sensors, Home appliance, Wireless Communication

Introduction (MTJ)

The introduction of new business models, such as in the electrical power distribution system, has resulted in substantial modifications to the electric power systems in recent years. End users can participate in the dynamics of Smart Grid (SG) networking thanks to these forms. This contact creates a complicated situation for the services because it brings up several important issues. One such issue is how to integrate software and hardware features. This is because power systems and organisations operate in diverse locations, which is crucial for guaranteeing an appropriate degree of security. Consequently, it is advised that a plan be implemented that takes into account every facet of the electrical sector.

Regulatory Authority (such as in the domains of monitoring, control, and maintenance), as well as meeting the requirements for cost-effectiveness, interoperability, clean sources of renewable energy generation, reliability, management, and controlling. All of these qualities are necessary for the SG domains [1].

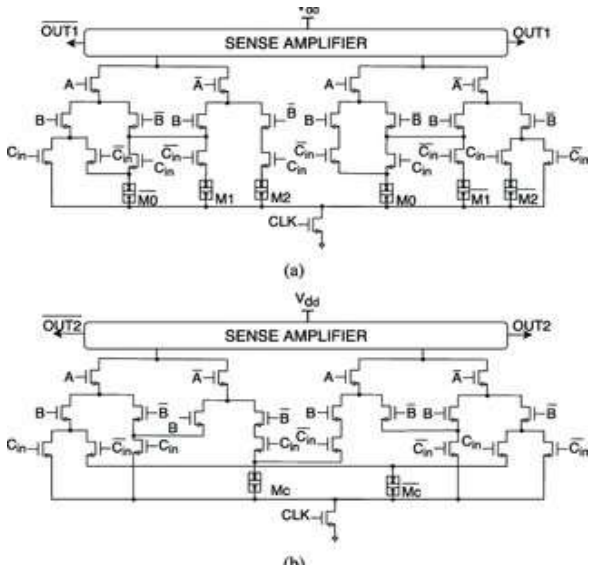
All things considered, an SG is a network that can intelligently and reliably provide security, viability, efficiency, and high-quality service while managing electrical systems and equipment in a variety of industries. Within those fields, there are seven related areas [2]. Generation, transmission, and distribution are handled by the first four—distribution, transmission, end users, and large-scale generation. In order to facilitate complete administration, such as data interchange, between consumers and the Advanced Metering Infrastructure (AMI), these fields need to guarantee two-way communication.

Important technological resources including data security, modularity, adaptability, interoperability, remote control capability, and the potential to use computational decisionmaking methodologies are all included in the scalable HEMS architecture. The plan also aims to include components like SG that are outside the scope of the SH field. By employing an AMI implemented in the cloud, it generates a single integrated interface system with an interoperable layer and provides a web service with the tool.

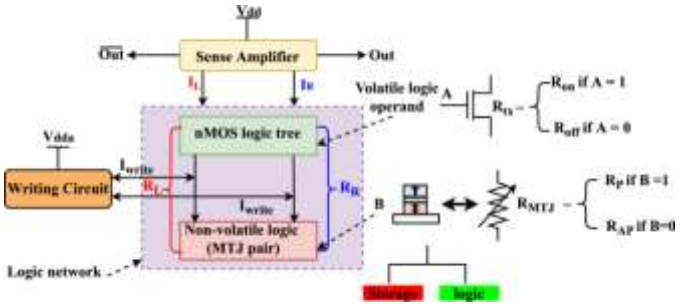
This paper is therefore an evolution of [6], [7], which now permits the tracking and identification of multiple users through the use of smartphones for internal Wi-Fi handover and the extraction of precise data from consumption, electric current, voltage, and identification of electric household appliances through the use of SO technology and NFC identification.

This new design also makes use of the LoRaWAN protocol, which is a dependable, long-range method for controlling and collecting data from home appliances.

This innovative suggestion attempts to aid numerous users to achieve the perfect electrical energy consumption regardless of their location in the house and what appliance they are currently using, implementing a recommender system to preserve electrical energy as well as user's comfort.



alu circuit

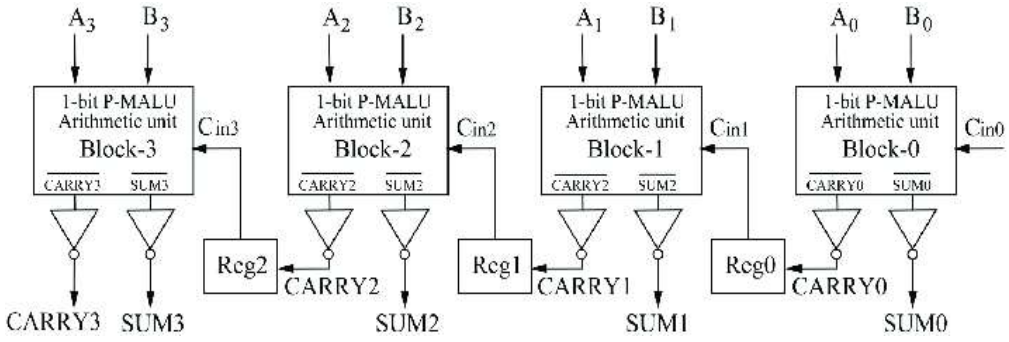


1) Detector/Read Circuitry: This circuit configuration is a current comparator. After pull-down networks (PDNs) have finished processing inputs, sense (a) Redesigned sum sub-circuit structure for M-MALU to generate SUM, SUM in arithmetic addition and XOR, AND, and OR functions in logical mode of operation, along with their complements. (b) The carry sub-circuit for M-MALU has been modified to produce CARRY, CARRY when adding arithmetically. The output of an amplifier is given in its authentic and complementary form.

2) Pull down network: This is an MTJ and MOS logic structure combination. Here, MTJs and MOS logic both contribute to the logical operations.

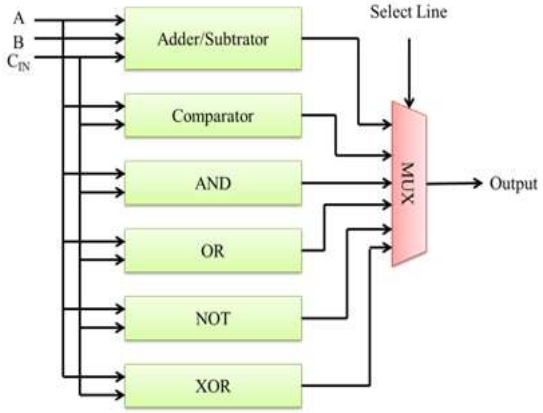
3) The input data is written into the MTJ using the writing block of the LIM architecture.

An amplifier for current comparator pre-charge sense is employed in the M-MALU and P-MALU designs. On the other hand, writing circuits is derived from writing MTJ states.



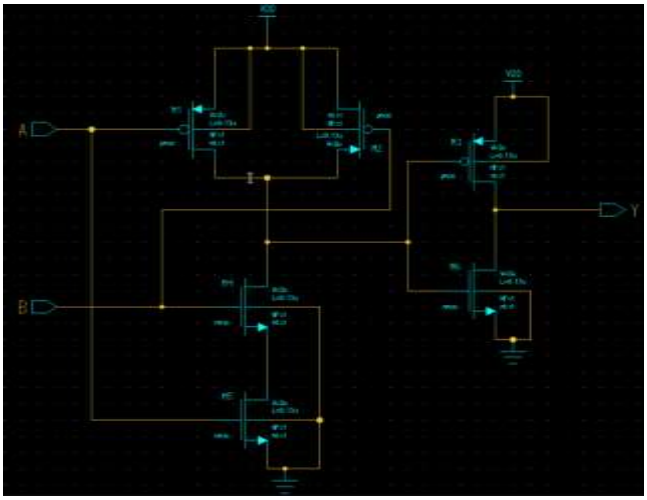
Now we study about the alu using cadence

- Typically, the ALU has direct input and output access to the processor controller, main memory (random access memory or ram in a personal computer) and input/output devices. Inputs and outputs flow along an electronic path that is called a bus.

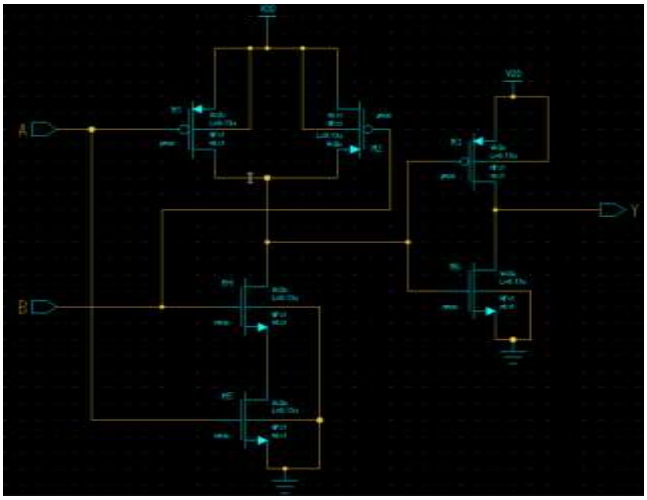


An alu consists of too many combinational and sequential circuits they are

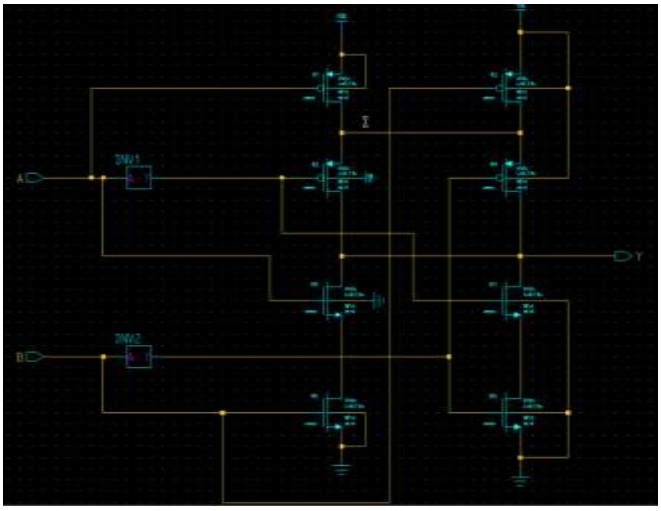
Schematic of AND gate :



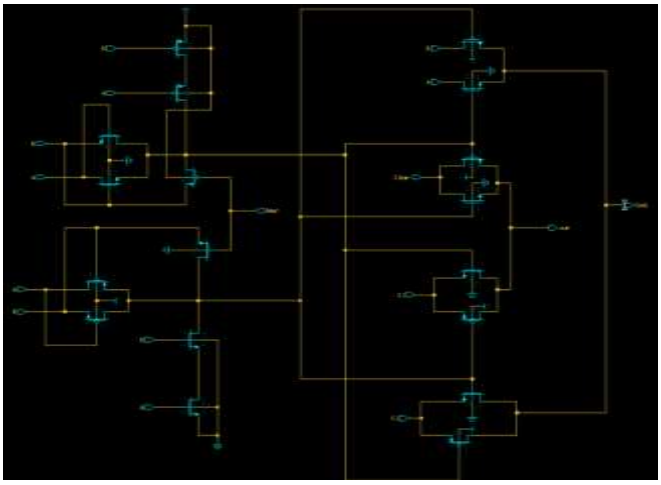
Schematic of OR gate :



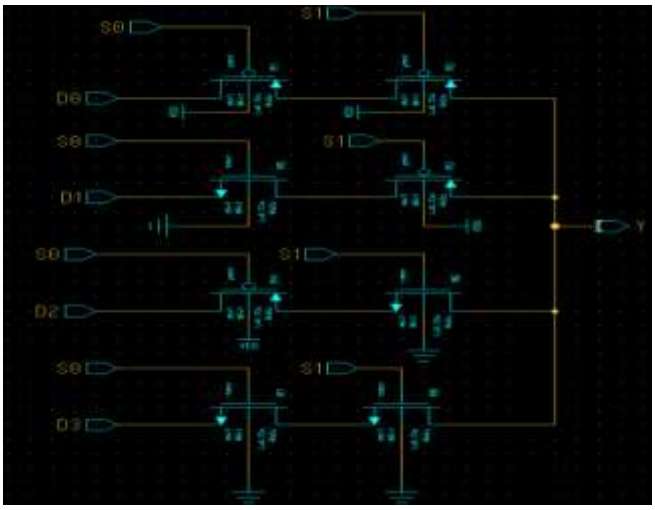
Schematic of XOR gate :



Schematic of Full Adder:



Schematic of MULTIPLEXER Design



FULL ADDER:

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

AND GATE :

The AND gate is a basic digital logic gate that implements logical conjunction (∧) from mathematical logic – AND gate behaves according to the truth table. A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If not all inputs to the AND gate are HIGH, LOW output results.

NAND GATE:

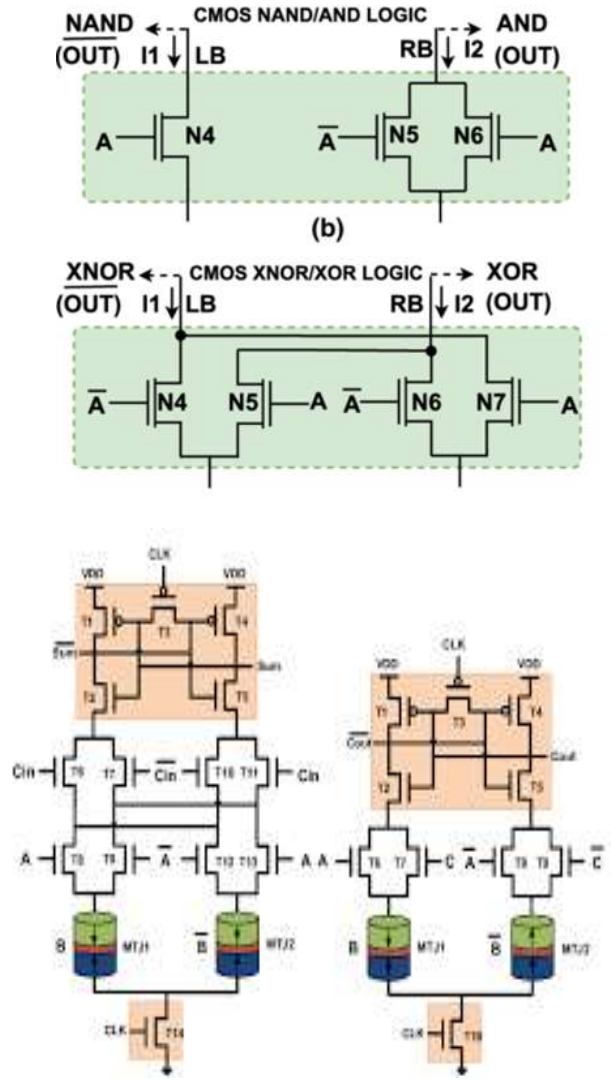
NAND is an abbreviation for “NOT AND.” A two-input NAND gate is a digital combination logic circuit that performs the logical inverse of an AND gate. While an AND gate outputs a logical “1” only if both inputs are logical “1,” a NAND gate outputs a logical “0” for this same combination of inputs.

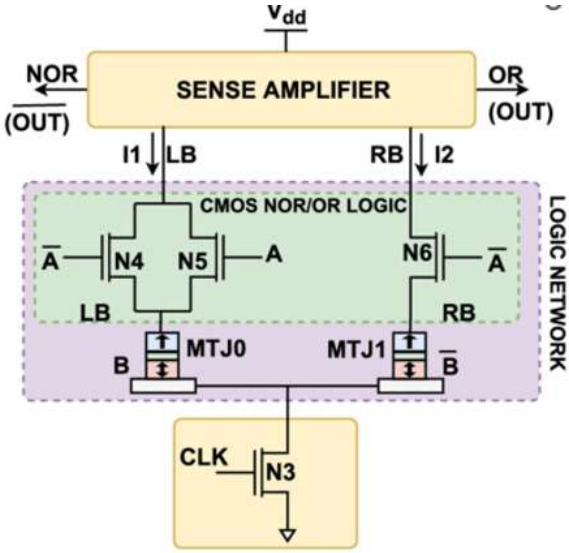
NOR GATE:

A NOR gate is a digital logic gate that gives an output of 0 when any of its inputs are 1, otherwise 1. NOR gates can be made to produce a variety of logic gates, including OR and AND gates. The output of the NOR gate is a logic 0 as long as the input voltage is below the threshold

OR GATE:

The OR gate is a digital logic gate that implements logical disjunction. The OR gate outputs "true" if any of its inputs are "true"; otherwise it outputs "false". The input and output states are normally represented by different voltage levels.

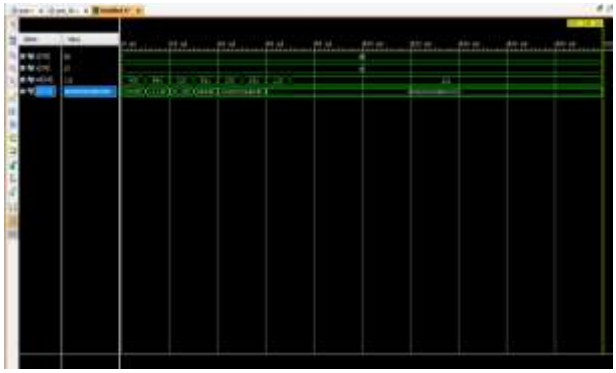




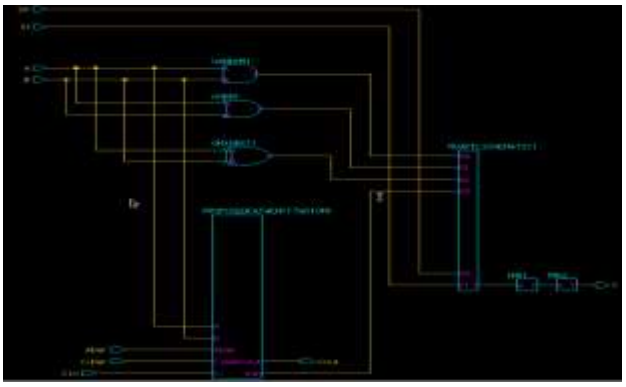
GATE LEVEL MODELING:

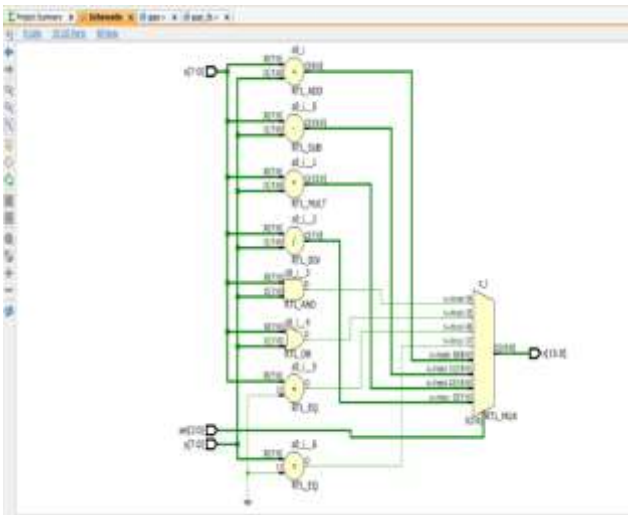
```
module PALU(x,y,sel,z);
input [7:0]x,y;
output reg [15:0]z;
input [2:0]sel;
parameter ADD=3'b000;
parameter SUB=3'b001;
parameter MUL=3'b010;
parameter DIV=3'b011;
parameter AND=3'b100;
parameter OR=3'b101;
parameter NOT1 =3'b110;
parameter NOT2 =3'b111;
always@(*)
case(sel)
ADD: z=x+y;
SUB: z=x-y;
MUL: z=x*y;
DIV: z=x/y;
AND: z=x&&y;
OR: z=x||y;
NOT1: z=!x;
NOT2: z=!y;
endcase
endmodule
```

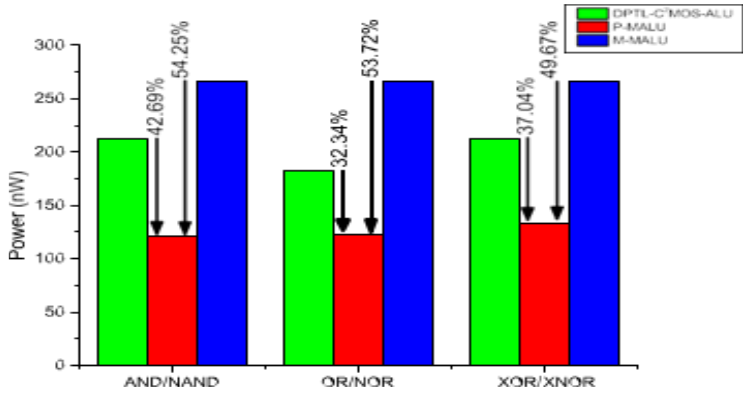
Logic	OPERATION	POWER DISSIPATION	DEVICE COUNT	NO
DPTl	XOR/XNOR/OR/NOR/NAND/AND/OR	212	36	1
MALU	XOR/XNOR/OR/NOR/NAND/AND/OR	265	41	2
P MALU	XOR/XNOR/OR/NOR/NAND/AND/OR	135	21	3



Schematic of SINGLE BIT ALU Design







CONCLUSION:

a novel P-MALU design is proposed and its power dissipation, device count, and delay are found to be better than those of DPTL-C2MOS-ALU and M-MALU designs. Because MTJs are not volatile in the slightest, when the power is turned on, the stored values are immediately usable for logic operations in addition to being stored. Because MTJ-developed hybrid circuits are non-volatile by nature, they don't require "backup" and "restore" functions and require zero static power consumption in standby mode. Compared to volatile CMOS design, hybrid circuits have this important advantage. The findings covered in this paper indicate that the suggested design uses less power and takes up less space on the silicon.Magnetic Tunnel Junctions (MTJs). An ALU is a crucial component of a computer's central processing unit (CPU), responsible for performing arithmetic and logic operations. However, MTJs are known for their use in magnetic random-access memory (MRAM), a type of non-volatile memory.

REFERENCES:

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[4] Jibin Wu , Chenglin Xu, Xiao Han, Daquan Zhou, Malu Zhang , Haizhou Li , Fellow, IEEE, and Kay Chen Tan , Fellow, IEEE