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Design of on Chip Permutations Network using 3D Mesh Network on Chip

[1]Yeleti Srivarshini, [2]Dr B Ramana Kumar

[1]Research Scholar, Department of ECE, International School of Technology and Sciences (Women), Affiliated to JNTUK, NH-16, East Gonagudem, Rajanagaram, Rajamahendravaram, Andhra Pradesh 533294, India.

[2]Associate Professor, Department of ECE, International School of Technology and Sciences (Women), Affiliated to JNTUK, NH-16, Eastgonagudem, Rajanagaram, Rajamahendravaram, Andhra Pradesh 533294, India.

ABSTRACT

The network on chip (NoC) due to their flexibility, scalability and high bandwidth features they are considered as on-chip communication fabrics for future multiprocessor system on chips(MPSOCs). In my abstract the design of a network on chip to support a guaranteed throughput is explained. The clos network topology is used with the three stages of switches of 4ports of inputs and outputs. This network is designed to support a guaranteed traffic permutation in multiprocessor system-on-chip applications. The proposed network employs a pipelined circuit-switching approach combined with a dynamic path-setup scheme enables runtime path arrangement for arbitrary traffic permutations. Network on chip (NoC) is a communication subsystem on a integrated circuit, typically between IP cores in a system on a chip(SoC).

I. Introduction

Multiprocessor systems-on-chips (MPSoCs) have emerged in the past decade as an important class of very large scale integration (VLSI) systems. An MPSoC is a system on- chip a VLSI system that incorporates most or all the components necessary for an application that uses multiple programmable processors as system components. MPSoCs are widely used in networking, communications, signal processing, and multimedia among other applications .A trend of multiprocessor system-on-chip (MPSoC) design being interconnected with on-chip networks is currently emerging for applications of parallel processing, scientific computing, and so on. The empirical law of Moore does not only describe the increasing density of transistors permitted by technological advances. It also imposes new requirements and challenges. Systems complexity increases at the same speed. Now a day's systems could never be designed using the same approaches applied 20years ago. New architectures are and must be continuously conceived. It is clear now that Moore's law for the last two decades has enabled three main revolutions.To overcome the drawback of packet switching and fixed arbitrary scheme for arbiter in switch circuit, a new design is proposed with configurable and programmable Arbiter for runtime traffic permutation. The main drawback previous system is with the Arbitration schemes. To overcome these problems we are using run time programmable arbiter in each switch. The Arbiter is programmed with new Arbitration schemes by overcoming drawbacks of previous schemes. The efficiency is improved. The proposed system re-routes data on erroneous links to a set of spare wires without interrupting the data flow. The main advantage of Circuit Switching is manual establishment of dedicated channel, with a fixed delay for data transaction

II. LITERATURE REVIEW

Technological evolution enables the integration of billions of transistors on a chip. This allows an efficient exploitation of resources and increasingly complex and varied design. The Multiprocessor Systems on Chip (MPSoC) represent a new paradigm emerged from this development. They can include several heterogeneous components like processors (Scalar, Risk) memories, hardware accelerators (DMA, DCT, FFT) and peripheral input/ output. The communication between these various components is provided by an interconnection network called Network on Chip (NoC). Performance evaluation is a key step in any MPSOCs design and especially of the selected communication architecture, allowing for decisions and trade-offs in view of system. The survey presents a perspective on the existing research and practices initiated for the Design Space Exploration (DSE) in Multiprocessor System on Chip (MPSoC) technology Reduction in size as well as adding more functionality within a single chip by incorporating multiple processors remains the key in the development of the modern MPSoC.

This rapid development has been made possible because of the techniques used for scaling down the size of the chip in the field of integrated circuits. MPSoC has been considered as the best candidate for applications such as networking, telecommunication, multimedia, etc. which require high computational demand, high performance, flexibility, high energy efficiency, and low cost design. The designers have the onerous task of building

MPSoCs for such applications because they have huge design options in terms of Processing Elements (PEs), micro-architectural features, interconnects, etc. to be considered with specific constraints.

Geoffrey Blake, Ronald G. Dreslinski, and Trevor Mudge carried out survey on multi core processors. Survey also discusses on architectural classifications, advantages by using multi core systems so that the performance can be increased by increasing number of cores rather than frequency. With the emergence of commercial multi core architectures in an array of application domains, it is important to understand the major design characteristics common among all multi cores. Survey defined five major attributes common among multi core architectures and discussed the tradeoffs for each attribute in the context of actual commercial products. These areas were application domain, power/performance, processing elements, memory, and accelerators/integrated peripherals.

B. Neji , Y. Aydi , R. Ben-atitallah ,S. Meftaly , M. Abid , J-L. Dykeyser carried out survey on multistage interconnect network for MPSoC. It also tells that multistage network is well suited for MPSoC. It also estimates performance in terms of area, latency and power consumption. It also discuss on topology, routing algorithm and technical arbitration, By taking a prototyping on FPGA, compares other type of networks in terms of performance.

III. MULTIPROCESSOR SYSTEM ON CHIP

Multiprocessor systems on chip (MPSoC) are the latest materialization of Very large scale integration (VLSI) technology. A single Integrated Circuit can contain over 100 million transistors and international technology road map for semiconductors predicts that chips with billion transistors are within reach. Harnessing all this raw computing power requires designers to move beyond logic design into computer architecture. The demands placed on these chips by applications require designers to face problems not confronted by traditional computer architecture. Real time deadlines, very low power operation and so on. These opportunities and challenges make MPSoC design an important field of research.

A Soc is an integrated circuit that implements most or all of the functions of a complete electronic system. The most fundamental characteristic of anSoC is complexity A memory chip may have many transistors, but its regular structure makes it a component and not a system. Exactly what components are assembled on the Soc varies with the application. Many SoC's contain analog and mixed-signal circuitry for input/output (I/O). Although some high-performance I/O applications require a separate analog interface chip that serves as a companion to a digital Soc, most of anSoc is digital because that is the only way to build such complex functions reliably. The system may contain memory, instruction-processors (central processing units), specialized logic, buses, and other digital functions. The architecture of the system is generally tailored to the application rather than being a general purpose processors.

IV. MULTISTAGE INTERCONNECTION NETWORK

The Processing Elements (PE's) previously described are mostly interconnected by a Network-on-Chip (NoC). A NoC is composed of Network Interfaces (NI), routing nodes and links. The NI implements the interface between the interconnection environment and the PE domain. It decouples computation from communication functions. Routing Nodes, also called routers, are in charge of routing are arbitrating the data between the source and destination PEs through the links. Several network topologies have been studied.

4.1 An Introduction to Interconnection Networks

Much of the early work on interconnection networks was motivated by the needs of the communications industry, particularly in the context of telephone switching. With the growth of the computer industry, applications for interconnection networks within computing machines began to become apparent.

Among the rest of these was the sorting of sequences of numbers, but as interest in parallel processing grew, a large number of networks were proposed for processor to memory and processor to processor interconnection. With the advent of the fast packet switch, interest in interconnection networks has turned full circle in that many of the networks originally proposed for parallel processing are now being considered for use in fast packet switch designs. Machines began to become evident.

4.2 Control Mechanism

Interconnection networks may also be classified according to the control mechanism employed to connections between input ports and output ports. If the algorithm is centralised and implemented in a central processor then the state of all existing connections and all connection requests may be consulted in order to make the necessary routing decisions. The use of a centralised control mechanism implies circuit switching where the holding time of a connection is much greater than the time required to establish connection. The vast majority of modern telephone switch designs use centralised control. In fast packet switching applications the control mechanism must be distributed across the switch fabric and must be capable of operating without access to information regarding the entire state of the switch.

V. DESIGN APPROACH

Proposed on chip network topology

The design of multistage switching on chip network topology with pipelined circuit switching with dynamic path, the dynamic path-setup scheme enables runtime path arrangement for arbitrary traffic permutations. The circuit-switching approach offers a guarantee of permuted data. The proposed design involves configuration and programming of Arbiter in switch circuit

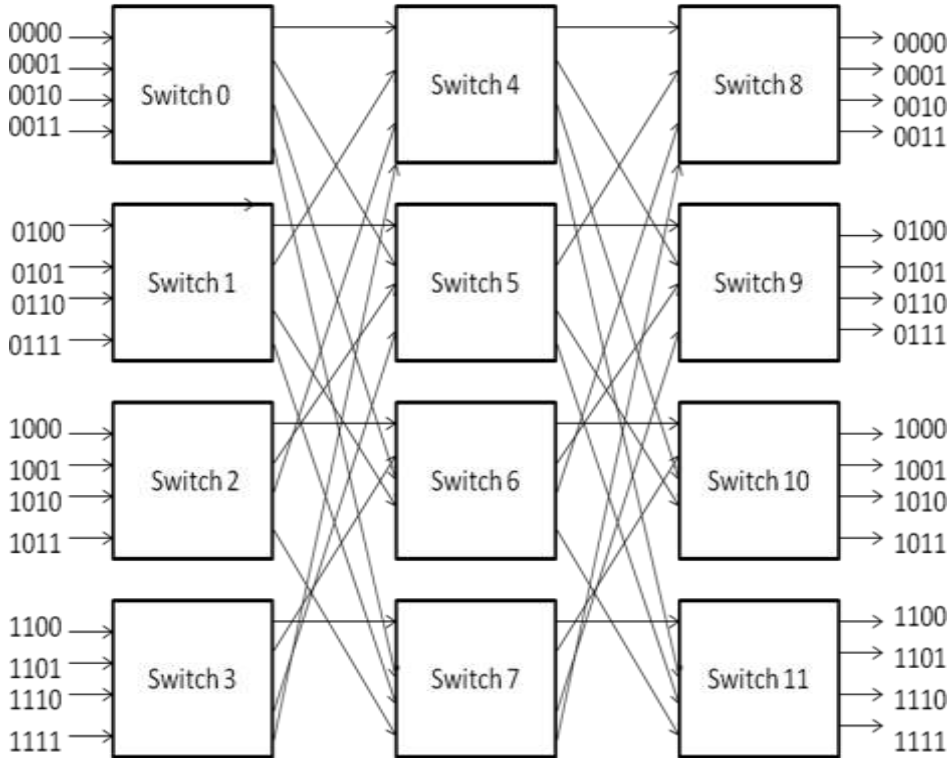


Figure5.1:Proposedon-chipnetworktopologywithportaddressingschem

VI. VERILOG HARDWARE DESCRIPTION LANGUAGE

A Hardware Description Language is a language used to describe a digital system, for example, a computer or a component of a computer. One may describe a digital system at several levels. For example, an HDL might describe the layout of the wires, resistors and transistors on an Integrated Circuit (IC) chip, i.e., the switch level or, it might describe the logical gates and flip flops in a digital system, i.e., the gate level. An even higher level describes the registers and the transfers of vectors of information between registers. This is called the Register Transfer Level (RTL). Verilog supports all of these levels. However, this handout focuses on only the portions of Verilog which support the RTL level.

Verilog is one of the two major Hardware Description Languages (HDL) used by hardware designers in industry and academia. VHDL is the other one. The industry is currently split on which is better. Many feel that Verilog is easier to learn and use than VHDL. As one hardware designer puts it, "I hope the competition uses VHDL." VHDL was made an IEEE Standard in 1987, while Verilog is still in the IEEE standardization process.

Popularity of Verilog HDL

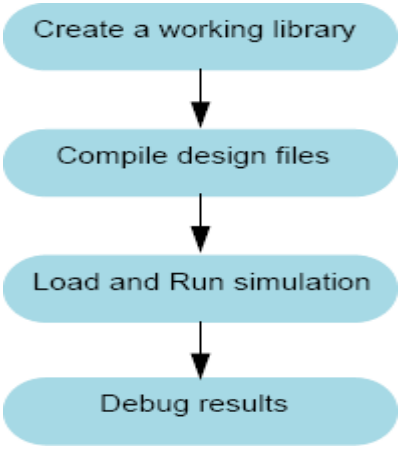
Verilog HDL has evolved as a standard hardware description language. Verilog HDL offers many useful features

- Verilog HDL is a general-purpose hardware description language that is easy to learn and easy to use. It is similar in syntax to the C programming language. Designers with C programming experience will find it easy to learn Verilog HDL.
- Verilog HDL allows different levels of abstraction to be mixed in the same model. Thus, a designer can define a hardware model in terms of switches, gates, RTL, or behavioural code. Also, a designer needs to learn only one language for stimulus and hierarchical design

VII. SIMULATION AND SYNTHESIS TOOLS

7.1 ModelSim

ModelSim is a verification and simulation tool for VHDL, Verilog, System Verilog, and mixed language designs. It is divided into four topics, which you will learn more about in subsequent lessons. • Basic simulation flow. • Project flow. • Multiple library flow. • Debugging tools.



Basic Simulation Flow The figure.7.1 shows the basic steps for simulating a design in ModelSim. Creating the Working Library in ModelSim, all designs are compiled into a library. You typically start a new simulation in ModelSim by creating a working library called "work," which is the default library name used by the compiler as the default destination for compiled design units.

- Compiling Your Design After creating the working library, you compile your design units into it. The ModelSim library format is compatible across all supported platforms. You can simulate your design on any platform without having to recompile your design.
- Loading the Simulator with Your Design and Running the Simulation With the design compiled, you load the simulator with your design by invoking the simulator on a top-level module (Verilog). Assuming the design loads successfully, the simulation time is set to zero, and you enter a run command to begin simulation.
- Debugging Your Results if you don't get the results you expect, you can use ModelSim's robust debugging environment to track down the cause of the problem

VIII SIMULATION RESULTS

8.1: Top module 3stage switching circuit:

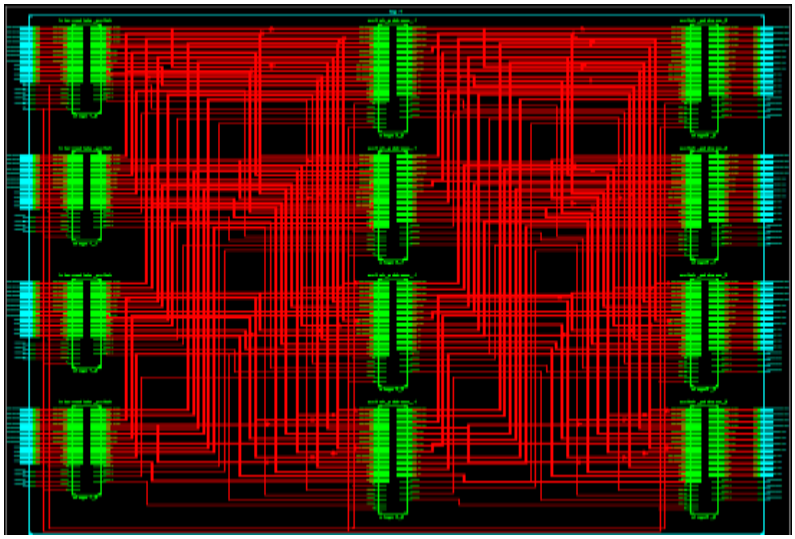


Figure8.1:Top module 3stage switching circuit

8.2: ARBITER

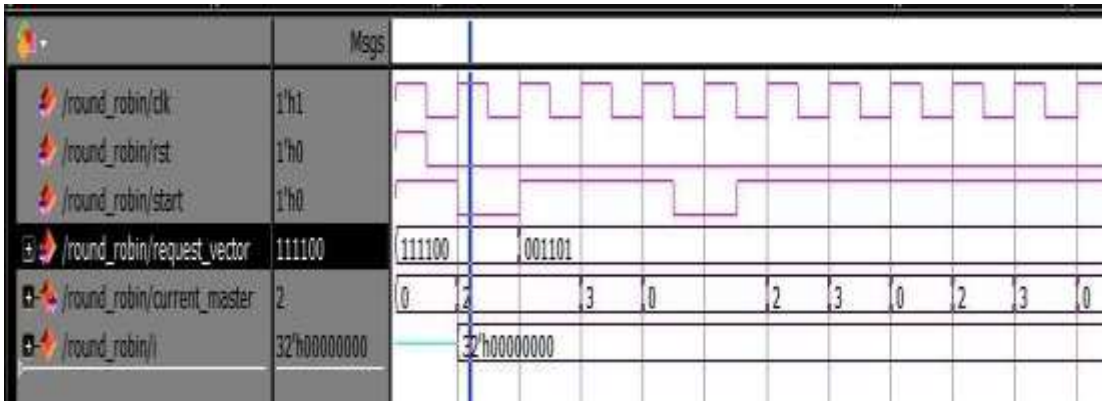


Figure 8.2.1: Simulation results for Round Robin

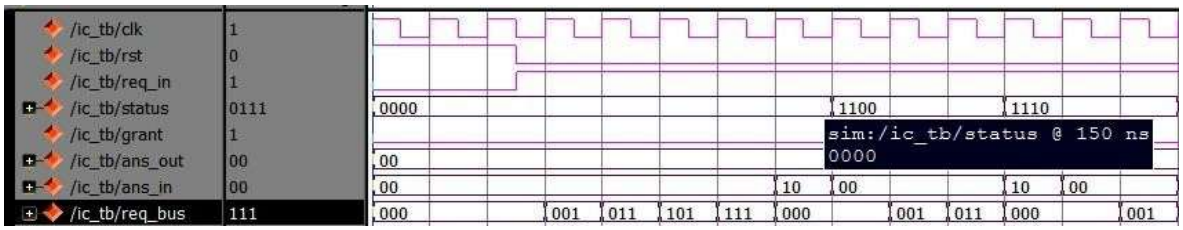


Figure 8.2.2:Simulation results for input circuit

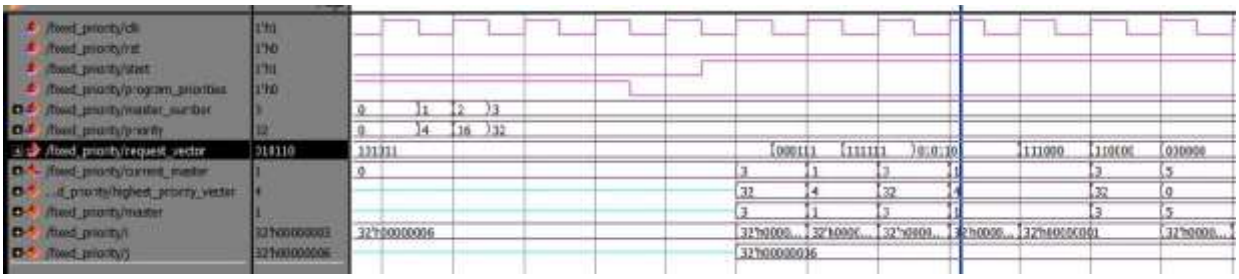


Figure 8.2.3:Simulation results for fixed priority

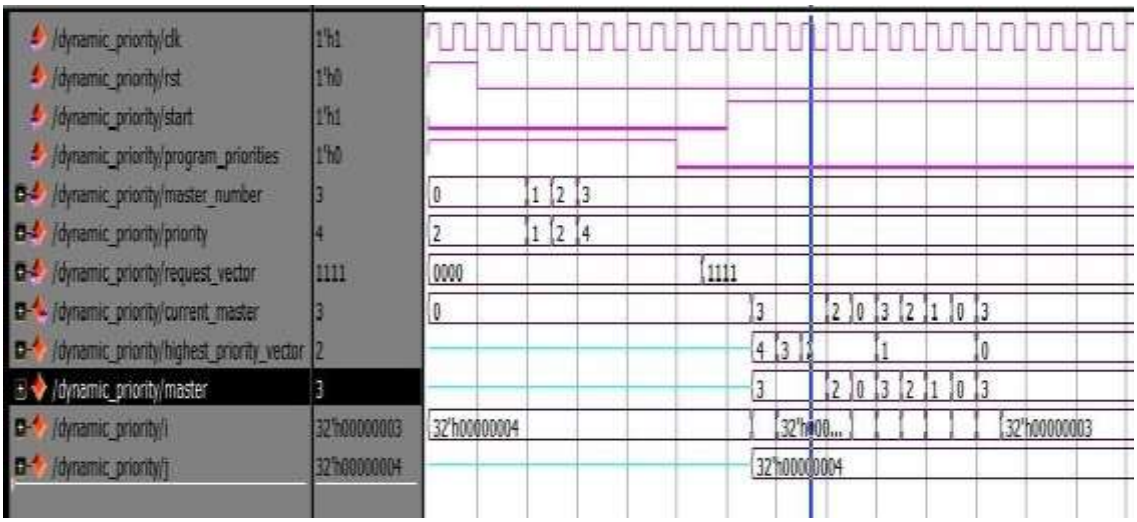


Figure 8.2.4: Simulation results for dynamic priority

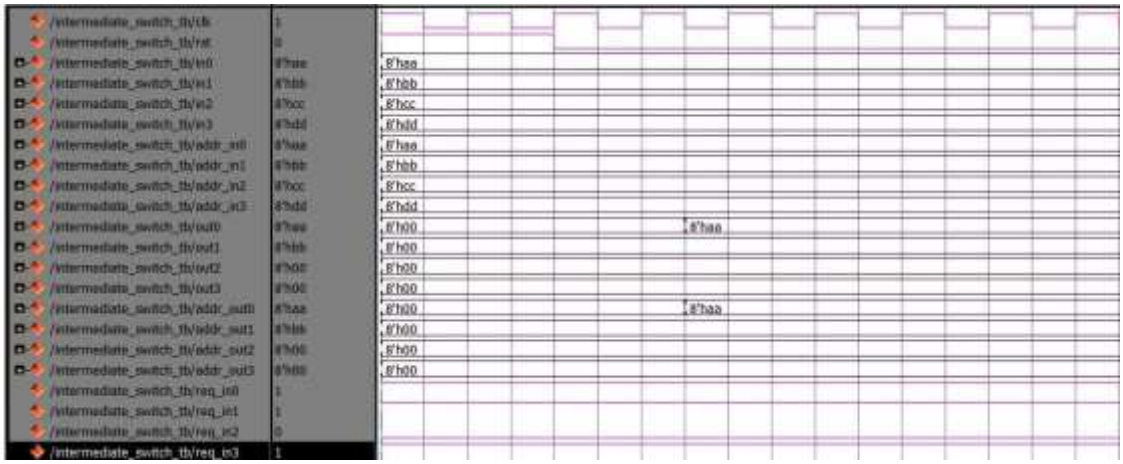


Figure 8.2.5: Simulation results for intermediate switch

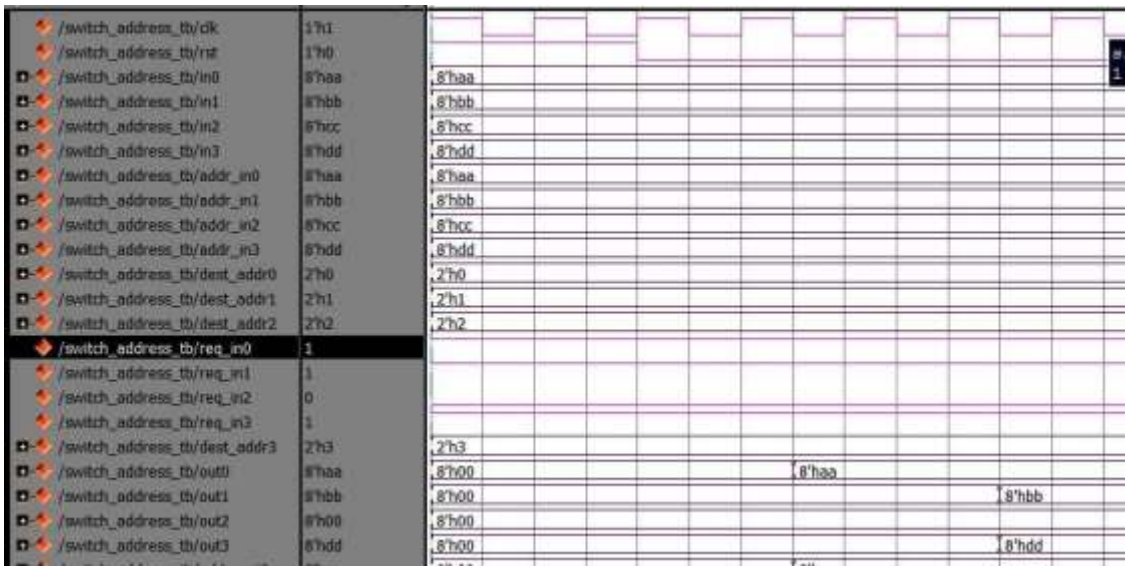


Figure 8.2.6: Simulation results for switch address

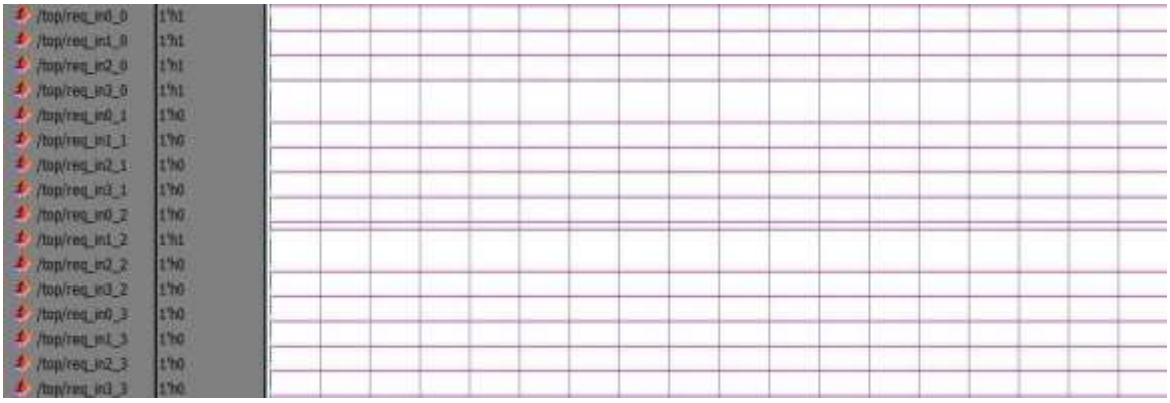


Figure 8.2.7:simulation results for part1 of ocp

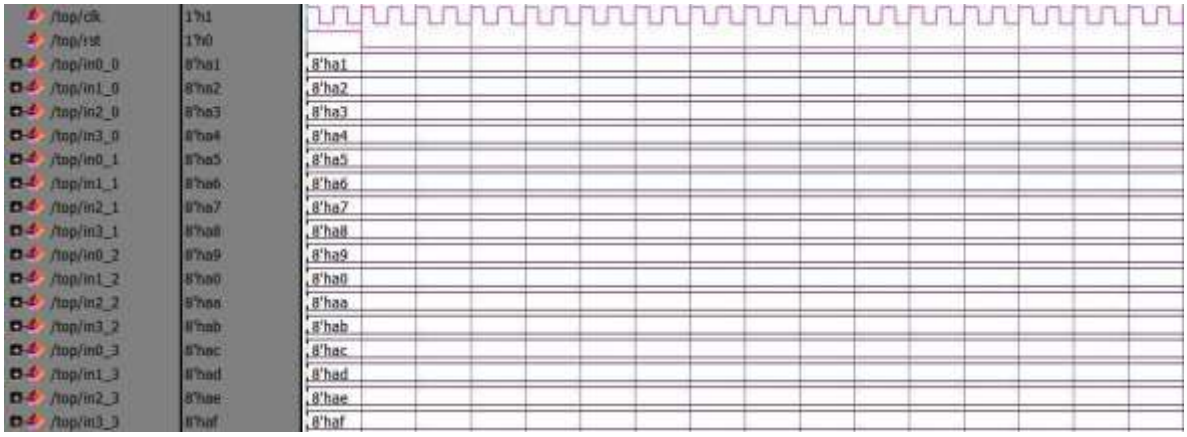


Figure 8.2.8:simulation results for part2 of ocp

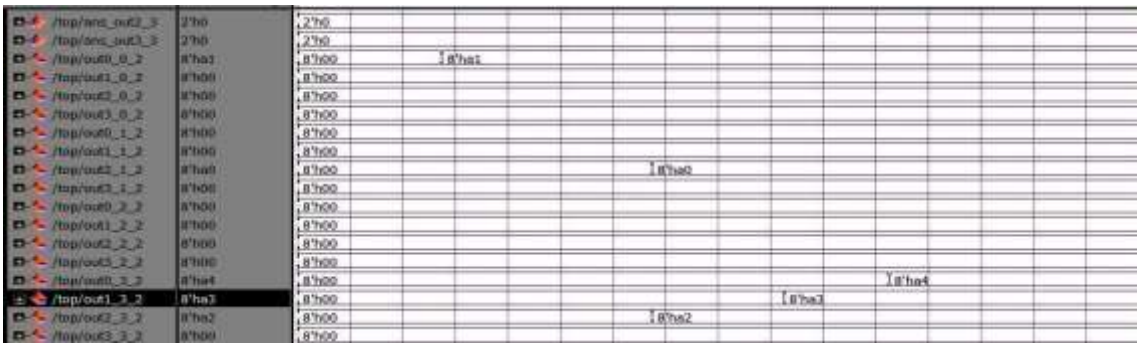


Figure 8.2.9:simulation results for part3 of ocp

IX CONCLUSION

Project designed NOC: onchip network designed supporting traffic permutations in MPSoC applications. By using a circuit-switching approach combined with dynamic path-setup scheme under a Closed network topology, the proposed design offers arbitrary traffic permutation in runtime with compact implementation overhead.

By using Closed Network Topology we can operate network at a range of approx: 100MHz frequency,bandwidth of approx: 30Gbps.

By using Circuit Switching technique we can have a dedicated path delay from source Node to Destination Node Link once established is serviced till all amount transactions is carried out.

EPB: Exhaustive profitable Backtracking is the routing technique used in setting up the link for data communication.

Dynamic path setup plays a major role in probing,forsetting link.

Future scope

Network On Chip link share Self Switching & Cross Coupling Capacitance nets ,due to this nets consume power.

For optimizing the dynamic power consumption we use an Encoding technique called Bus-Invert method.

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