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Low-Power And High-Performance Shift Register Using Pulsed Latch

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ABSTRACT:

The design and implementation of Shift register with pulsed latches was proposed for low power consumption and high performance. Basically, shift registers are built by flip flops but here flip flops are replaced by pulsed latches to reduce the power consumption. The timing problem exhibited by the latches is reduced by taking necessary delays in pulses for latches. This includes a pulse generator for generating pulses with delays. A shift register using pulsed latches is designed through Verilog HDL using Xilinx tool. This design of shift registers with latch, flip flops and pulsed latch will be compared and analysed and finally will be shown that shift register with proposed pulsed latch is low power and high performance.

Keywords: Pulsed latch, pulsed clock, shift register, flip flop

1. INTRODUCTION

- The structure of a shift register is quite easy. An N-bit shift sign in consists of collection connected N data flip-flops.
- The smallest turn in flip-flop is appropriate for the shift register to lessen the place and electricity consumption. lately, pulsed latches have replaced flip-flops in lots of applications, due to the fact a pulsed latch is tons smaller than a flip flop.
- but the pulsed latch can not be utilized in a shift sign in due to the timing problem between pulsed latches.

2. LITERATURE SURVEY

- S. Shibatani and A.H.C.li : Even with these techniques, the dynamic power of clock network can be large since registers are used as state elements in the design. In general, a flip-flop is used as the register or you can say sequential circuits.

- Byung-Do Yang :In this work it has been proposed to use multiple non-overlaps delayed pulsed clock signals as a solution to this problem in pulsed latch technique.

- Seungwhun Paik and Youngsoo Shin: Hence pulsed latch can be approximated as a faster and smaller flip-flop which have advantages of both flip-flop and latches.

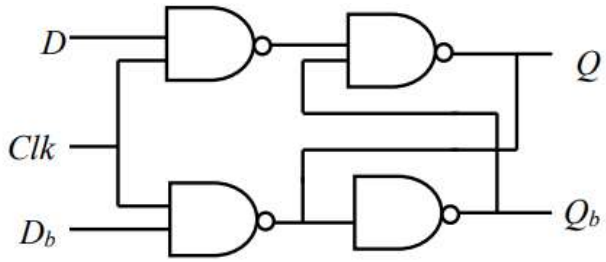
- R. Kumar, K. Bollapalli and S. Khatri:Using flip-flop leads to large power dissipation, counting up to 50 percent of overall power of circuit. Hence, there is requirement of replacing the flip-flop with more efficient circuit which has same functionality while achieving low power, area and robustness to PVT variations.

3. PULSED LATCH TECHNIQUE

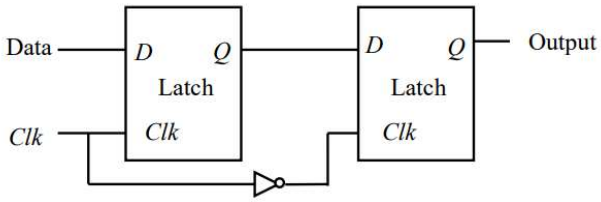
Flip-flop is the most common form of sequencing elements. Flip-flop synchronization with the clock edge is widely used because it is matched with static timing analysis, however, high sequencing leads to overhead in terms of delay, power and area. A latch is quite simple and at the same time consumes much less power than that of the flip-flop. However, it is little difficult to apply static timing analysis with latch design because of the data transparent behavior. A latch is capable of capturing data during the time duration determined by the width of clock waveform. This time duration is known to be very sensitive to its operation.

It is possible to trigger a latch using pulse clock waveform. A latch synchronized by a pulse clock is known as pulsed latch and its behavior is similar to an edge-triggered flip-flop because the rising and falling edges of the pulse clock are almost identical in terms of timing. In a pulsed latch technique, the setup times of pulsed latch are expressed with respect to the rising edge of the pulse clock and hold times are expressed with respect to the falling edge of the pulse clock. Thus timing models of pulsed latch is very similar to that of the edge-triggered flip-flop. The Fig.1. shows a NAND based D latch. A D flip-flop is implemented using two D latch, shown in Fig.2. Pulsed latch technique broadly comprises of a pulse generator and a latch [7]. A pulsed

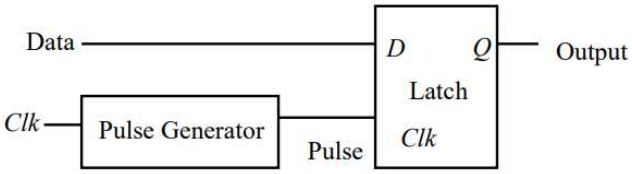
latch having same functionality as D flip-flop is shown in Fig.3. Thus a Pulsed latch circuit consists of one D latch and a basic pulse generator to give similar functionality as D flip-flop. The most attractive feature of using pulse latch technique is that regardless of master slave configuration of latch in flip-flop, pulsed latch eliminates one latch from each cycle and clock's complement. Another important advantage of using pulse latch technique is that the performance of existing designed can be improved without altering the existing design style.
perform other computer vision tasks.



NAND based D Latch

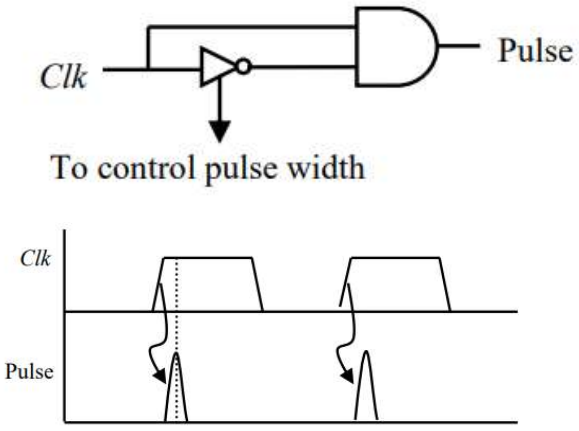


D Flip-flop



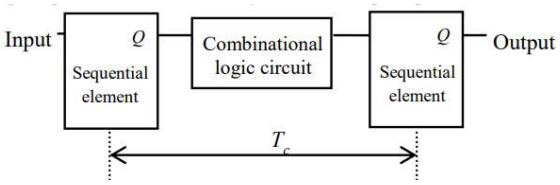
Pulsed latch technique

The timing models of a pulsed latch is similar to that of edge triggered flip-flop. The Fig.3 depicts the pulse generator consisting of AND gate and NOT gate. It generates pulse clock for source clock input. Pulse width of generated pulse clock is adjusted with the help of NOT gate or by inserting delay block in series with the NOT gate. This generated pulse clock is provided to latch. The pulse generator, whose output pulse clock is provided to latch, leads to the functionality same as that of a flip flop.



Pulse Generator and its waveform

In pulsed latch, the setup time is expressed in terms of rising edge of pulse clock, while hold time is expressed in terms of falling edge of pulse clock. This means timing model of pulsed latch is similar to that of flip-flop. Regardless of master slave configuration of latch in flip-flop, pulsed latch eliminates one latch from each cycle and clock's complement. The sequencing overhead is about twice that of latches for flip-flop. Time borrowing capacity as well as use of non-overlapping clocking in flip-flop, complicates its timing analysis. In addition, flip-flop holds data for long period of time, increasing the chances of hold time violations. While in case of pulsed latches, the amount of time borrowing capability is better and very less pulse width offer design to simplify its timing model. Even the sequencing overhead of the pulsed latches is lower than compared to flip-flop. Hence pulsed latch can be approximated as a faster and smaller flip-flop which have advantages of both flip-flop and latches.



Sequencing circuit

Above fig shows sequencing circuit where combinational logic circuit is between sequencing element which can be flip-flop or pulsed latch. In first case, taking flip-flop as sequencing element, then combinational logic propagation delay represented as t_{pd} can be expressed as,

$$t_{pd} \leq Tc-(t_{pcq}+t_{setup}) \quad (1)$$

where, Tc is clock period, t_{pcq} is sequential element clock to output Q propagation delay and t_{setup} is sequential element setup time. $t_{pcq} + t_{setup}$ is figure of merit or sequencing overhead of flip-flop. tpd is circuit dependent. For flip-flop data needs to arrive before the clock edge hence t_{setup} is positive therefore sequencing overhead is much higher. In second case, taking pulsed latch as sequencing element and tpd can be expressed as

$$t_{pd} \leq T_c - \max (t_{pdq}, t_{pcq} + t_{setup}-t_{pw}) \quad (2)$$

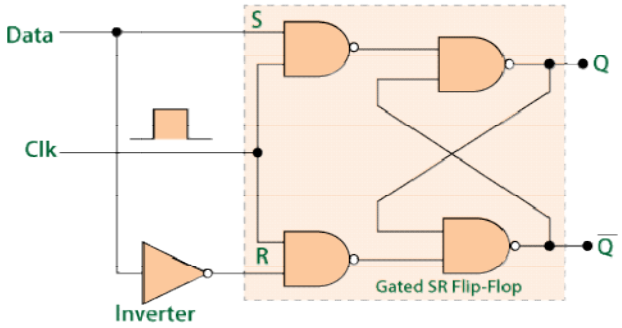
where, t_{pdq} is latch D to output Q propagation delay and t_{pw} is pulse width of clock given to latch of pulsed latch. In this case for pulsed latch, there are two possibilities of transition. First when pulse should be wide enough such that only one latch is critical in one time period so it facilitates the transition or second where pulse should be narrower than setup time such that data must setup before the pulses rises. Therefore for pulsed latch the sequencing overhead is maximum of any one of possibilities overhead. In this case, the data can arrive even after the clock edge hence setup time may be negative. From above discussions and Eq.(2), it is clear that sequencing overhead for pulsed latch is lower than that of flip-flop.

Simulation Result For Pulsed Latch:

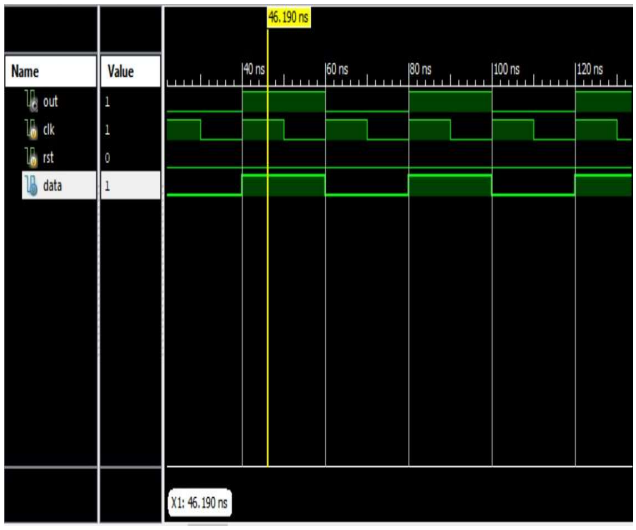
4.Shift Register With D Flip-flops

4.1 D Flip-flop:

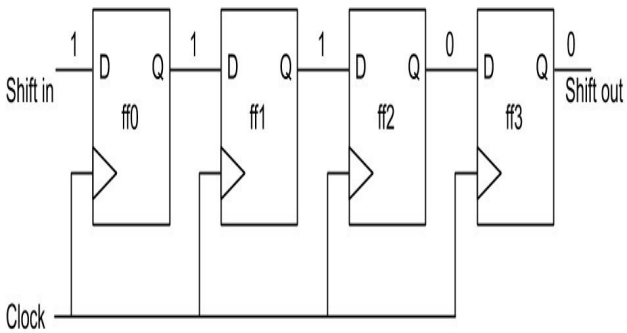
In D flip flop, the single input "D" is referred to as the "Data" input. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset. However, this would be pointless since the output of the flip flop would always change on every pulse applied to this data input.



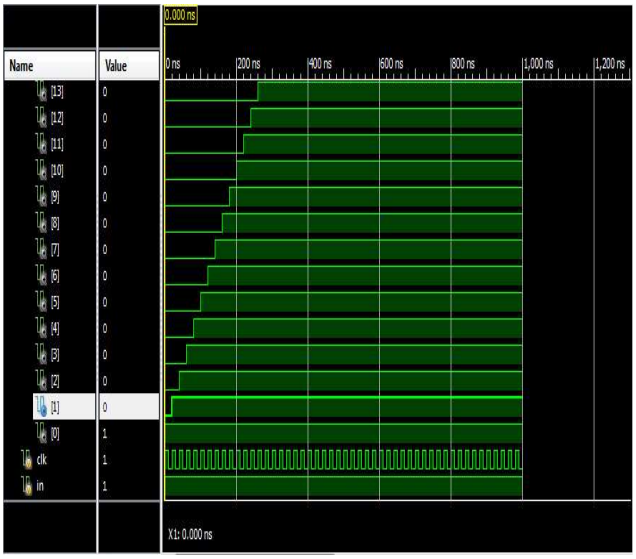
4.2 Simulation Result:



4.3 Block Daigram For Shift Register with Flip-flop :



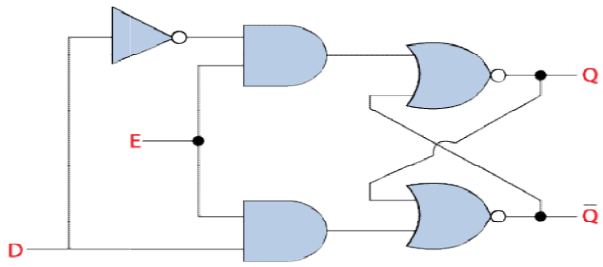
4.4 Simulation Result:



5.Shift Register With D Latch

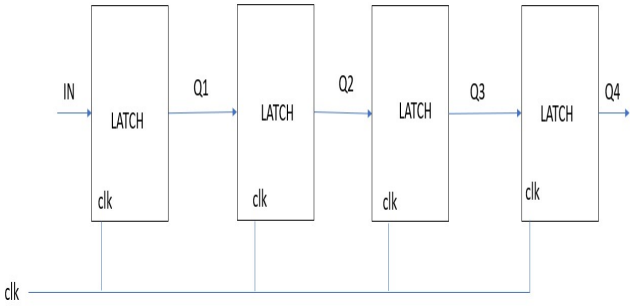
5.1 D Latch:

Latch is an electronic device that can be used to store one bit of information. The D latch is used to capture, or 'latch' the logic level which is present on the Data line when the clock input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch.

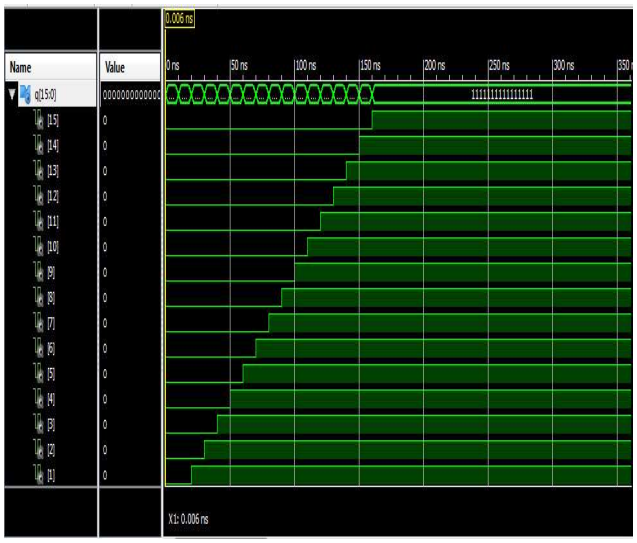


5.2 Simulation Result:

5.3 Block Daigram For Shift Register with Latches :

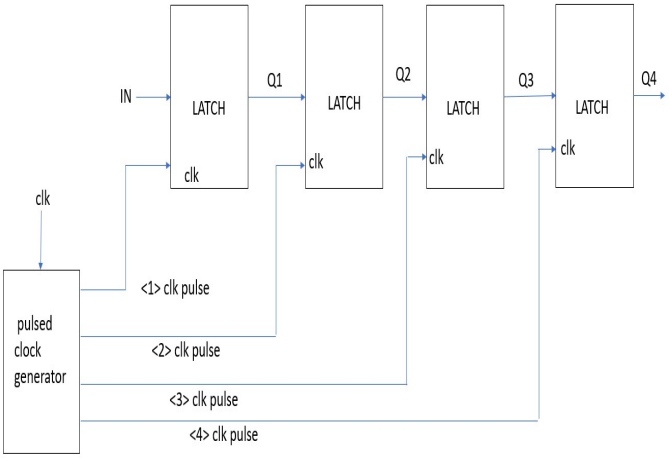


5.4 Simulation Result :

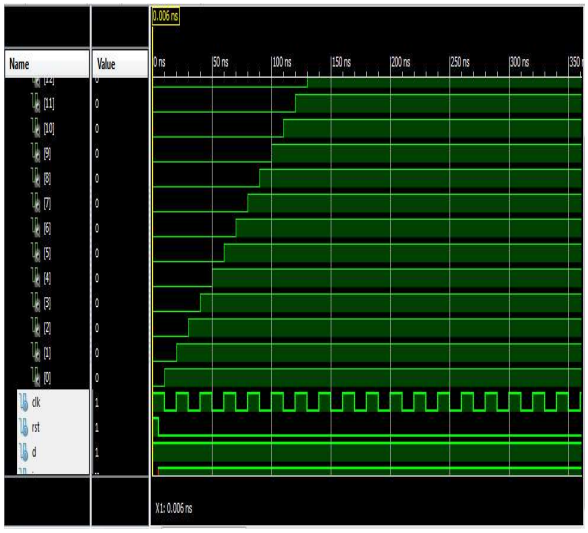


6.Proposed Shift Register With Pulsed Latches

6.1 Block Daigram :



6.2 Simulation Result:



7.Comparision Results

Parameter	D latch	D flip-flop	Pulsed latch
Power(μW)	3.39	204.9	165
Delay(ps)	225.4	56.56	54.39
Power delay product	0.81	10.91	8.59
No. of transistors	16	34	24

The Table summarizes the results obtained for D latch, D flip-flop and pulsed latch. It is observed that pulsed latch technique has better performance.

The power dissipation, power delay product and transistor count is reduced using
Pulsed latch technique.

8.CONCLUSION:

Replacement of flip-flop with pulsed latch can save appreciable amount of power consumption hence now days it is preferred in low power design. This paper proposed different types of shift registers using pulsed latch technique. The number of transistors utilized in pulsed latch is less than that of flip-flop, hence area is significantly reduced. Pulsed latch circuit saves power consumption and power delay product in comparison with flip-flop circuit hence it can be inferred from the results that the circuits using the pulsed latches can be used instead of flip flop for low power, less area and high speed applications. Pulsed latches are faster than flip-flops and offer some time borrowing capability at the expense of greater hold times. They have fewer clocked transistors and hence lower power consumption. The advantages of pulsed latch over flip-flop are saving clock period, power consumption, delay and area. The trading towards applications using pulsed latches from conventional flip-flop circuits in heavy pipelining, mobile devices or in low power ASIC circuits is immense achievement in field of VLSI designing.

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10. BIOGRAPHIES

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