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ARCHITECTURAL DESIGN OF BIST USING LFSR ALGORITHM IN VLSI TECHNOLOGY

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ABSTRACT

This abstract gives a study on design and analysis of a '**Architectural Design Of BIST Using LFSR In VLSI Technology**'. The increasing growth of sub-micron technology has resulted in the difficulty of VLSI testing. Test and design for testability are recognized today as critical to a successful design. **Built-in-Self Test (BIST)** is becoming an alternative solution to the rising costs of external electrical testing and increasing complexity of devices Small increase in the cost of system reduces large testing cost. BIST is a design technique that allows a circuit to test itself **Test-pattern generator (TPG)** using **Linear Feedback Shift Resister (LFSR)** is proposed which is more suitable-for BIST architecture. The construction of the BIST is done with the LFSR decoder circuits, which makes a path in testing the circuit by providing random and complete input sequences to the built architecture. The decoding logic is also employed to make it perfect for fault tolerant architecture. The pavement made of the BIST with LFSR is said to be the efficient technique in finding the faults in the working of the circuitry so this is termed as the fault tolerant architecture the construction of the proposed architecture is done in Xilinx proceeding with Verilog HDL language.

Keywords*: Built-in-Self Test (BIST), Test-pattern generator (TPG), Linear Feedback Shift Resister (LFSR), Verilog HDL*

1. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The power dissipation during test mode is 200% more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges. This report addresses the problem of testing digital logic circuits. System-On-Chip (SOC). Today a combination of external Automated Test Equipment (ATE) and internal BIST (Built-In-Self-Test) techniques are used to ensure the highest possible fault coverage of the device at the lowest possible costs. IC testing using exclusively external ATE's can require SOC architects to allocate a fairly large number of pins of the device to invoke the test procedure and run vectors into and through the various blocks of the device such as memory, user defined logic, dedicated functional macros, etc. Combination of external ATE's and internal BIST however can result in, utilizing far fewer external pins on the IC but at the cost of embedding test logic inside the device. To test large circuit, circuits are partitioned to save the test time but this parallel testing results in excessive energy and power dissipation. Due to the lack of at speed equipment availability, delay is introduced in the circuit during testing. This cause power dissipation. In the successive functional input vectors applied toa given circuits in normal mode have a significant correlation, while the correlation between consecutive test patterns can be very low. This can cause large switching activity in the circuit during test than that during its normal operation. Power dissipation in CMOS circuits is proportional to switching activity, this excessive witching activity during test may be responsible for cost, reliability, performance verification, autonomy and technology related problems. The destructive nature of testing requires that the developer discard preconceived notions of the correctness of his/her developed software.

2. LITERATURE SURVEY

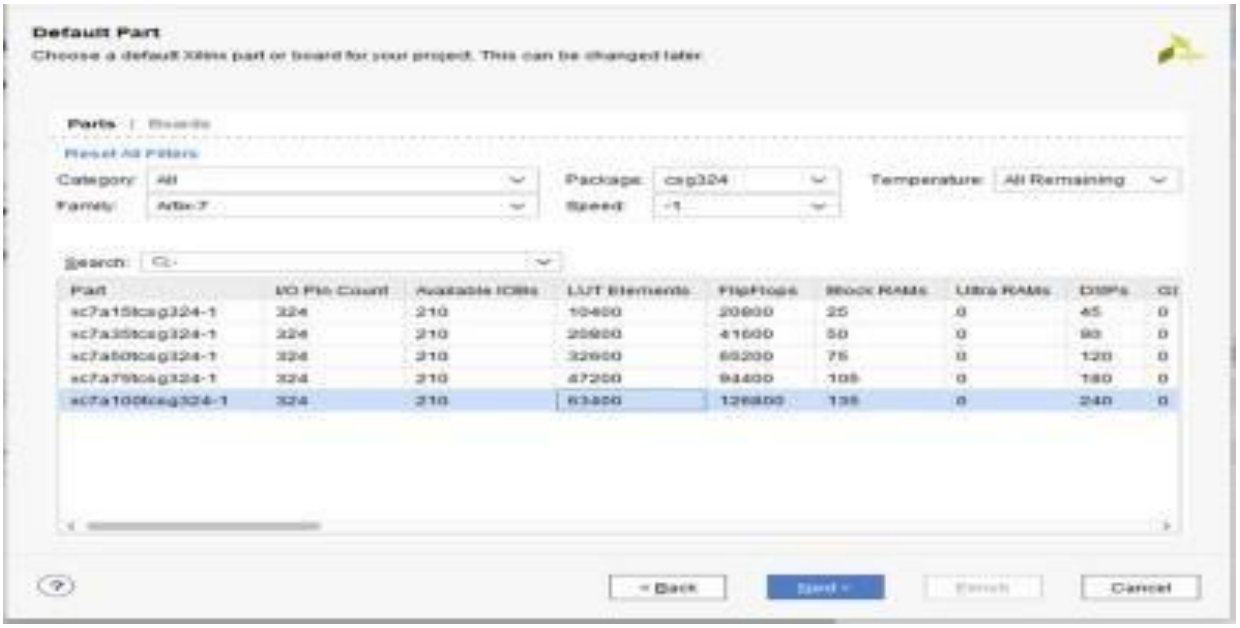
Krishnendu chakrabarty and Shivakumar Swaminathan (Duke University, Durham), have presented built-in self-testing of high-performance circuits using twisted-ring counters. They presented enhanced built-in self-test (BIST) architecture for high-performance circuits. This approach is especially suitable for embedding pre-computed test sets for core-based systems since it does not require a structural model of the circuit, either for fault simulation or for test generation. It utilizes a twisted-ring counter (TRC) for test-per-clock BIST and is appropriate for high-performance designs because it does not add any mapping logic to critical functional paths. Test patterns are generated on-chip by carefully reseeding the TRC. They showed that a small number of seeds are adequate for generating test sequences that embed complete test sets for the ISCAS benchmark circuits.

Mehrdad Nourani, Mohammad Tehrani poor presented their research work on Low-Transition Test Pattern Generation for BIST-Based Applications. In their work; a low-transition test pattern generator, called the low transition linear feedback shift register (LT-LFSR), is proposed to reduce the average and peak power of a circuit during test by reducing the transitions among patterns. Transitions are reduced in two dimensions:

1) Between consecutive patterns (fed to a combinational only circuit) and

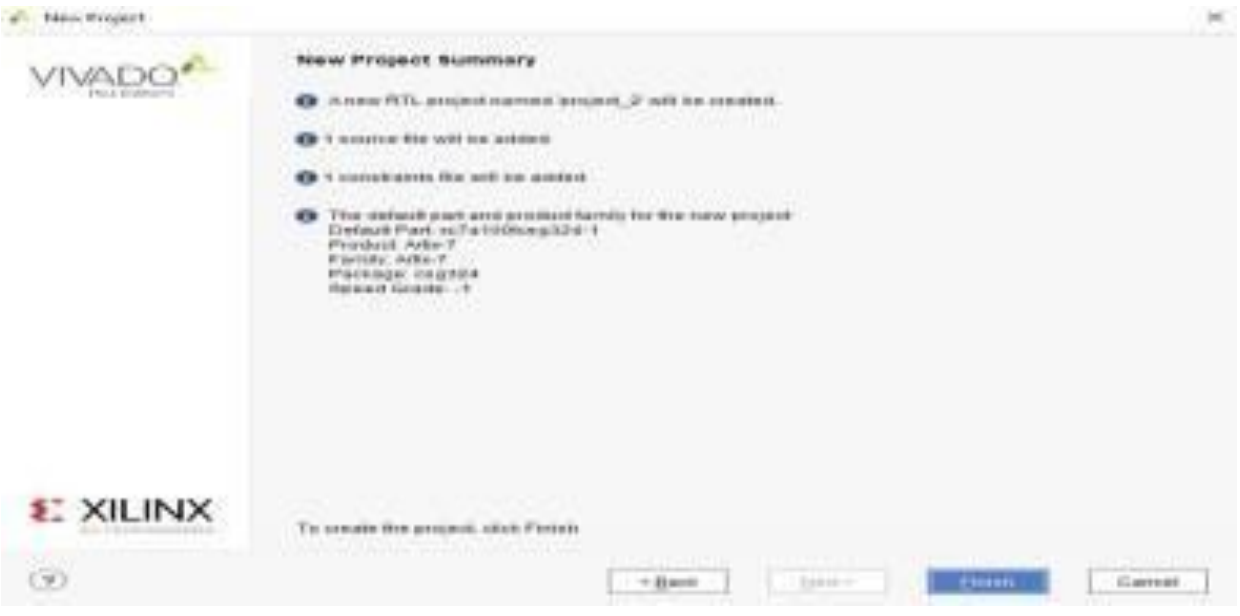
2) Between consecutive bits (sent to a scan chain in a sequential circuit). LT-LFSR is independent of circuit under test and flexible to be used in both BIST and scan-based BIST architectures. Their proposed architecture increases the correlation among the patterns generated by LT-LFSR with negligible impact on test length. The experimental results for the ISCAS'85 and '89 benchmarks confirm up to 77 percent and 49 percent reduction in average and peak power, respectively.

3. METHODOLOGY



Xilinx solutions enable smarter, connected, and differentiated systems, integrating the highest levels of software-based intelligence with hardware optimization and any-to-any connectivity. Xilinx serves the aerospace and defense industry with commercial, industrial, military, and space grade products.

- Double click on VIVADO 2018.1 software.
- Click on create project in Quick start menu and create new project.
- Quick start >> Create project next >> RTL project >>Add sources (Create file >> select file type as VHDL >> File name) >> ok and next >> Add constraints (create file >> select file type as XDL >> File name) >> ok and next) >> below window will be open.
- Click On Next:



Create inputs and outputs in define module according to the project >> Then in Sources window >> source file (file name. vhd), click on that and add the logic in .vhd file window >> Project manager >> simulation (run behavioral simulation).

- In the objects window >> give input values >> Right click on input force constant >> force value.
- Click on run for ten microseconds or Shift+F2 and observe the output waveforms.
- RTL analysis >> open elaborated design >> click on ok. Then schematic output will be displayed

  Click on Run SYNTHESIS in Project Manager window >> Launch Run window >> Change No of jobs as "4">> Click on OK >> If NO ERRORS Synthesis Completed Window will be opened.

  >> Project Manager >> Run IMPLEMENTATION >> Click on OK then IMPLEMENTATION Completed Window will be opened

  Click on Cancel >> Click on LAYOUT in File Menu then I/O Planning.

All ports window will be open in the downside Select Scalar Ports Assign Outputs & Inputs as per kit port number.

Connect the KIT and switch on the power supply >> Click on SAVE in File Menu >> Save constraints tab will be open then click on Ok. >> Project Manager >> Run IMPLEMENTATION >>Click on OK >> IMPLEMENTATION Completed Window will be opened. >> Project Manager >> Click on Generate Bit stream >> Click On OK >> Launch Runs tab will be opened Click on OK >> Bit Stream generation completed tab will be opened >> Open hardware Manger >> Click on OK >> hardware Manger tab will open then click on Open Target >> Auto Connect >> Click on Program device >> Program device will Opened >>Click On Program.

Verify the Program by using switches and LEDs on the KIT.

4. MODELING AND ANALYSIS

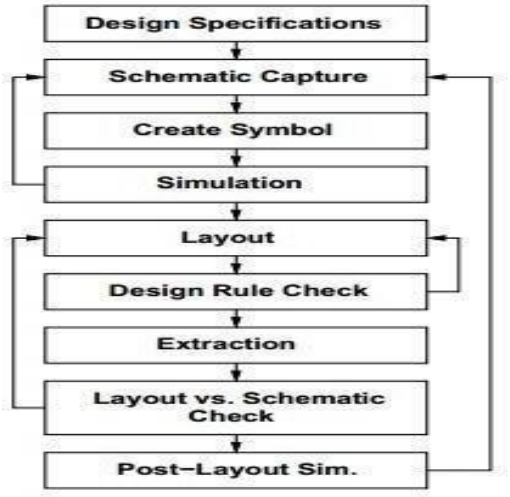


Fig 4.1: VLSI Design Flow

The VLSI IC circuits design flow is shown in the figure below. The various levels of design are numbered and the blocks show processes in the design flow. Specifications comes first, they describe abstractly, the functionality, interface, and the architecture of the digital IC circuit to be designed.

5. RESULTS

The following figure show the schematic diagram of BIST using LFSR

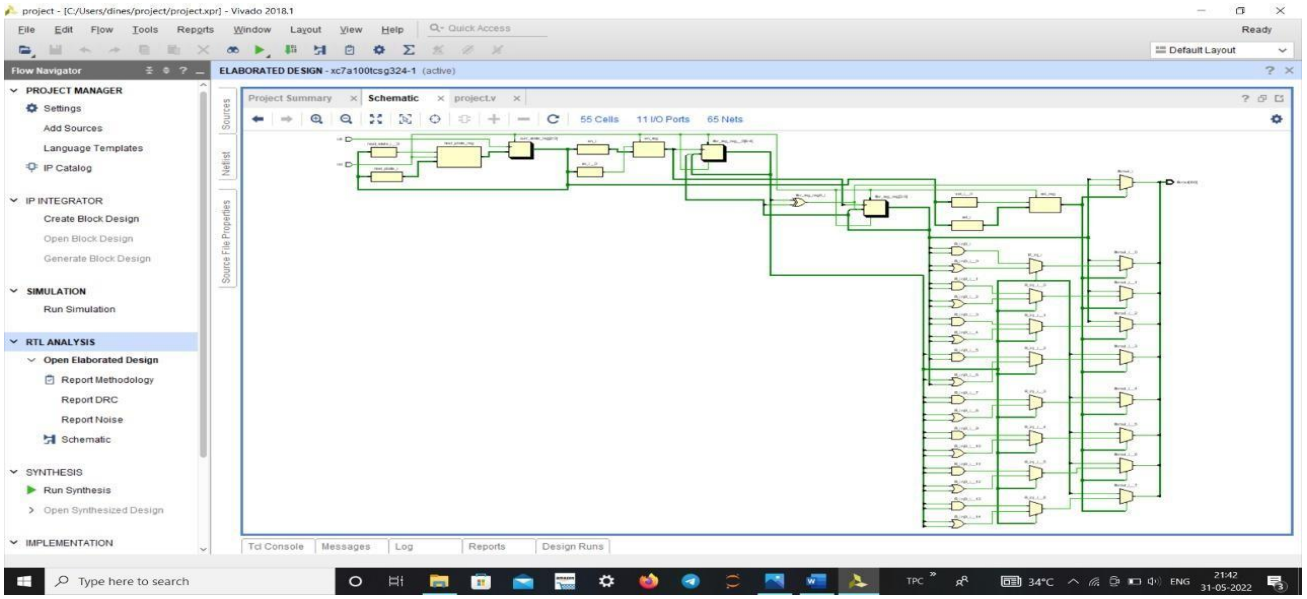


Fig 5.1: Schematic Diagram of BIST Using LFSR

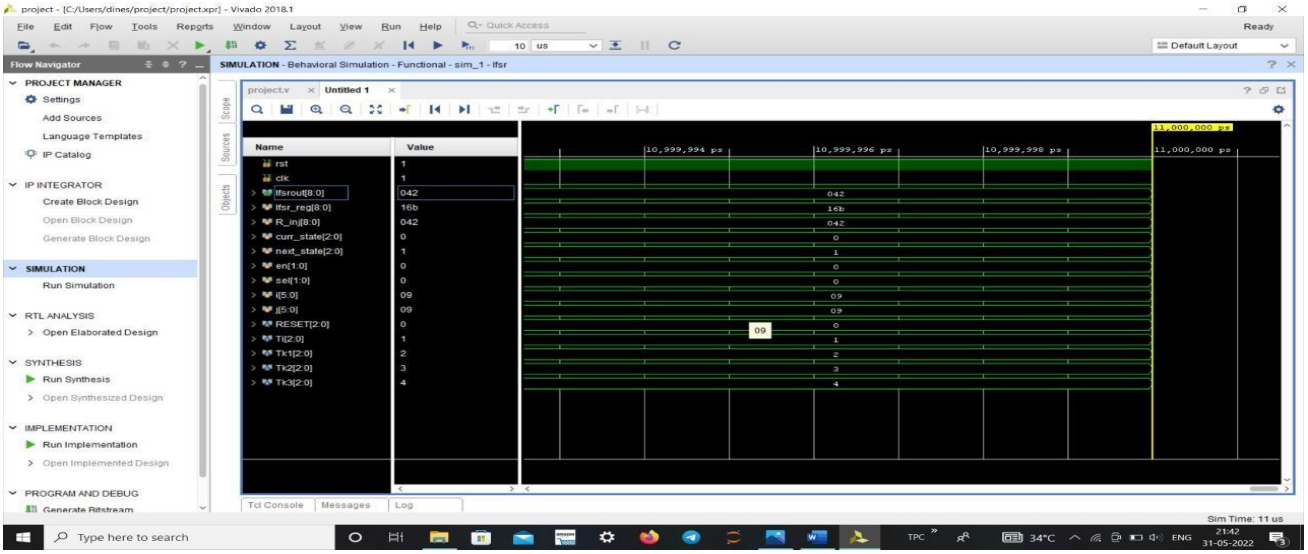


Fig 5.2: Input & output Results

6. CONCLUSION

Built-in self-tests are the heart of any modern reliability tests. Their applications are ranging from cryptography and bit-error-rate measurements, to wireless communication systems employing spread spectrum or code division multiple access techniques. However, the strict time constraints limit the complexity of the tests as such, that multiple compression methods via a parallel LFSR (Linear Feedback Shift Register) signature analyzer exist. This chapter's purpose is to raise awareness of the issue to propose a common framework for the identification of pattern resistant logic as well as a means to ensure a more stable and safe fault tolerance using a ROM (Read Only Memory) memory as a look-up table. The alternative proposed method for implementing BIST (Built In Self-Test) avoids the use of advanced compression algorithms and needs very little hardware overhead so having small cost and die size. All this research is contained in the presented paper in the Conference on Computers from Rhodes 2009. Another point of view is about the possibility to increase the encoding efficiency of LFSR Reseeding-Based Test Compression. The same method for High Test Data Compression is frequently used also for BIST functioning. The method of reseeding it is possible to be developed for Built-in Test for Circuits using Multiple – Polynomial LFSR.

7. ACKNOWLEDGEMENTS

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