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Design and Simulation of Low Power Circuit using Feed through Logic

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ABSTRACT:

Nonstop technology scaling and increased frequency of operation of VLSI circuits leads to increase in power density which raises thermal operation problem. Thus design of low power VLSI circuit fashion is a grueling task without immolating its performance. Herein, we design of a low power dynamic circuit using a new CMOS domino sense family called feedthrough (FTL) sense. Dynamic sense circuits are more significant because of its faster speed and lower transistor demand as compared to stationary CMOS sense circuits.The proposed circuit for low power feedthrough logic (LP-FTL) improves dynamic power consumption as compared to the being FTL and to further enhance its speed, we propose another circuit high speed feedthrough logic (HS-FTL). This logic family improves speed at the cost of dynamic power consumption and area. Proposed modified FTL circuit families give better PDP as compared to the FTL.Simulation results of both the proposed circuit using 0.18 µm, 1.8 V CMOS process technology indicate that the LP-FTL structure reduces the dynamic power approximately by 35% and the HS-FTL structure achieves a speed up to 1.3 for 10-stage of inverters and 8-bit ripple carry adder in comparison to existing FTL logic.Continuous scaling of technology towards the nanometer range significantly increases leakage current level and the effect of noise. This research can be further extended for performance optimization in terms of power, speed, area and noise immunity.

1.Introduction:

The invention of transistor brought about a giant technology leap in microelectronics. With the advent of transistor and the arrival of IC's, power dissipation is a lesser concern. Greater emphasis is placed on performance and size[1]. To continue to improve the performance of circuits and to integrate more functions into chip, feature size reduces significantly. As a result, the magnitude of power per unit area (power density) has kept growing and the problem of heat removal and cooling getting worse. In the last few years we have seen that the emerging battery powered portable applications like pocket calculator, hearing aids, implantable pacemakers should consume less power for longer life[2, 3]. Consequently, ever since then power reduction has become one of the most critical factors in the evolution of technology. Even with the scaling of supply voltages power dissipation has not reduced significantly because more number of functionality is embedded in a single chip[4, 5]. An alternative to solve this problem could mean accepting either the large cost for cooling subsystem[6-8]. Ineffective cooling degrades reliability. As a result, today it is widely accepted that power efficiency is another important design criterion along with area and performance[9]. So the power consumption should be minimized at each abstraction level and at each phase of the design process[10, 11].A power circuit is defined as any circuit used to carry electricity that operates a load. This may seem like a simplistic definition but it is important to distinguish power circuits from control circuits since they serve different purposes[12].
Low power design is a collection of techniques and methodologies aimed at reducing the overall dynamic and static power consumption of an integrated circuit (IC)[13].The goal of low power design is to reduce the individual components of power as much as possible, thereby reducing the overall power consumption. The power equation contains components for dynamic and static power. Dynamic power is comprised of switching and short-circuit power; whereas static power is comprised of leakage, or current that flows through the transistor when there is no activity. The value of each power component is related to any of the following factors such as activity, frequency, transition time, capacitive load, voltage, leakage current, peak current etc. e.g. the higher the voltage, the higher the power consumed by each component, resulting in higher overall power[14, 15]. Conversely, the lower the voltage, the lower the overall power. To achieve the best performance with the lowest power consumption, trade-offs for each of these different factors are tried and tested via various low power techniques and methodologies. Further, the companies are continuing to push the boundaries on new features and functionality, all packed into portable, handheld, and battery powered devices. For such products, improving the battery life by minimizing power consumption is a huge differentiator and extremely important to their end users' applications. Improving the time, it takes for a device to go from OFF/SLEEP state to ON/ACTIVE state is just as important, as the end user wants to have a seamless experience along with longer battery life.For "plug-in" products, power consumption is also important because it can affect the overall cost of systems by requiring heat sinks and elaborate cooling systems, increasing electricity costs, etc. For example, in server farms, where massively parallel systems are used, a reduction in power for a single chip can result in significant power savings because it is used throughout the system[16]. The power and cost savings by upgrading these systems with newer and more power efficient ICs can be significant.There are many low power design techniques available, some of which are

very simple to use while others are more involved and complex such as

(a) Clock Gating

This technique is typically performed during logic synthesis where enable flops are optimized into a clock gating structure, thereby saving mux area and reducing the overall switching activity of the clock net. With respect to the power equation, the goal is to reduce capacitive load (via area reduction) and activity factors which reduces the switching power component of dynamic power. This is a very simple and readily available technique to reduce power and area. However, it does rely on the logic synthesis tool to perform this optimization. Fortunately, this technique is well-known and well supported in most tools and flows.

(b) Multi Voltage:

This is a technique where functions of a chip are partitioned via performance characteristics – perhaps one block is high performance, while the rest of the chip is lower performance as shown in Figure 3. To achieve the goals for the high-performance block, a higher voltage is typically required; while to save power on the lower performance blocks, a lower voltage can be used. This is in lieu of designing the entire block at the higher voltage, which is simpler but more power intensive. In the power equation, voltage is reduced which decreases every static and dynamic power component. With multi voltage designs, there is the complication of designing in separate voltage islands where voltage crossings between islands may require "Level Shifter" (LS) cells with the need to implement and analyze the blocks at their different voltage characteristics.

(c) Power Gating

This is a technique where functions on an IC are also partitioned, much like multi voltage, but this time the power supplies for the power domains are connected to power switches. Power gating effectively shuts off the power completely for a block. In the power equation, this zero out the voltage and shuts off power, resulting in both static and dynamic savings for the time that the block is turned off. Power gating typically offers the most aggressive power savings, and thus it's an ideal goal to shut off as many domains as possible, as often as possible, while maintaining functionality. In order to achieve this power savings with power gating, power switches must be implemented in the design, which requires Isolation gates that clamp the boundaries of the power domain to known values when off. The power states of the design and what combination of ON/OFF states for given voltages must be considered. Lastly, a power management unit (PMU) that controls the power switch and isolation enable signals must be implemented. It is essential that the order of these signals are correct during power down and power up, such that the values during shutdown are clamped to the right values at the right time.

1. **Design of LP-FTL:**

The performance analysis of the LP-FTL structure is carried out by designing various cascaded combinational and sequential logic circuits. We have designed a long chain of inverter (10-stage), 8-bit RCA and a LFSR by using LP-FTL structure. We have used 0.18- um CMOS process technology model library from UMC, using the parameter for typical process corner at 25 0C. Power supply VDD is constant for all simulations and is equal to 1.8V. Circuits are simulated in HSPICE simulator.

1.1 Longchainofinverter

A long chain of inverter (10-stage) is designed by LP-FTL structure is shown in Figure 1. Figure 2 show the plot of output voltage from the 1st stage of inverter to the 10th stage of inverter at 10 fF capacitive loads for existing FTL and LP-FTL. From this figure the reduction in VOL of LP-FTL as compared to FTL causes improvement in average power consumption. The layout and av_extracted view is shown in Figure 3 to 7.

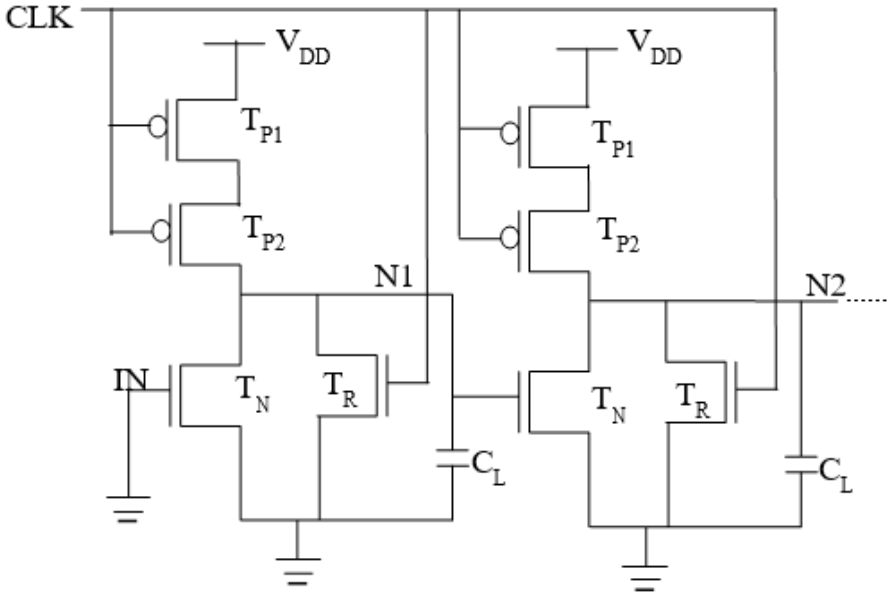
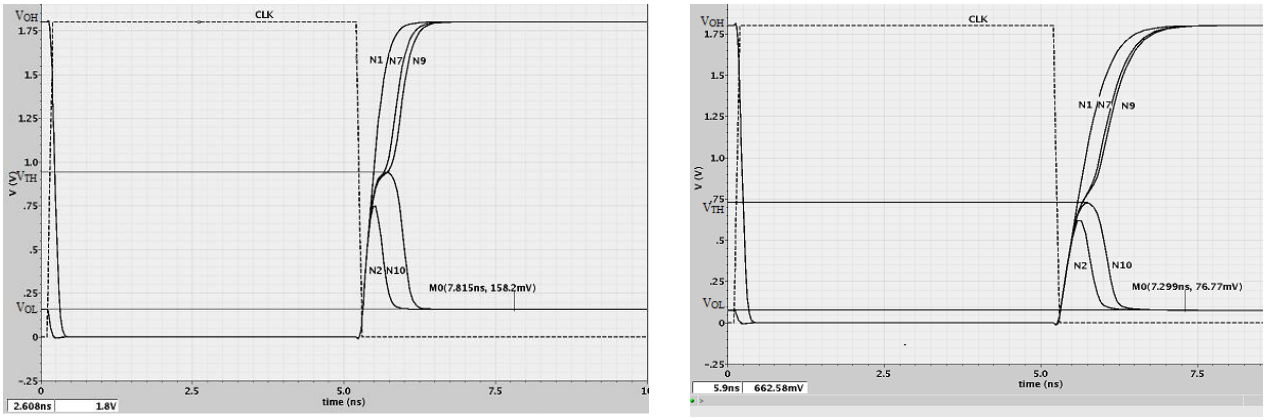


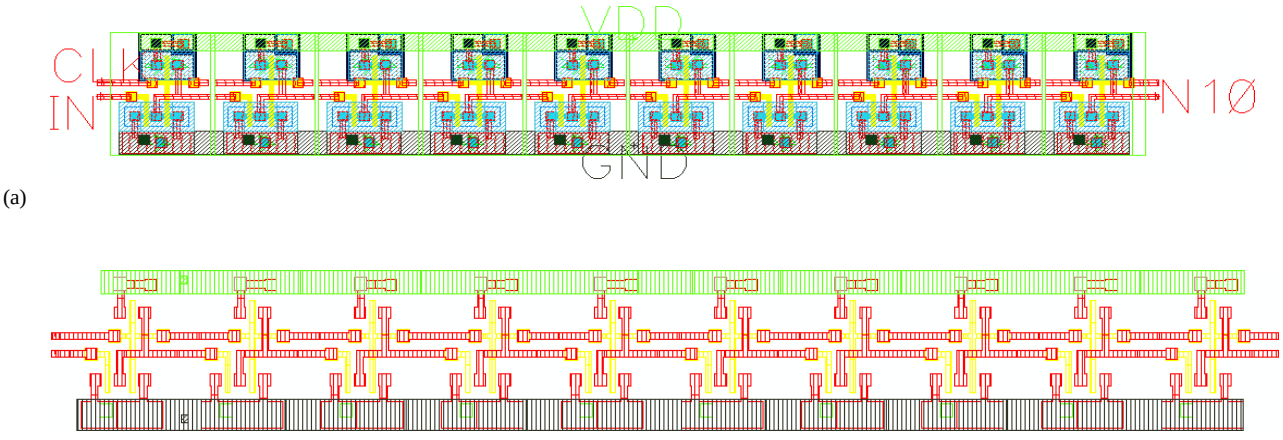
Figure 1. LongChainofLP-FTLinverter



(a) (b)

Figure2. Plotoftheoutputvoltagesfrom1st stage(N1)to10thstage(N10)ofinverters.

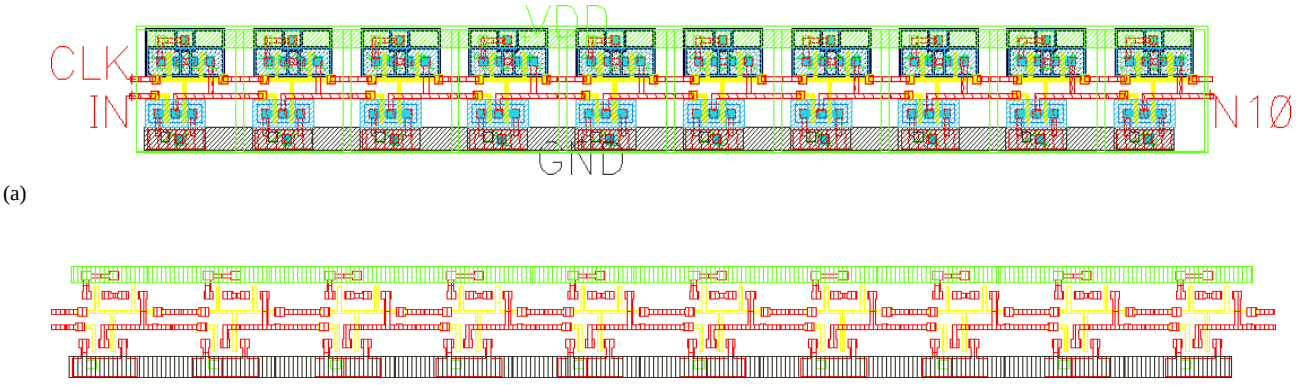
(a) ForFTL(b)ForLP-FTL



(a)

(b)

Figure3 (a)LayoutofFTLinverter(10-stage)(b)av_extracted view



(a)

(b)

Figure4(a)LayoutofLP-FTLinverter(10-stage) (b)av_extracted view

Table 1 shows the average power (Pavg), average values of propagation delays (tp), and power delay product (PDP) comparison of LP-FTL and the

existing FTL in [15] for 10 fF capacitive loads at 100 MHz. The LP-FTL structure provides reduction in power consumption due to reduction in VOL. The power consumption by LP-FTL structure is 42.8% less than that of existing FTL and it provides an area overhead of 24.4%.

Table 1. Post Layout Simulation results comparison between FTL, LP-FTL in termsofpower,delayandarea(10-inverterchain)

LogicFamily	P_{avg}(µW)	t_p(ns)	Area(µm²)	PDP (µW*ns)
FTL[15]	271	800	221	216
LP-FTL	155	950	275	147

2.2. 8-bitRippleCarry Adder

The basic sum and carry cell of a full adder designed by LP-FTL structure is shown in Figure 2.7 The sum and carry expression of full adder is given by

SUM' = ABCIN +COUT' (A+B+CIN) (2.1)

COUT'= AB+CIN (A+B) (2.2)

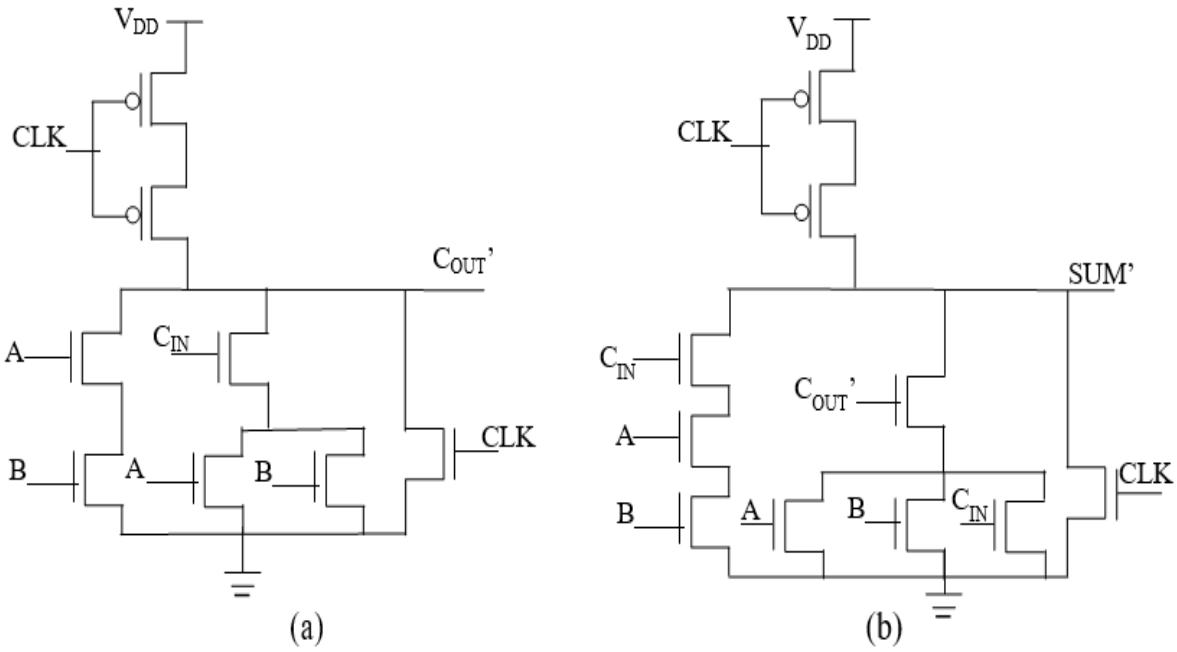


Figure 5. Ripple Carry Adder for LP-FTL structure (a) carry cell (b) sum cell

An 8-bit RCA is designed by cascading such eight full adder cell. To maintain the correct polarity between the RCA cells the A and B inputs of even adder cells and the sum output of odd adder cells are inverted as in [6]. All the 8-bit ripple carry adders i.e. Domino, FTL and LP-FTL adders are simulated in 0.18-um CMOS process technology model library from UMC, using the parameter for typical process corner at 250C. Power supply VDD is constant for all simulations and is equal to 1.8V.

Table 2. Comparison between LP-FTL, FTL and Domino structures in terms of power, propagation delay and area for 8-bit RCA

Logicfamily	t_p(ns)	P_{avg}(µW)	Area(µm²)	$t_p$ratio	PDP (µW*ns)
Domino	2.51	146	1320	1	366.46
FTL[15]	0.620	732	1340	4.04	453.84
LP-FTL	0.681	422	1628	3.68	287.382

Table 2 shows the comparison between Domino, FTL and proposed LP-FTL adder in terms of average power consumption (Pavg), propagation time delays (tp), layout area, PDP for 10 fF capacitive loads. From the table both FTL and LP-FTL structure improves the speed by a factor of 4.04 and 3.68 w.r.t. domino adder. The LP-FTL structure improves the power consumption by 42.34% w.r.t. FTL adder, but speed is reduced by a factor of 1.09 and area overhead of 21.49%. The effect of load capacitance (CL) on propagation delay (tp) is shown in Figure 6. From this figure the LP-FTL adder is faster as compared to the domino adder

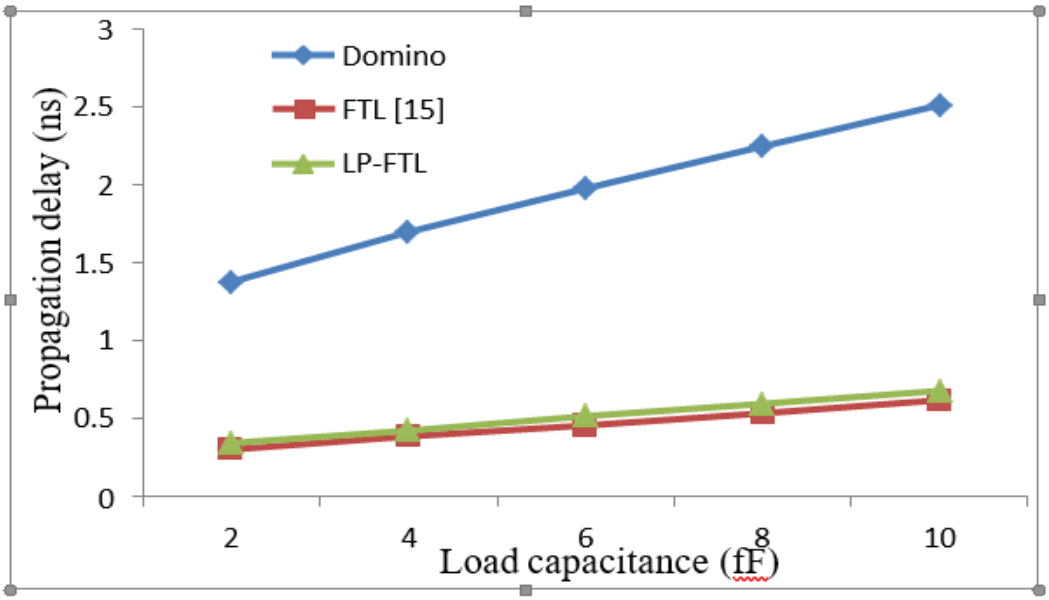


Figure6.Effectofloadcapacitanceonpropagationdelay

2.3. LFSR:

In order to explain the usefulness of proposed LP-FTL in pipelined circuit, we designed a LFSR circuit as shown in Figure 7 The LP-FTL flip-flop shown in Figure 8 is constructed from two cascaded LP-FTL latch controlled by the CLK and CLK'. The structure of LP-FTL latch is shown in Figure 9. The XNOR-gate is also designed by using proposed LP-FTL structure controlled by CLK.

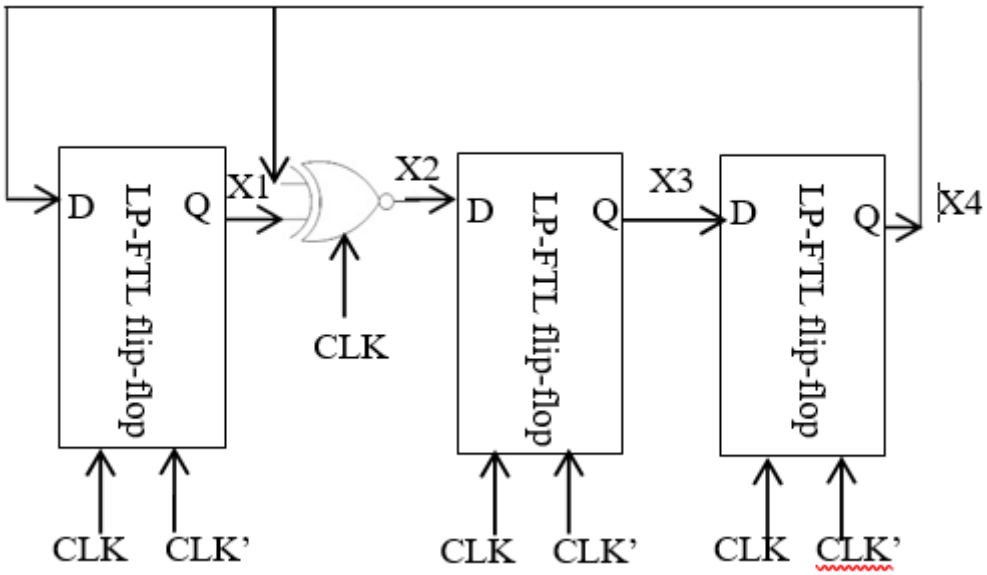


Figure 7 LFSR using LP-FTL flip-flop

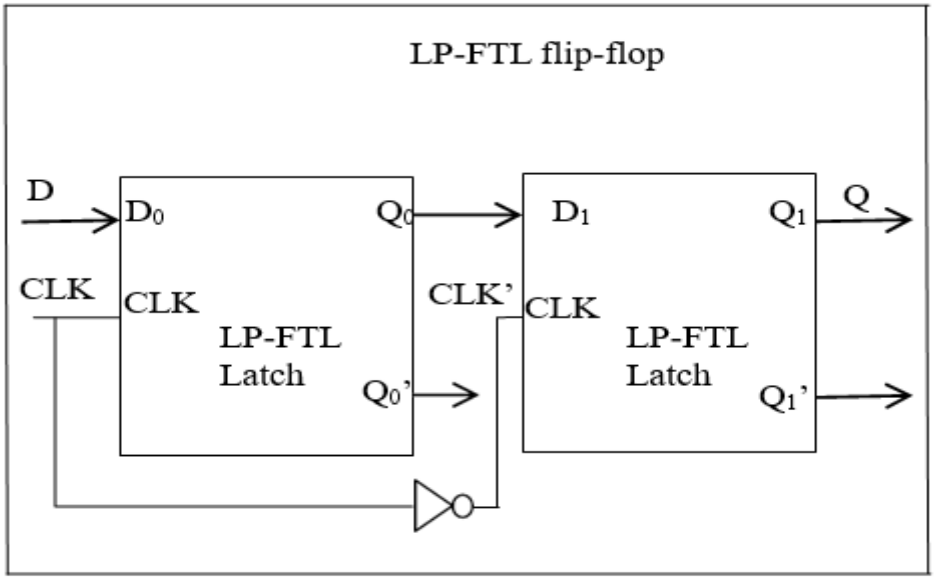


Figure 8 Positive edge triggered D flip-flop

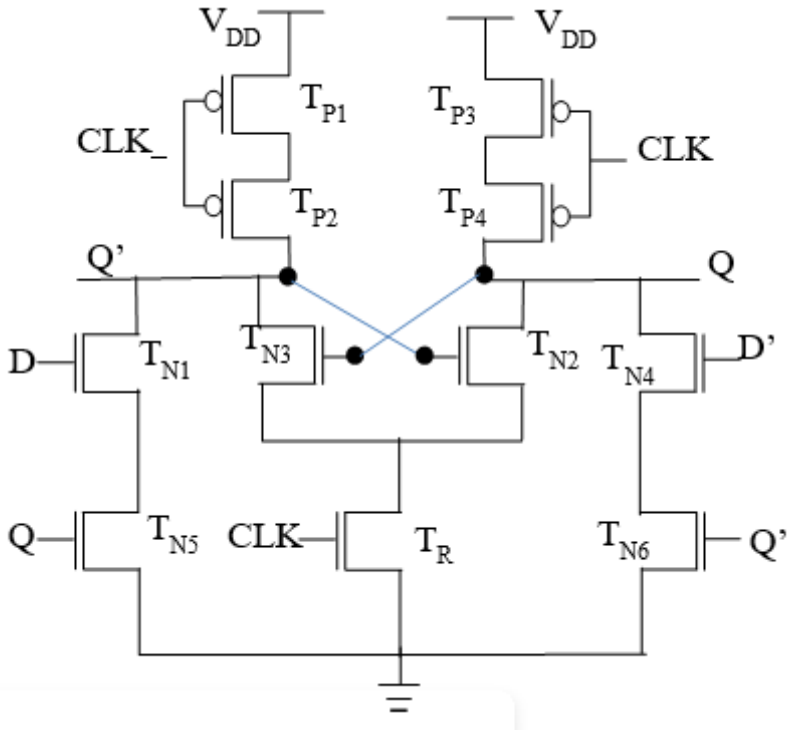


Figure 9. D-latch using LP-FTL3.4

2.3.1. Operation of D-latch

The circuit diagram of D-latch by using LP-FTL structure is shown in Figure 9. The operation of D-latch as follows. During the reset phase i.e. when CLK =1, TR turned on, both the output node Q and Q' holds their last state. During evaluation phase i.e. when CLK =0 TR turned off, depending upon D Value Q and Q' are updated.Suppose when CLK=0 and D=1,

i) if in the last state Q=0 and Q'=1, then node Q charged to VDD through TP3 and TP4, since now D=1 and Q=1, hence the transistor TN1 and TN5 are turned on as a result node Q' will evaluates to a logic low i.e. VOL.Two cascaded FTL latch forms a positive edge triggered D-flip flop as shown in Figure-. ii) When CLK=0, the 1st LP-FTL latch is evaluated at the same time 2nd LP-FTL latch holds the last state. The input D is latched at the output of 1st FTL- latch. When CLK goes from 0 to 1, the 2nd FTL latch is in evaluation phase the previously latched D value comes at the output of 2nd LP-FTL latch.

2.3.2. Simulation Results of LFSR

The average power consumption and propagation delay of LFSR is shown in Table 3

iii). The proposed LP-FTL structure consumes less dynamic power as compared to existing FTL. The waveforms at X1, X2, X3, X4 after every clock pulse is shown in Figure 10.

Table 3. Power and propagation Delay Comparison between FTL and LP-FTL for

Logic family	**P_{avg}(µW)**	**t_p(ns)**
FTL	349	5.167
ProposedLP-FTL	196	5.290

Figure 10. Output wave form at the X1, X2, X3, X4 of LFSR and total power

2. Design and simulation of ofHS-FTLStructure:

In order to improve the speed of proposed LP-FTL structure the reset transistor TR is connected to VDD/2 as shown in Figre11 (a). The operation of this circuit is as follows, when CLK =1, the output node (OUT) will charges to the threshold voltage VTH. During evaluation phase according to input value the output node only makes partial transition from VTH to VOH or VOL. Since during evaluation phase the output node (OUT) only makes partial transitions, this improves propagation delay. An inverter designed by using HS-FTL is shown in Figure 11 (b).

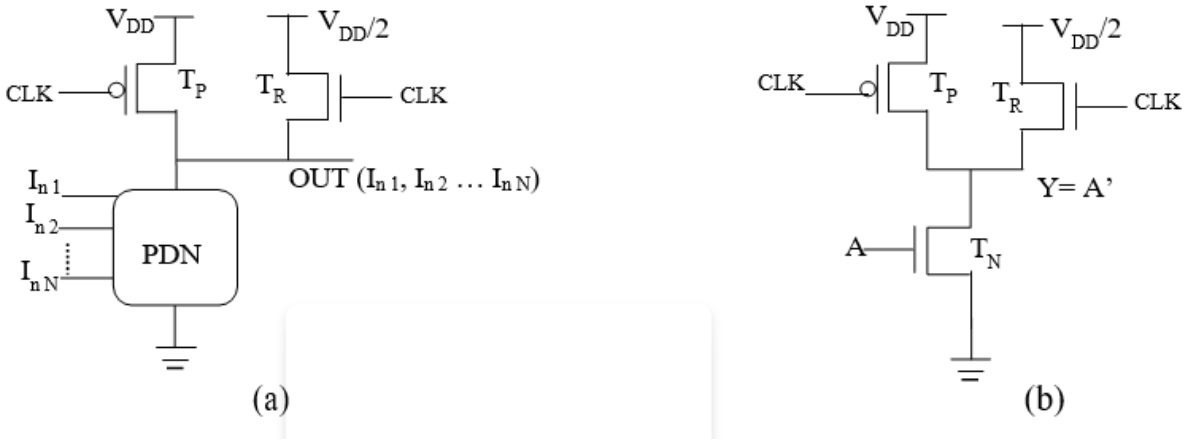


Fig 11.(a)ProposedmodifiedHS-FTL.(b)HS-FTLinverter

3.1 Performance analysis of HS-FTL

The performance analysis of the HS-FTL structure is carried out by designing various cascaded combinational circuits. We have designed a long chain of inverter (10-stage), 8-bit RCA by using HS-FTL structure. We have used 0.18-um CMOS process technology model library from UMC, using the parameter for typical process corner at 25 0C. Power supply VDD is constant for all simulations and is equal to 1.8V. Circuits are simulated in HSPICE simulator.

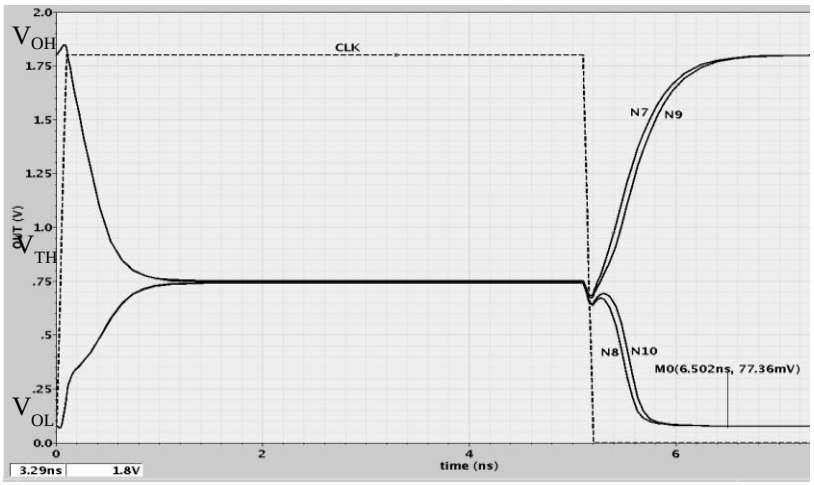


Figure 12. Plot of the output voltages from 1st stage (N1) to 10th stage (N10) of inverter in HS-FTL

From Figure 12 during CLK=1, the output node at each stage of inverter charges to VTH. When CLK goes from 1 to 0 all the output nodes makes transition from VTH to either VOH or VOL only. The simulation result for a long chain of inverter (10-stage) is given in Table 2.4. From the Table 4.the PDP of both the improved structure is better as compared to the FTL in [15].

Table 4. Simulation results comparison between FTL, LP-FTL and HS-FTL in terms of power, delay (10-inverter chain)

Logicfamily	**P_{avg}(µW)**	**t_p(ns)**	**PDP (µW*ns)**
FTLin[15]	270	0.725	195.75
ProposedLP-FTL	152	0.830	126.16
ProposedHS-FTL	290	0.538	156.02

Table 5 Simulation results for an 8-bit RCA designed by proposed FTL structure and the existing FTL structure [15]

Logicfamily	**P_{avg}(µW)**	**t_p(ns)**	**PDP (µW*ns)**
FTLin[15]	732	0.620	453.84
LP-FTL	422	0.681	287.382
HS-FTL	735	0.430	316.05

Table 5 shows average power consumption, propagation delay time (tp), and power delay product (PDP) of existing FTL structure in [15], LP-FTL and HS-FTL structure. The proposed HS-FTL structure achieves a speed up factor of 1.58 with respect to LP-FTL structure and 1.44 with respect to existing FTL structure. The power delay product of both the proposed structures are better as compared to the existing FTL structure. The PDP improves due to reduction of power in LP-FTL and reduction of average propagation delay in HS-FTL structure.

3.Conclusions

This paper presents performance analysis of two improved FTL i.e. LP-FTL and HS-FTL. Both these FTL structure provides improvement in speed

ascompared domino CMOS. The RCA designed by LP-FTL structure is 3.68 times faster thandomino and reduces the average power consumption by 42% as compared to existing FTL.This LP-FTL structure suffers from area overhead and increases in propagation delay ascompared toexistingFTL. In order toimprove propagation delay further, HS-FTL structureisproposed.ThisHS-FTLstructureimprovesspeedwithoutareaoverhead.Boththeseimproved FTLstructure provideslessPDPascomparedtoexistingFTL.

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