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Design of Digital Logic Circuits Using Memristor

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ABSTRACT

Many inventions in the VLSI field have resulted from the introduction of the memristor. The features of memristors, such as nanoscale scale measurements and nonvolatile memory capabilities, have attracted increased study attention. The memristor's nanometer-scale feature opens up a new avenue for developing novel circuits for logic blocks that aren't available in more traditional designs.Non-volatile memory property empowers us to acknowledge new outline strategies for an assortment of computational components that prompt novel models. By this, there comes the idea of the combination of the Nano-scale memristor and CMOS, which ends up conceivable to diminish usage of silicon territory accordingly giving a promising alternative in the plan of memristor and CMOS based circuits. In this paper, we are presenting a combinational and sequential circuit design using memristor and CMOS logic as well as the implementation of a built-in self-test circuit to test the core functionalities of the logic. It consists of a test pattern generator and an output response analyzer that compares the output response of the unit under test circuit to the unit under test's pre-stored predicted patterns. Designing the circuit with this combination of memristor and CMOS saves a lot of chip area and power while also being very dependable

INTRODUCTION

The technique of building an integrated circuit (IC) by merging thousands of transistors into a single chip is known as very-scale-scale integration (VLSI). With the advancement of semiconductor and communication technologies in the 1970s, VLSI was born. A VLSI device is used as the microprocessor.

VLSI is a type of integrated circuit that has several devices on a single chip. The word, like many other scale integration classifications based on the number of gates or transistors per IC, dates back to the 1970s.The advancements in large-scale integration technologies are principally responsible for the electronics industry's extraordinary growth. The number of options for ICs in control applications, telecommunications, high-performance computing, and consumer electronics as a whole continues to grow with the emergence of VLSI designs.

Due to VLSI technology, current technologies such as smartphones and cellular communications provide unparalleled mobility, processing capacity, and application access. As demand continues to rise, the projection for this trend implies a quick growth.

Prior to the development of VLSI technology, most ICs could only execute a limited number of jobs. CPU, ROM, RAM, and other sensible glue may be found in the electronic circuit. VLSI enables IC designers to combine all of these features into a single chip.Power utilization is a significant thought in the plan of Very Large-Scale Integration (VLSI) circuits, which utilize the Complementary Metal Oxide Semiconductor (CMOS) as the major innovation. The ongoing spotlight on low power isn't only because of the new ascent in portable application needs. Power utilization has forever been a significant issue, even before the portable age. Numerous analysts have introduced numerous strategies to defeat the power dispersal issue, going from the gadget level to the compositional level and then some. In any case, since there is no uniform answer for wipe out tradeoffs between power, dormancy, and region, fashioners should pick OK ways to deal with meet application and item prerequisites.

CMOS power utilization is comprised of both dynamic and static parts. At the point when semiconductors switch, dynamic power is consumed, and static power is consumed paying little mind to semiconductor flipping. Since dynamic power represented 90% or a greater amount of all out chip power (at 0.18 innovation or more), it was generally the absolute most significant concern for low-power chip planners.

Therefore, a few recently proposed approaches zeroed in on unique power decrease, for example, voltage and recurrence scaling. Static power has turned into a central issue for existing and future innovation as component sizes diminish, for instance, to 0.09 and 0.065. Kim et al. show that subthreshold spillage power scattering of a chip might outperform dynamic power dissemination at the chip level, in light of the International Technology Roadmap for Semiconductors (ITRS).

Expanded subthreshold spillage power is one of the essential drivers of spillage power development. At the point when the size of a specialized component is decreased, the stock voltage and edge voltage are diminished too. As edge 1 voltage brings down, subthreshold spillage power develops dramatically. Moreover, the short channel gadget's development diminishes the edge voltage considerably further. Entryway oxide spillage power, brought about by the burrowing current by means of the door oxide separator, adds to spillage power notwithstanding subthreshold spillage. Since entryway oxide thickness will drop as innovation propels, door oxide spillage power in nanoscale innovation might be identical to subthreshold spillage power on the off chance that not controlled suitably. Notwithstanding, we expect that elective methodologies will be utilized to settle entryway oxide spillage, for example, high-k dielectric door encasings.

MEMRISTOR

A memristor is a non-linear two-terminal electrical component involved in the connection of electric charge and magnetic flux. It was described and named by Leon Chua in 1971 and also completes a theoretical quartet of basic electrical components consisting of resistor, capacitor, and inductor.

Chua and Kang later generalized the concept to memory systems.[2] Such a system includes a circuit consisting of a plurality of conventional components, also commonly referred to as a memristor, which mimics the essential properties of the ideal memristor component. Several such memristor system technologies have been developed, particularly Re RAM.

The definition of mnemonic features in electronic devices has caused controversy. Experimentally, the ideal memristor has not yet been proven.

Chua in his 1971 paper identified a theoretical symmetry between the non-linear resistor (voltage vs. current), non-linear capacitor (voltage vs. charge), and non-linear inductor (magnetic flux linkage vs. current). From this symmetry he inferred the characteristics of a fourth fundamental non-linear circuit element, linking magnetic flux and charge, which he called the memristor. In contrast to a linear (or non-linear) resistor the memristor has a dynamic relationship between current and voltage including a memory of past voltages or currents. Other scientists had proposed dynamic memory resistors such as the memistor of Bernard Widrow, but Chua introduced a mathematical generality.

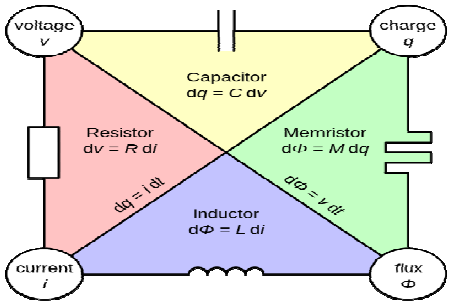

Figure 4.1: Fundamental Elements

4.2 DERIVATION AND CHARACTERISTICS

The memristor was originally defined in terms of a non-linear functional relationship between magnetic flux linkage $\Phi_m(t)$ and the amount of electric charge that has flowed, q(t):

$$f(\Phi_{\mathrm{m}}(t), q(t)) = 0$$

The magnetic flux linkage, Φ_m, is generalized from the circuit characteristic of an inductor. It does not represent a magnetic field here. Its physical meaning is discussed below.

$$M(q) = \frac{\mathrm{d}\Phi_{\mathrm{m}}}{\mathrm{d}q}$$

The symbol Φ_m may be regarded as the integral of voltage over time.

$$M(q(t)) = \frac{\mathrm{d}\Phi/\mathrm{d}t}{\mathrm{d}q/\mathrm{d}t} = \frac{V(t)}{I(t)}$$

In the relationship between Φ_m and q, the derivative of one with respect to the other depends on the value of one or the other, and so each memristor is characterized by its memristance function describing the charge-dependent rate of change of flux with charge. Substituting the flux as the time integral of the voltage, and charge as the time integral of current, the more convenient forms are; To relate the memristor to the resistor, capacitor, and inductor, it is helpful to isolate the term M(q), which characterizes the device, and write it as a differential equation.

Table 4.2.1: Differential Equations

Device	Characteristic property (units)	Differential equation
Resistor (R)	Resistance (V / A, or ohm, Ω)	R = dV / dI
Capacitor (C)	Capacitance (C / V, or farad)	C = dq / Dv
Inductor (L)	Inductance (Wb / A, or henry)	L = $d\Phi_m$ / dI
Memristor (M)	Memristance (Wb / C, or ohm)	M = $d\Phi_m$ / dq

The above table covers all meaningful ratios of differentials of I, q, Φ_m, and V. No device can relate dI to dq, or $d\Phi_m$ to dV, because I is the derivative of q and Φ_m is the integral of V.

It can be inferred from this that memristance is charge-dependent resistance. If M(q(t)) is a constant, then we obtain Ohm's Law R(t) = V(t)/I(t). If M(q(t)) is nontrivial, however, the equation is not equivalent because q(t) and M(q(t)) can vary with time. Solving for voltage as a function of time produces

This equation reveals that memristance defines a linear relationship between current and voltage, as long as M does not vary with charge. Nonzero current implies time varying charge. Alternating current, however, may reveal the linear dependence in circuit operation by inducing a measurable voltage without net charge movement—as long as the maximum change in q does not cause much change in M.

Furthermore, the memristor is static if no current is applied. If I(t) = 0, we find V(t) = 0 and M(t) is constant. This is the essence of the memory effect. Analogously, we can define

$$i(t) = W(\phi(t))v(t)$$

The power consumption characteristic recalls that of a resistor, I^2R.

$$P(t) = I(t)V(t) = I^2(t)M(q(t))$$

As long as M(q(t)) varies little, such as under alternating current, the memristor will appear as a constant resistor. If M(q(t)) increases rapidly, however, current and power consumption will quickly stop.M(q) is physically restricted to be positive for all values of q (assuming the device is passive and does not become superconductive at some q). A negative value would mean that it would perpetually supply energy when operated with alternating current.

4.3 MODELING AND VADILATION

In order to understand the nature of memristor function, some knowledge of fundamental circuit theoretic concepts is useful, starting with the concept of device modelling

Engineers and scientists seldom analyze a physical system in its original form. Instead, they construct a model which approximates the behaviour of the system. By analyzing the behaviour of the model, they hope to predict the behaviour of the actual system. The primary reason for constructing models is that physical systems are usually too complex to be amenable to a practical analysis.

In the 20th century, work was done on devices where researchers did not recognize the memristive characteristics. This has raised the suggestion that such devices should be recognised as memristors. Pershin and Di Ventra have proposed a test that can help to resolve some of the long-standing controversies about whether an ideal memristor does actually exist or is a purely mathematical concept.

The rest of this article primarily addresses memristors as related to ReRAM devices, since the majority of work since 2008 has been concentrated in this area.Dr. Paul Penfield, in a 1974 MIT technical repor mentions the memristor in connection with Josephson junctions. This was an early use of the word "memristor" in the context of a circuit device.

One of the terms in the current through a Josephson junction is of the form:

$$\begin{aligned} i_M(v) &= \epsilon \cos(\phi_0)v \\ &= W(\phi_0)v \end{aligned}$$

4.5 MEMRISTOR CIRCUITS

Due to the practical difficulty of studying the ideal memristor, we will discuss other electrical devices which can be modelled using memristors. For a mathematical description of a memristive device (systems),

A discharge tube can be modelled as a memristive device, with resistance being a function of the number of conduction electrons

4.6 INTRODUCTION TO REVERSABLE LOGIC GATES

Reversible rationale has gotten extraordinary consideration in the new years because of their capacity to diminish the power scattering which is the fundamental necessity in low power VLSI plan. It has wide applications in low power CMOS and Optical data handling, DNA processing, quantum calculation and nanotechnology. Irreversible equipment calculation brings about energy scattering because of data misfortune. As per Landauer's exploration, how much energy disseminated for each irreversible bit activity is something like KTln2 joules,) is the Boltzmann's consistent and T is the temperature at which activity is performed.

The intensity created because of the deficiency of the slightest bit of data is tiny at room temperature however when the quantity of pieces is more as on account of fast computational works the intensity disseminated by them will be enormous to the point that it influences the exhibition and results in the decrease of lifetime of the parts In 1973, Bennett showed that KTln2 energy wouldn't scatter from a framework as long as the framework permits the multiplication of the contributions from noticed yields.

Reversible rationale upholds the method involved with running the framework both forward and in reverse. This implies that reversible calculations can create inputs from yields and can go back and forth back to any point in the calculation history. A circuit is supposed to be reversible on the off chance that the info vector can be remarkably recuperated from the result vector and there is a coordinated correspondence between its feedback and result tasks, i.e., not just the results can not entirely set in stone from the data sources, yet in addition the data sources can be recuperated from the results Energy scattering can be diminished or even killed assuming calculation becomes Information-lossless. A circuit is supposed to be reversible on the off chance that the info vector can be particularly recuperated from the result vector and there is a balanced correspondence between its feedback and result tasks. A circuit is supposed to be reversible in the event that the info vector can be extraordinarily recuperated from the result vector and there is a

coordinated correspondence between its feedback and result tasks. Irreversible equipment calculation brings about energy scattering because of data misfortune.

4.7 PARAMETERS RELATETED TO REVESIBLE GATES

Reversible Gate

Reversible doors are circuits in which number of results is equivalent to the quantity of data sources and there is balanced correspondence between the vector of data sources and results. A reversible entryway is reversible provided that data sources = yields.

Garbage Output

Undesirable result of reversible entryway is called trash yield. The result of reversible door isn't utilized as an essential result or as contribution to different entryways is called trash yield. Trash's results are required in circuit to keep up with reversibility idea. For instance when 3x3 Toffoli door is utilized to carry out the activities like AND EX-OR, result vector created P=A, Q=B These additional result called trash yield.

Quantum Cost

Quantum cost of the circuit is determined by knowing the quantity of basic(primitive) reversible entryways expected to understand the circuit. Quantum cost of 1x1 reversible entryway is zero and quantum cost of 2x2 reversible door is 1. Quantum entryways have some property given in condition 1, 2 and 3.

1. V*V=NOT
2. V*V+ =V+*V=1
3. V+*V+=NOT

Restriction on Reversible rationale combination

In planning reversible circuit utilizing reversible entryway need to keep up with certain restraints, for example, more than one fan-out isn't permitted and circle or criticism is completely limited.

Delay of Reversible Circuit

Postponement of reversible circuit is characterized as deferral of basic way. Here Critical way express that the most extreme number of entryways for any contribution to any result in the circuit. Every reversible entryway will set aside some margin for inner rationale tasks in the circuit.

4.8 NOTATION AND BACKGOUND

Reversibility in processing suggests that no data about the computational states can at any point be lost, so we can recuperate any prior stage by registering in reverse or un-figuring the outcomes. This is named as sensible reversibility. The advantages of sensible reversibility can be acquired solely after utilizing actual reversibility. Actual reversibility is a cycle that disseminates no energy to warm. Totally amazing actual reversibility is essentially impossible. Processing frameworks radiate intensity when voltage levels change from positive to negative: bits from zero to one. A large portion of the energy expected to roll out that improvement is emitted as intensity. As opposed to changing voltages higher than ever, reversible circuit components will step by step move charge starting with one hub then onto the next. Along these lines, one can hope to lose brief measure of energy on each change. Reversible figuring emphatically influences computerized rationale plans. Reversible rationale components are expected to recuperate the condition of contributions from the results. It will affect guidance sets and undeniable level programming dialects also. Ultimately, these will likewise must be reversible to give ideal effectiveness.

A reversible rationale door is a n-input n-yield rationale gadget with balanced planning. This assists with deciding the results from the sources of info and furthermore the data sources can be interestingly recuperated from the results. Additionally, in the amalgamation of reversible circuits direct fan-Out isn't permitted as one-to-numerous idea isn't reversible. Nonetheless, fan-out in reversible circuits is accomplished utilizing extra entryways. A reversible circuit ought to be planned utilizing least number of reversible rationale doors.

According to the perspective of reversible circuit plan, there are numerous boundaries for deciding the intricacy and execution of circuits.

- The quantity of Reversible entryways (N): The quantity of reversible doors utilized in circuit.
- The quantity of consistent data sources (CI): This alludes to the quantity of data sources that are to be maintained steady at one or the other 0 or 1 to incorporate the given legitimate capacity.
- The quantity of trash yields (GO): This alludes to the quantity of unused results present in a reversible rationale circuit. One can't keep away from the trash yields as these are very fundamental to accomplish reversibility.
- Quantum cost (QC): This alludes to the expense of the circuit as far as the expense of a primitive door.

4.9 BASIC REVERSIBLE LOGIC GATES

Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 4.9.1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A ⊕ B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs

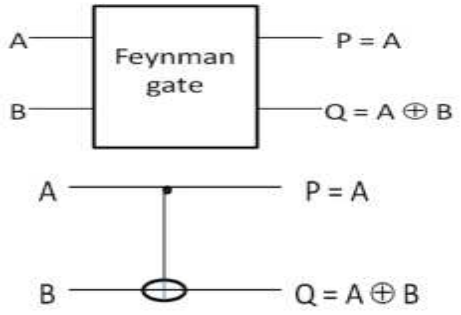

Figure 4.9.1: FEYNMAN GATE

Peres Gate

Figure 4.9.2 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A ⊕ B and R=AB ⊕ C. Quantum cost of a Peres gate is 4.

In the proposed design Peres gate is used because of its lowest quantum cost.

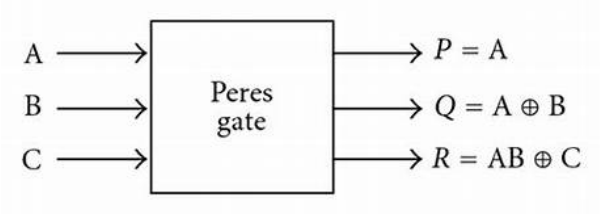

Figure 4.9.2: Peres Gate

Fredkin Gate

Figure 4.9.3 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B ⊕ AC and R=A′C ⊕ AB. Quantum cost of a Fredkin gate is 5.

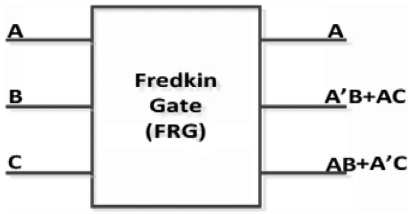

Figure 4.9.3: Fredkin Gate

TR GATE

The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A ⊕ B and R=AB' ⊕ C. Quantum cost of a TR gate is 4. In the proposed design TR gate is used because of its lowest quantum cost.

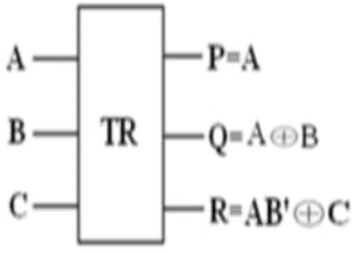

Figure 4.9.4: TR GATE

SOFTWARE USED

5.1 FALSTAD:

Circuit Simulators A circuit simulator is a great way to learn about circuits, test new designs, or troubleshoot a design prototype that has failed on the breadboard. Eventually, we will teach you to use the LTspice simulator which provides better precision, better visualization tools, the ability

to save circuits for later exploration, and the ability to add our own components. However, an installation is required and the learning curve is a little higher and, even for simple circuits, the added steps in running a small simulation can be intimidating. The circuit simulator at https://www.falstad.com/circuit provides a good first view of a circuit simulator that yields results in seconds

If you limit yourself to certain components like resistors, capacitors, switches, and inductors (bearing in mind the limitation mentioned above), the Falstad simulator will do a very nice job of simulating things. It's also pretty good for simulating simple logic circuits, though its library of chips is rather limited

Circuit simulation is a process in which a model of an electronic circuit is created and analyzed using various software algorithms, which predict and verify the behavior and performance of the circuit.

RESULTS

The proposed design is successfully implemented in FALSTAD tool

6.1 SIMULATION CIRCUIT AND WAVEFORM

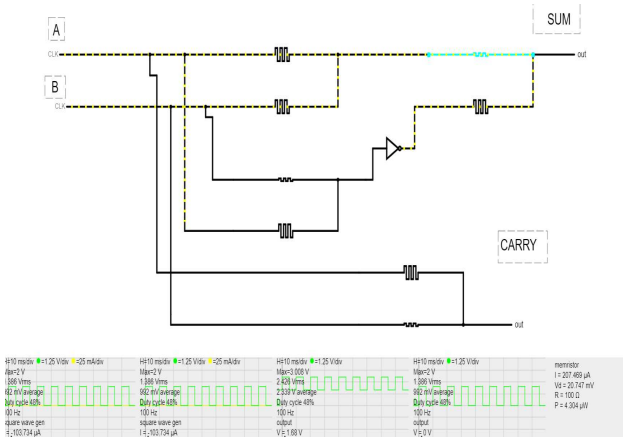

Figure 6.1: Half Adder

Figure 6.1 shows the half adder circuit using memristors, inputs are A and B, sum and carry represents the outputs. In order to construct the half adder, we required 8 memristors and one not gate where as in CMOS design we required 12 number of transistors. From this we can conclude that we required a smaller number of memristors for the construction of half adder with same operation when compared to the CMOS design, hence the die is required for the design of half adder is less when we design with memristors .2 volts is the maximum voltage, it is operating at 100Hz with approximately 48% duty cycle. The total power required in the design of half adder using memristors is approximately given by 4.304µw where as in the CMOS design the total power consumption is approximately 18µw, from this we can conclude that power required is less in case of half adder when we designed using memristors.

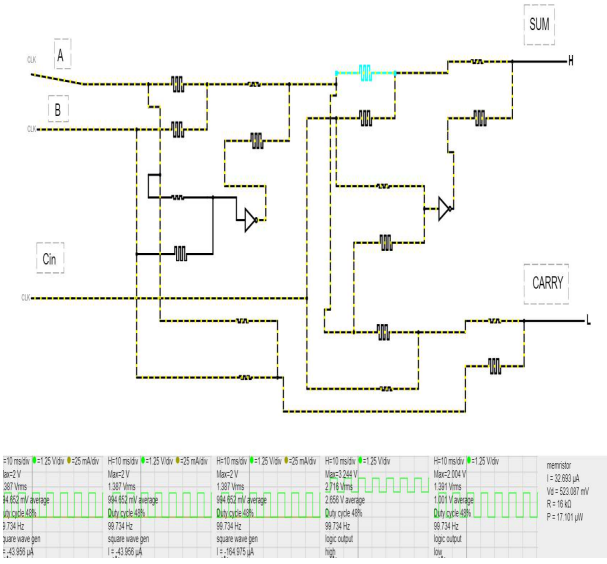

Figure 6.2: Full Adder

Figure 6.2 shows the full adder circuit using memristors, inputs are A, B and Cin, sum and carry represents the outputs. In order to construct the full adder, we required 18 memristors and 2 not gate where as in conventional CMOS design we required 24 number of transistors. From this we can conclude that we required a smaller number of memristors for the construction of full adder with same operation when compared to the CMOS design, hence the die is required for the design of half adder is less when we design with memristors .2 volts is the maximum voltage, it is operating at 99.734Hz with approximately 48% duty cycle. The total power required in the design of full adder using memristors is approximately given by 17. 101µw.Delay also very less in the memristors design when compared to CMOS design. So, in order to get efficient, less die area, less power and faster response we can go with memristor design digital circuit.

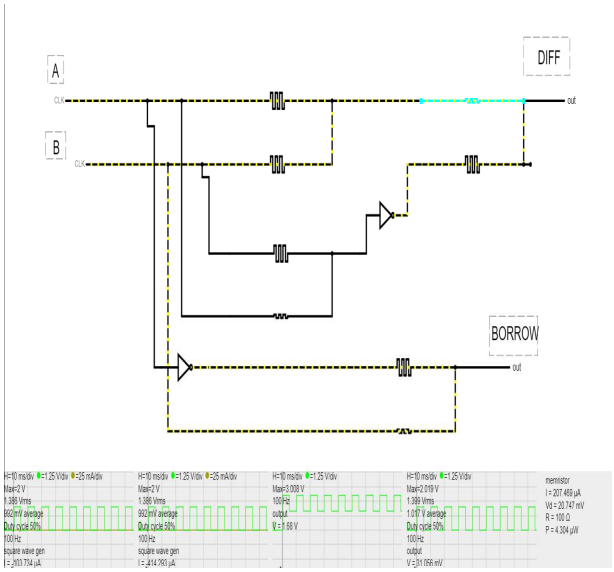

Figure 6.3: Half Substractor

Figure 6.3 shows the half substractor circuit using memristors, inputs are A and B, Diff and Borrow represents the outputs. In order to construct the half substractor, we required 8 memristors and 2 not gate where as in conventional CMOS design we required 18 number of transistors. From this we can conclude that we required a smaller number of memristors for the construction of half substractor with same operation when compared to the CMOS design, hence the die is required for the design of half substractor is less when we design with memristors .2 volts is the maximum voltage, it is operating at 100Hz with approximately 50% duty cycle. The total power required in the design of half substractor using memristors is approximately given by 4.304µw. Delay also very less in the memristors design when compared to CMOS design. So, in order to get efficient, less die area, less power and faster response we can go with memristor design digital circuit.

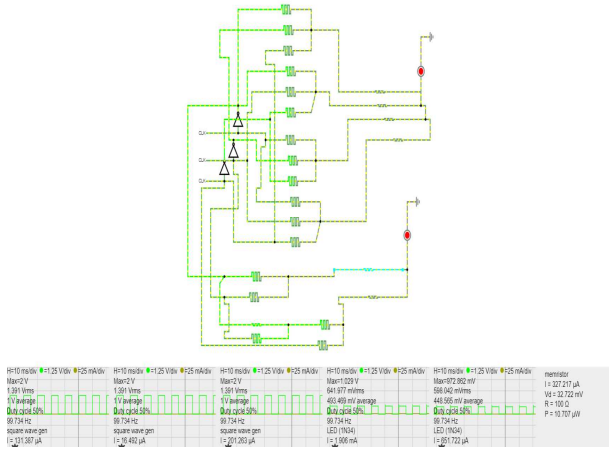

Figure 6.4: Full Substractor

Figure 6.4 shows the full substractor circuit using memristors, inputs are A, B and Bin, Diff and Borrow represents the outputs. In order to construct the half substractor, we required 24 memristors where as in conventional CMOS design we required 26 number of transistors. From this we can conclude that we required a smaller number of memristors for the construction of full substractor with same operation when compared to the CMOS design, hence the die is required for the design of full substractor is less when we design with memristors .2 volts is the maximum voltage, it is operating at 99.734Hz with approximately 50% duty cycle. The total power required in the design of full substractor using memristors is approximately given by 10.707µw. Delay also very less in the memristors design when compared to CMOS design. So, in order to get efficient, less die area, less power and faster response we can go with memristor design digital circuit.

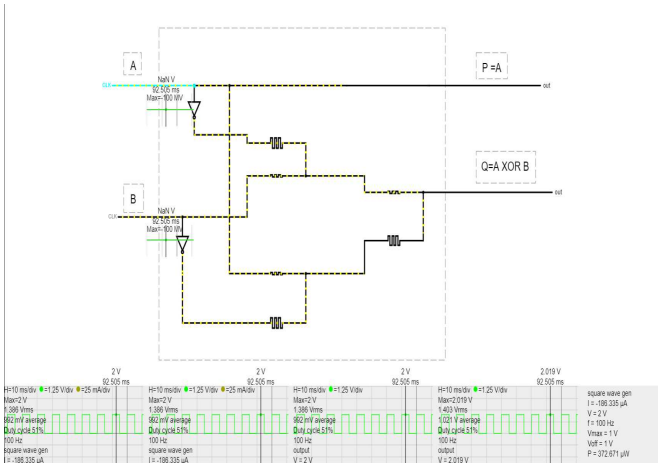

Figure 6.5: Feynman Gate

The total power consumed by the feynman gate using memristor is given by372.671µw.

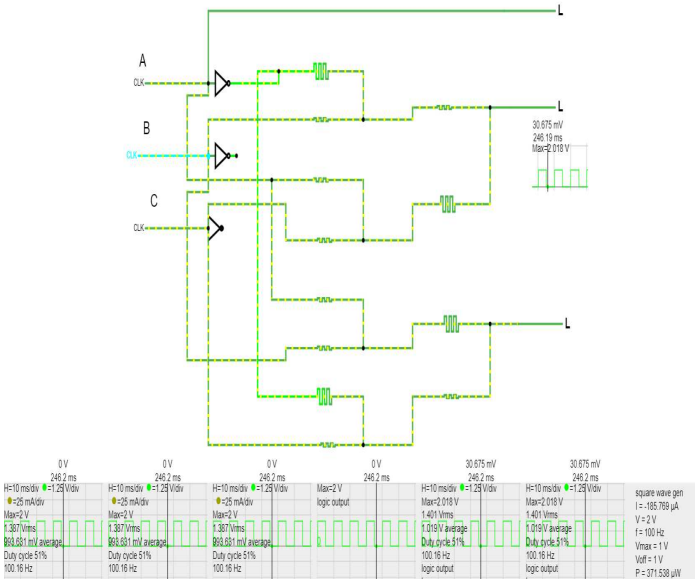

Figure 6.6: Fredkin Gate

The total power consumed by the fredkin gate using memristor is given by371.538µw.

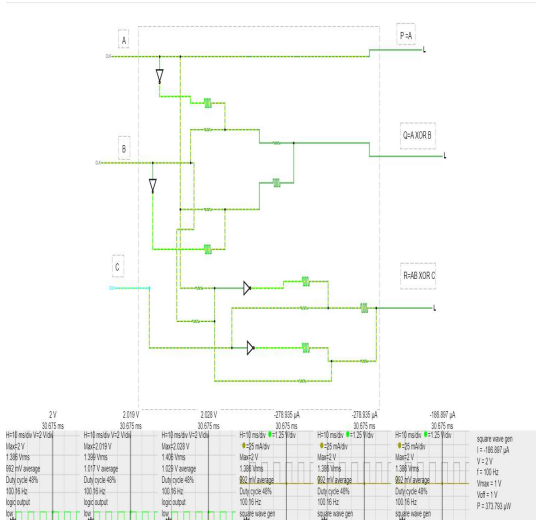

Figure 6.7: Peres Gate

The total power consumed by the peres gate using memristor is given by373.793µw.

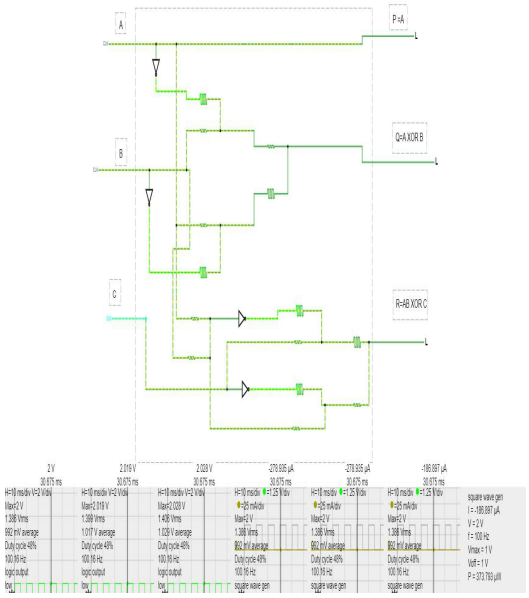

Figure 6.8: TR Gate

The total power consumed by the tr gate using memristor is given by373.793µw.

Figure 6.5,6.6,6.7 and 6.8 shows the basic reversable logic gates using memristor. The total power consumed by the feynman gate using memristor is given by 372.671µw. The total power consumed by the fredkin gate using memristor is given by 371.538µw. The total power consumed by the peres gate using memristor is given by 373.793µw. The total power consumed by the tr gate using memristor is given by 373.793µw.Here we can conclude the area also very small when compared to other technology, nonvolatility, low power consumption when compared to individual circuits hence we can save power. Capability to memorize the flow of chargers. Does not use power when they are in active provides better reliability. Generally, we have many advantages with reversable logic gates in terms of power, delay and area, by considering this when we design these gates with memristor we will get an efficient circuit design which combine the advantages of reversable logic gates and the advantages of memristor

CONCLUSION

We herewith investigated the design of digital circuits using the emerging nano-device called memristor. Additionally, we proposed the built-in self – test circuits to test the core functionality of the logic gates. We designed Reversable logic gates using memristor successfully.

Here we can conclude the area also very small when compared to other technology, nonvolatility, low power consumption when compared to individual circuits hence we can save power. Capability to memorize the flow of chargers. Does not use power when they are in active provides better reliability. Generally, we have many advantages with reversable logic gates in terms of power, delay and area, by considering this when we design these gates with memristor we will get an efficient circuit design which combine the advantages of reversable logic gates and the advantages of memristor

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