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Design of D Flip-Flops for High Performance VLSI Applications using CMOS Technology

Y. Vamsi Kalyan, M. Vineeth Kumar, P. Sreenath

Department of Electronics and Communication Engineering
Madanapalle Institute of Technology & Science
Madanapalle, Andhra Pradesh, India
malathivineethkumarmvk@gmail.com

ABSTRACT

There is vast variation encountered in present circuits because of aggressive scaling and process imperfections. So this paper deals with various D flip-flop circuits in terms of power and propagation delay. This work compares various known D flip-flop circuits and then identifies the circuit which is fastest as compared to others taken into consideration. In this paper, we have investigated the output levels of various D flip-flop circuits. Push-pull isolation D flip-flop proves to be more efficient as compared to other circuits in terms of delay variability. The circuits have been simulated using Microwind tool. The designs offering minimum delay and power , to aid the designer in selecting the best design depending on specific requirements.

Introduction

The technique of building an integrated circuit (IC) by merging thousands of transistors into a single chip is known as very-scale-scale integration (VLSI). With the advancement of semiconductor and communication technologies in the 1970s, VLSI was born. A VLSI device is used as the microprocessor's is a type of integrated circuit that has several devices on a single chip. The word, like many other scale integration classifications based on the number of gates or transistors per IC, dates back to the 1970s..The advancements in large-scale integration technologies are principally responsible for the electronics industry's extraordinary growth. The number of options for ICs in control applications, telecommunications, high-performance computing, and consumer electronics as a whole continues to grow with the emergence of VLSI designs.

Due to VLSI technology, current technologies such as smartphones and cellular communications provide unparalleled mobility, processing capacity, and application access. As demand continues to rise, the projection for this trend implies a quick growth.Prior to the development of VLSI technology, most ICs could only execute a limited number of jobs. CPU, ROM, RAM, and other sensible glue may be found in the electronic circuit. VLSI enables IC designers to combine all of these features into a single chip

Power utilization is a significant thought in the plan of Very Large-Scale Integration (VLSI) circuits, which utilize the Complementary Metal Oxide Semiconductor (CMOS) as the major innovation. The ongoing spotlight on low power isn't only because of the new ascent in portable application needs. Power utilization has forever been a significant issue, even before the portable age. Numerous analysts have introduced numerous strategies to defeat the power dispersal issue, going from the gadget level to the compositional level and then some. In any case, since there is no uniform answer for wipe out tradeoffs between power, dormancy, and region, fashioners should pick OK ways to deal with meet application and item prerequisites.

CMOS power utilization is comprised of both dynamic and static parts. At the point when semiconductors switch, dynamic power is consumed, and static power is consumed paying little mind to semiconductor flipping. Since dynamic power represented 90% or a greater amount of all out chip power (at 0.18 innovation or more), it was generally the absolute most significant concern for low-power chip planners. Therefore, a few recently proposed approaches zeroed in on unique power decrease, for example, voltage and recurrence scaling. Static power has turned into a central issue for existing and future innovation as component sizes diminish, for instance, to 0.09 and 0.065. Kim et al. show that subthreshold spillage power scattering of a chip might outperform dynamic power dissemination at the chip level, in light of the International Technology Roadmap for Semiconductors (ITRS).

D-flip-flops (Dff's) are one of the significant capacities in finite-state machines (FSM), which thus structure a basic piece of control rationale. It has been accounted for in [1] that the control rationale of a chip can use 21% of the processor's power. As further developed engineering ideas, for example, register renaming and mixed up execution in a superscalar chip [2], keep on overarching, the control rationale is probably going to turn out to be more complicated, and its power dissemination is probably going to develop past its ongoing level. Moreover, to support processor clock recurrence, current processors normally embrace super pipelined execution [2], which additionally utilizes Dff's. Further making DFF speed can either induce a higher clock rate or grant extra reasoning profundities between two pipeline registers. In this paper, we first glance at the area, speed, and power dispersal of existing DFF executions with a standard in general safe DFF [3], a low-region DFF, and a low-power DFF [4]. Then, we propose two energy-significant DFF plans: a push-pull DFF for execution and a push-pull isolation DFF (PPI-DFF) for execution and energy limit. These are

then isolated and the ceaseless plans and demonstrated to be better for most superb execution, energy-equipped applications. Discussion is then loose to the usage of twofold pass-semiconductor thinking (DPL) for speed and tri-granted circuit for diminishing short out power dispersal. Last, qualities of metastability of all the five DFF executions are inspected.

Flip-flops or the information stockpiling components are right around a fundamental part of each and every consecutive hardware. Among different flip-flops, D flip-flop is regularly utilized. It catches the worth of the D contribution at a specific predefined piece of the clock beat (rising or falling edge of the clock) and its result isn't impacted at different pieces of the clock. According to the timing point of view, postpone created by flip-flops consumes a huge piece of the process duration while the working recurrence increments. Throughout the course of recent many years CMOS innovation have gone under uncommon scaling with the perspective on mix thickness, fast and low power dispersal. By and by, a few additional obstacles have come into picture, which are more basic than prior. Changeability is one of them, characterized as the proportion of standard deviation (σ) to mean (μ) of any plan metric. These peculiarities have made semiconductors profoundly delicate to PVT (cycle, voltage and temperature) varieties. Planning a circuit of given details is incredibly troublesome. For lithography least element sizes utilized at 45-nm innovation hub have around diminished to quarter of frequency of light (at 45-nm innovation hub to patter 45 nm semiconductors 193 nm frequency of light is utilized), prompting obstacles like LER (line edge harshness) and LWR (line width unpleasantness) [1]. Remembering the previously mentioned issues, this paper explores for postponement and fluctuation different D flip-flops. Determination of a flip-flop has a significant impact in giving more leeway time to simpler time planning and hearty circuits in enormous frameworks. These reasons are expanding the interest of individuals in flip-flop plan and examination in late time. In the current situation there is a steadily expanding interest for quick and hearty gadgets. In this way, suitable choice of components at the exceptionally essential level, i.e., flip-flops is vital to acquire the ideal qualities to help the greater framework. Remembering these realities this paper gives the accompanying commitments:

1) It takes seven exceptional D flip-flop circuits and notice their differentiating yields.

2) Then the results are explored to check which circuit gives the most un-spread delay. Additionally, the eccentricity assessment of actuating delay is performed.

3) Finally, it wraps up with the best D flip-flop circuit like spread delay and its power.

Remaining paper is organized as follows. Area II talks about every one of the seven D flip-flops utilized for examination. Segment III gives the reproduction results (delay and its changeability) of the relative multitude of circuits displayed in area II. Area IV winds up with the end.

The term computerized in hardware addresses the information age, handling or putting away as two states. The two states can be addressed as HIGH or LOW, positive or non-positive, set or reset which is eventually parallel. The high 1 and low is 0 and consequently the advanced innovation is communicated as series of 0's and 1's. A model is 0110110 in which each term addresses a singular state. Along these lines, this hooking system in equipment is finished utilizing specific parts like lock or Flip-flop, Multiplexer, Demultiplexer, Encoders, Decoders and so on aggregately called as Sequential rationale circuits.

In this way, we will examine about the Flip-flops likewise called as hooks. The locks can likewise be perceived as Bistable Multivibrator as two stable states. By and large, these lock circuits can be either dynamic high or dynamic low and they can be set off by HIGH or LOW signals separately.

Types of flip-flops are,

1. RS Flip-flop
2. D Flip-flop
3. JK Flip-flop
4. T Flip-flop

The D in the D flip flop addresses the information (generation, handling, or putting away) as states. The two states are binary, 0 (Low) and 1 (High), set or reset, positive or non-positive.

4.2 D Latch

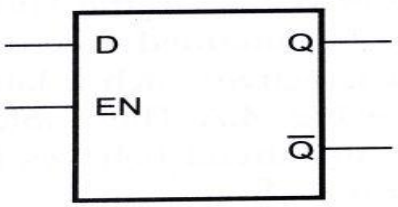

FIGURE 4.2.1: Logic Symbol

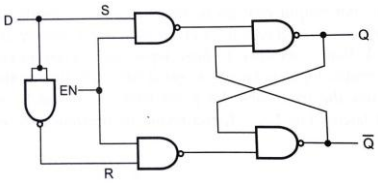

FIGURE 4.2.2: CIRCUIT DIAGRAM

The above figure shows the D latch. The NAND gates 1, 2, 3, and 4 structure the fundamental SR latch with enable information. The utilization of the fifth NAND entryway is to give the supplemented inputs.

TABLE 4.2.3: TRUTH TABLE OF D LATCH

EN	D	Qn	Qn+1	Stable
1	0	X	0	Reset
1	1	X	1	Set
0	X	X	Qn	No change (NC)

As shown in all actuality table, the Q yield follows the D data. In this manner, D latch is sometimes called a clear latch.
Looking at reality table for D latch with enable info and chipping away at Qn+1 work by k-map we get the brand name condition for D latch with engage input as

Qn+1 = EN * D + (EN)' * Qn.

Clocked D Flip-Flop

Like in D latch, in D flip-flop furthermore, the key SR flip flop is used with further developed inputs. The D flip flop seems to be D latch except for clock beat followed by edge identifier is used instead of empower data. Such an edge-set off D flip flop can be of two sorts:

- Positive edge-set off D flip flop
- Negative edge-set off D flip flop

Positive Edge Triggered D flip flop

It contains a gated D latch and a positive edge finder circuit. As shown in fact table under, the circuit yield answers the D information right at the positive edges of the clock beat. No less than a couple of sneak peaks of time, the D flip flop won't answer the improvements in input.

TABLE 4.4.1: TRUTH TABLE OF POSITIVE EDGE TRIGGERED D FLIP FLOP

CP	D	Qn+1
I	0	0
I	1	1
0	X	Qn

Seeing reality table for the D flip flop we can comprehend that Qn+1 work follows D obligation at the positive-going edges of the clock beats. In this manner, the brand name condition for D flip flop is Qn+1 = D. Regardless, the outcome Qn+1 is yielded by one clock period. In this way, D flip flop is all around called concede flip - flop.

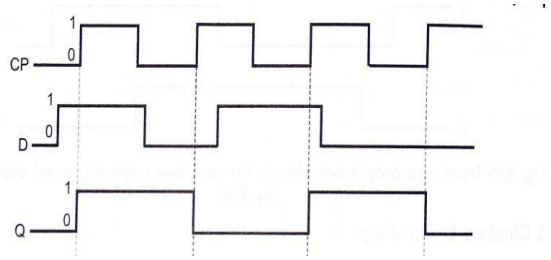

FIGURE 4.4.2: Input and output waveforms of clocked D flip flop

Expecting we accomplice the Q' aftereffect of D flip flop to its D information, the consequence of D flip flop will change either from 0 to 1 or from 1 to 0 at each specific edge of the D flip flop. Such a difference in the outcome is known as flipping of the flip flop yield.

Negative Edge Triggered D Flip Flop

In the above clarification, we have seen the aftereffect of D flip flop is precarious at the positive edge of the clock input. By excellence of negative edge setting off, the outcome is fragile at the negative edge of the clock input.

TABLE 4.5.1: TRUTH TABLE OF NEGATIVE EDGE TRIGGERED D FLIP FLOP

CP	D	Qn+1
I	0	0
I	1	1
0	X	Qn

The above truth table is for negative edge triggered D flip flop. Also, the input and output waveforms for negative edge triggered flip flop is as shown below:

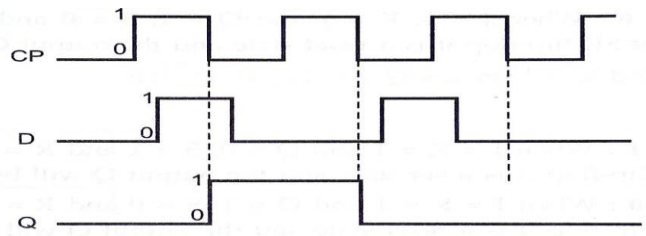

FIGURE 4.5.2: Input And Output Waveforms Of Negative Edge D Flip Flop

The above tables show the excitation table and truth table for D flip flop, uninhibitedly. In D flip flop, the going with state is liberated from the ongoing status and is reliably essentially indistinguishable from the D data. Thusly, D ought to be 0 enduring Qn+1 should be 0, and 1 expecting that Qn+1 should be 1, despite the value of Qn..In the end, if we look for an overwhelming assortment of this D flip flop, clearly, we can achieve it. We will add a second S R flip flop to its result. Might we eventually see how it further makes execution.

A few Applications of Flip Flops

- It is used as postpone parts.
- Goes all over are used as memory parts.
- It gets out key debounce.

RESULT

The proposed Symatic design is successfully implemented in DSCH tool

7.1 SYMATIC DIAGRAM

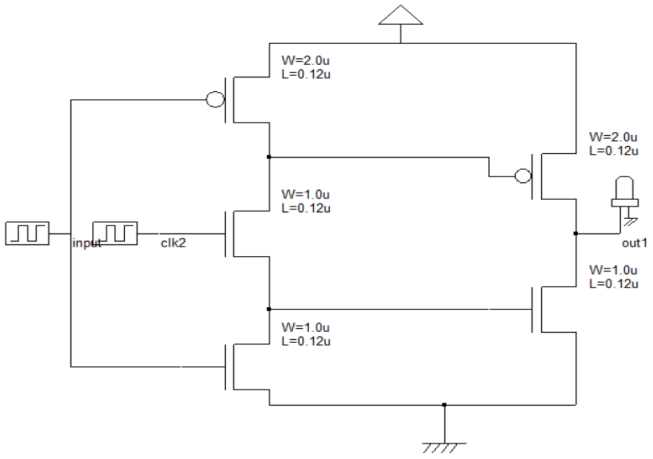

FIGURE 7.1.1: 5 TRANSISTOR D FLIP-FLOP

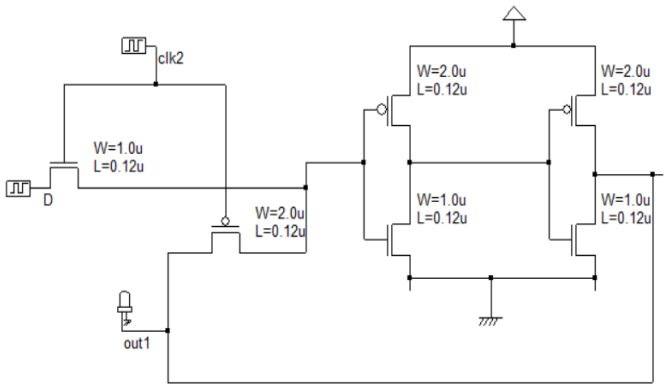

FIGURE 7.1.2: 6 TRANSISTOR D FLIP-FLOP

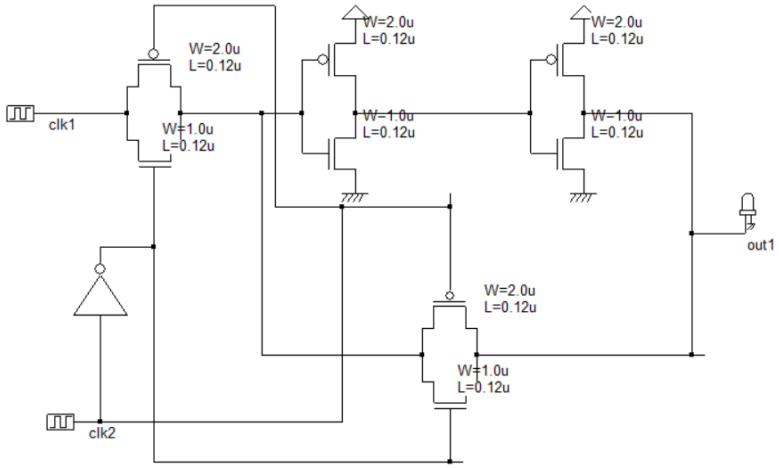

FIGURE 7.1.3: TRANSMISSION GATE D FLIP-FLOP

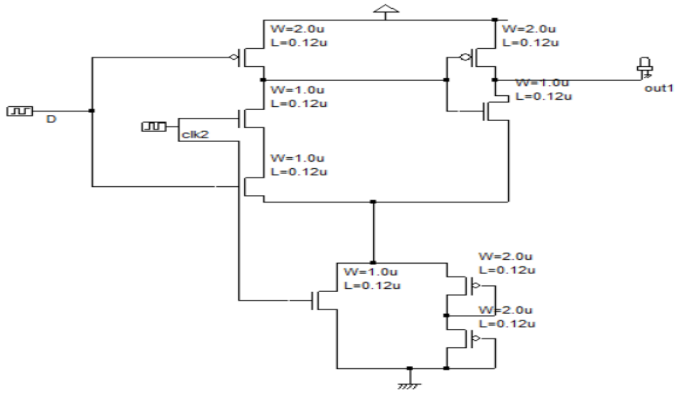

FIGURE 7.1.4: 8 TRANSISTOR D FLIP-FLOP

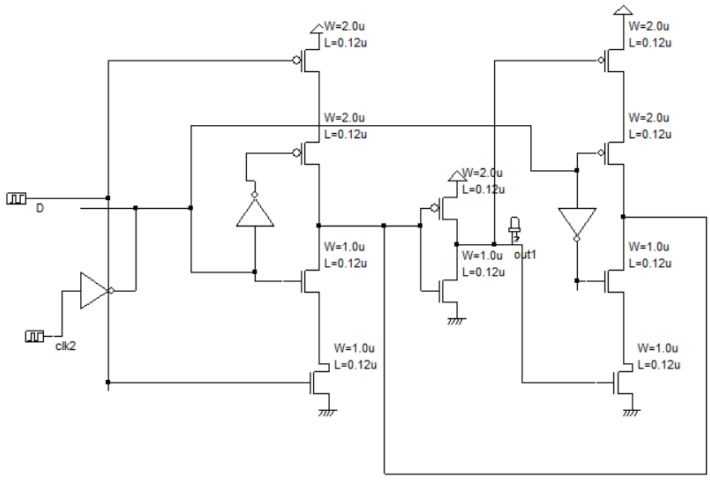

FIGURE 7.1.5: 10 TRANSISTOR D FLIP-FLOP

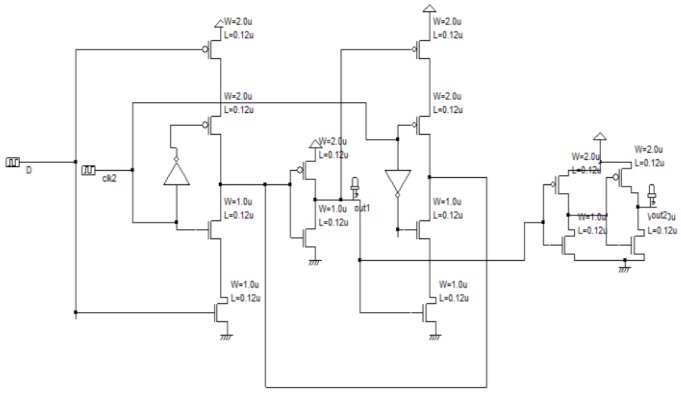

FIGURE 7.1.6: 14 TRANSISTOR D FLIP-FLOP

The proposed design is successfully implemented in MICROWIND tool

7.2 SIMULATION LAYOUT AND WAVEFORM
5 TRANSISTOR D FLIP-FLOP

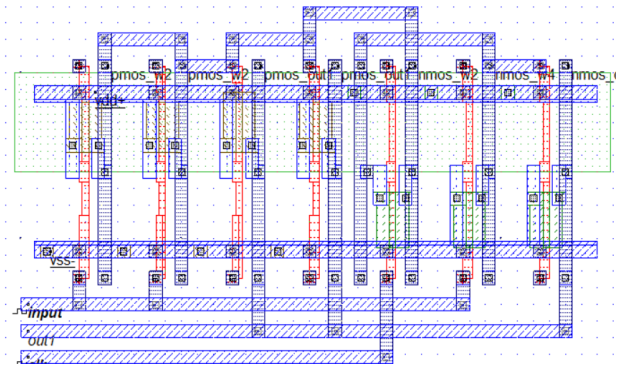

FIGURE 7.2.1: LAYOUT DESIGN

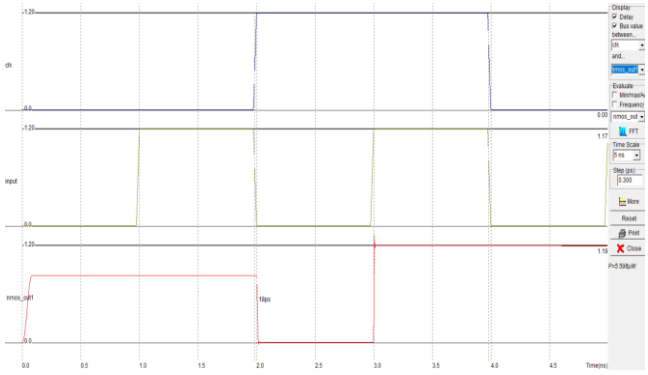

FIGURE 7.2.2: OUTPUT WAVEFORM

layout of 5transistor d flipflop is given in figure 7.2.1 and figure 7.2.2 is the output wave form of 5transistor d flipflop. The total power consumed by the d flipflop when we constructed with 5 transistors is given by 5.59µw.The total power consumed by the conventional d flipflop that's is 6 transistors d flipflop is given by 1.86µw.for 5 transistor d flipflop average clock to q delay is given by 17ps and the power delay product is given by 95.03aJ, from this we can conclude that for less delay we can prefer 5 transistor d flipflop.

6 TRANSISTOR D FLIP-FLOP

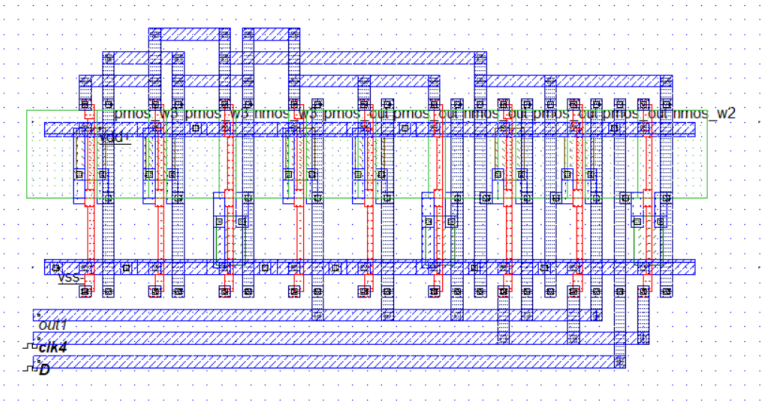

FIGURE 7.2.3: LAYOUT DESIGN

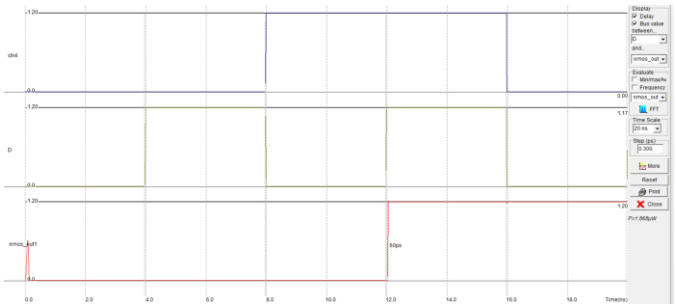

FIGURE 7.2.4: OUTPUT WAVEFORM

Layout of 6 transistor d flipflop is given in figure 7.2.3 and figure 7.2.4 is the output wave form of 6transistor d flipflop. The total power consumed by the d flipflop when we constructed with 6 transistors is given by 1.86µw. For 6 transistor d flipflop average clock to q delay is given by 59.5ps and the power delay product is given by 110.67aJ, from this we can conclude that for less power we can prefer 6 transistor d flipflop

TRANSMISSION GATE D FLIP-FLOP

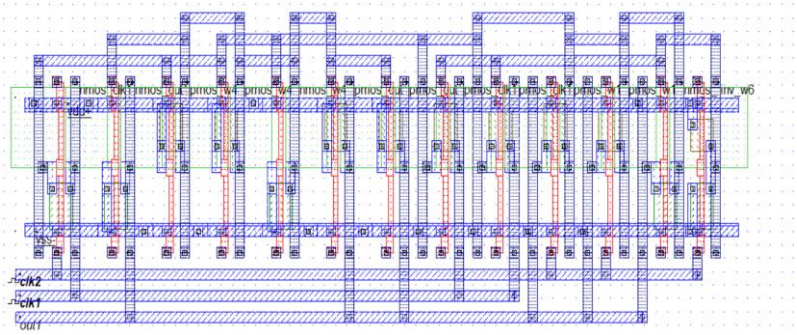

FIGURE 7.2.5: LAYOUT DESIGN

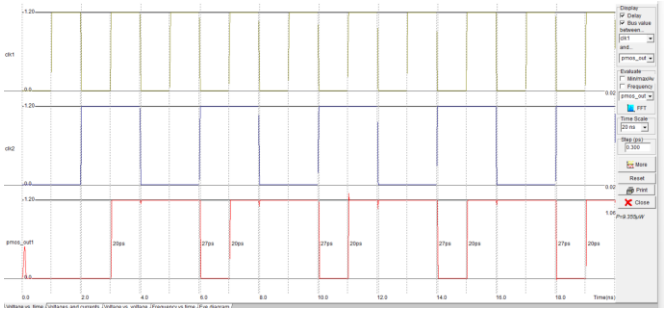

FIGURE 7.2.6: OUTPUT WAVEFORM

Layout of Transmission Gate D Flip-Flop is given in figure 7.2.5 and figure 7.2.6 is the output wave form of Transmission Gate D Flip-Flop. the total power consumed by the d flipflop when we constructed with transmission gate is given by 9.355µw. For this d flipflop average clock to q delay is given by 23.5ps and the power delay product is given by 215.165aJ.

8 TRANSISTOR D FLIP-FLOP

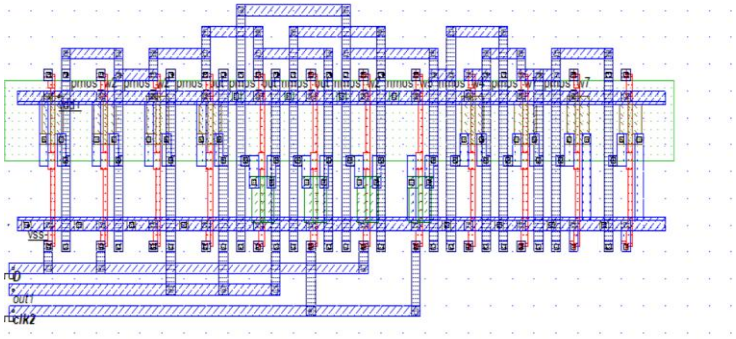

FIGURE 7.2.7: LAYOUT DESIGN

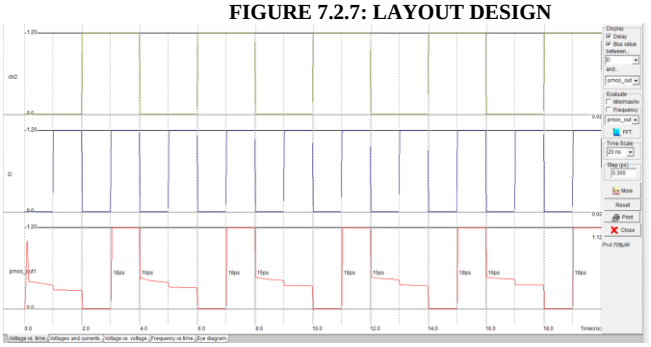

FIGURE 7.2.8: OUTPUT WAVEFORM

Layout of 8transistor d flipflop is given in figure 7.2.7 and figure 7.2.8 is the output wave form of 8transistor d flipflop. The total power consumed by the d flipflop when we constructed with 8 transistors is given by 6. 27µw.The total power consumed by the conventional d flipflop that's is 6 transistors d flipflop is given by 1.86µw.For 8transistor d flipflop average clock to q delay is given by 17.5ps and the power delay product is given by 109.75aJ, from this we can conclude that when compared to conventional d flipflop 8transistor d flipflop provides less delay.

10 TRANSISTOR D FLIP-FLOP

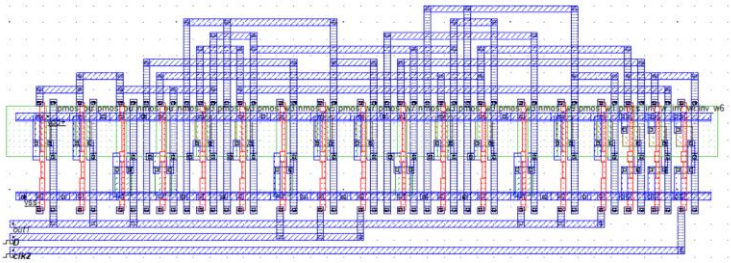

FIGURE 7.2.9: LAYOUT DESIGN

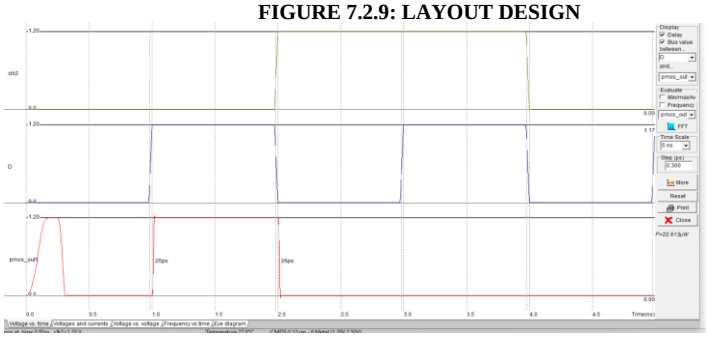

FIGURE 7.2.10: OUTPUT WAVEFORM

Layout of 10 transistor d flipflop is given in figure 7.2.9 and figure 7.2.10 is the output wave form of 10 transistor d flipflop. The total power consumed by the d flipflop when we constructed with 10 transistors is given by 24.28µw. The total power consumed by the conventional d flipflop that's is 6 transistors d flipflop is given by 1.86µw. For 10 transistor d flipflop average clock to q delay is given by 27ps and the power delay product is given by 648.16aJ, from this we can conclude that when compared to conventional d flipflop 10 transistor d flipflop provides less delay.

14 TRANSISTOR D FLIP-FLOP

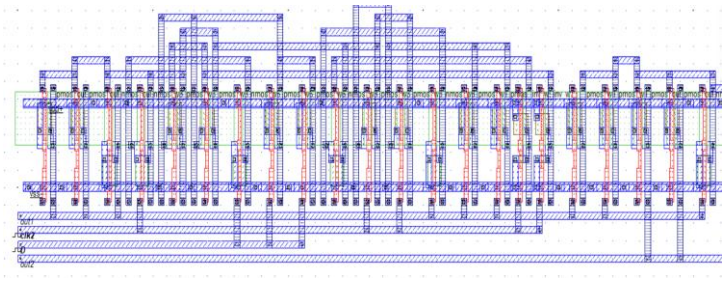

FIGURE 7.2.11: LAYOUT DESIGN

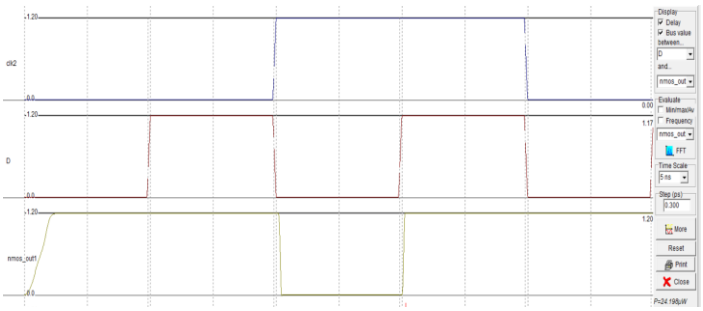

FIGURE 7.2.12: OUTPUT WAVEFORM

Layout of 14 transistor d flipflop is given in figure 7.2.19 and figure 7.2.20 is the output wave form of 14 transistor d flipflop. The total power consumed by the d flipflop when we constructed with 14 transistors is given by 25.53µw. The total power consumed by the conventional d flipflop that's is 6 transistors d flipflop is given by 1.86µw.For 14 transistor d flipflop average clock to q delay is given by 51.5ps and the power delay product is given by 284.79aJ, from this we can conclude that when compared to conventional d flipflop 14transistor d flipflop provides less delay.

CONCLUSION

A method for creating multifunctional binary reversible gates has been provided. These gates can be used to implement Boolean functions in regular circuits. Multiple-valued reversible gates with comparable features may also be built in the same way. Design of reversible logic gates and a D flipflop using fundamental reversible gates like the Feynman and Fredkin gates, as well as complementary metal oxide semiconductors and pass transistors. This study is a significant step forward in the development of big and sophisticated reversible sequential circuits. From this we came to conclude that among all types 5T based D flip-flop consumes less power and less delay so it can used in lower power devices.

TABLE 8.1: COMPARISION TABLE

D flipflop	Clock to Q delay(low - high)	Clock to Q delay(high-low)	Average clock to Q delay	Average power consumption (µw)	Power delay product(aJ)
Nand based	----	----	----	3.76	----
Muxs based	----	-----	-----	3.01	---
5Transistors	18ps	16ps	17ps	5.59	95.03
6Transistors	60ps	59ps	59.5ps	1.86	110.67
TG based	20ps	27ps	23.5ps	9.355	215.165
8 Transistors	19ps	16ps	17.5ps	6.27	109.725
10 Transistors	27ps	27ps	27ps	24.28	648.16
14 Transistors	61ps	42ps	51.5ps	25.53	284.795

From the above table we can conclude that when we design a d flip flop with 5 transistors we will get less average delay and when we design d flipflop with 6 number of transistors we will get less power

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