WWW.IJRPR.COM

International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

AN EFFECTIVE DESIGN OF SRAM CELL USING VARIOUS TRANSISTORS

Srikanth J, Vinay kumar G, Vamsi krishna G

Department of Electronics and Communication Engineering, Madanapalle Institute of Technology & Science, Madanapalle, Andhra Pradesh, India

ABSTRACT

Presently, huge advancements are being witnessed in the electronics sector like AR, AI, driverless cars, smart homes, portable devices like mobile phones, etc. that requires the improvement of memory technology for efficient working. Memory plays a major role in the present scenario of improvements and growth. Out of different forms of memory devices, the most popular and presently used type of form is the semiconductor MOS memory, specifically SRAM (Static Random-Access Memory) that plays a very important role in the microprocessor domain as it covers a large portion of the chip. But with the increased scale of integration, leakage power, leakage current, and delay becomes a problem in the designing of an SRAM cell. This paper is a review of SRAM cells that have been proposed in the past for achieving improvement in SRAM cell parameters like power consumption, delay, leakage current, read and write stability, better cell operations, etc.

Keywords*: Cell area, low power, MOS, SRAM Cell, SRAM ,stability.*

1. INTRODUCTION

The technique of building an integrated circuit (IC) by merging thousands of transistors into a single chip is known as very-scale-scale integration (VLSI). With the advancement of semiconductor and communication technologies in the 1970s, VLSI was born. A VLSI device is used as the microprocessor's is a type of integrated circuit that has several devices on a single chip. The word, like many other scale integration classifications based on the number of gates or transistors per IC, dates back to the 1970s..The advancements in large-scale integration technologies are principally responsible for the electronics industry's extraordinary growth. The number of options for ICs in control applications, telecommunications, high-performance computing, and consumer electronics as a whole continues to grow with the emergence of VLSI designs.

Due to VLSI technology, current technologies such as smartphones and cellular communications provide unparalleled mobility, processing capacity, and application access. As demand continues to rise, the projection for this trend implies a quick growth.Prior to the development of VLSI technology, most ICs could only execute a limited number of jobs. CPU, ROM, RAM, and other sensible glue may be found in the electronic circuit. VLSI enables IC designers to combine all of these features into a single chip

Power utilization is a significant thought in the plan of Very Large-Scale Integration (VLSI) circuits, which utilize the Complementary Metal Oxide Semiconductor (CMOS) as the major innovation. The ongoing spotlight on low power isn't only because of the new ascent in portable application needs. Power utilization has forever been a significant issue, even before the portable age. Numerous analysts have introduced numerous strategies to defeat the power dispersal issue, going from the gadget level to the compositional level and then some. In any case, since there is no uniform answer for wipe out tradeoffs between power, dormancy, and region, fashioners should pick OK ways to deal with meet application and item prerequisites.

2. STATIC RANDOM ACCESS MEMORY

2.1. INTRODUCTION TO SRAM:

In this chapter, we explain important notation and VLSI background used in this dissertation. First, we introduce subthreshold leakage power consumption on which our research focuses. Next, we explain the background underlying a particular leakage power model able to explain the stack effect, which is an important leakage reduction factor in our research. We then explain the body-bias effect. Furthermore, we explain subthreshold leakage power consumption of a conventional 6 Transistor (6-T) SRAM cell.

2.2. LEAKAGE POWER

In this section, we explain notation and background relevant to leakage power consumption.

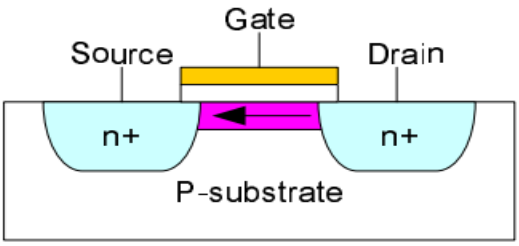

Fig-2.2 (a): Sub threshold leakage of an Fet

Although dynamic power is dominant for technologies at 0.18µ and above, leakage (static) power consumption becomes another dominant factor for 0.13µ and below. One of the main contributors to static power consumption in CMOS is subthreshold leakage current shown in Figure 1, i.e., the drain to source current when the gate voltage is smaller than the transistor threshold voltage. Since subthreshold current increases exponentially as the threshold voltage decreases, nanoscale technologies with scaled down threshold voltage

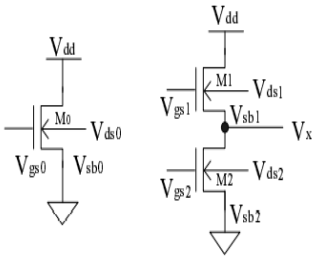

Fig-2.2(b): Single transistor and stacked transistor

Sub threshold leakage can be reduced by stacking transistors, i.e., taking advantage of the so-called "stack effect". The stack effect occurs when two or more stacked transistors are turned off together; the result is reduced leakage power consumption. Let us explain an important stack effect leakage reduction model.

2.3 SRAM cell leakage path

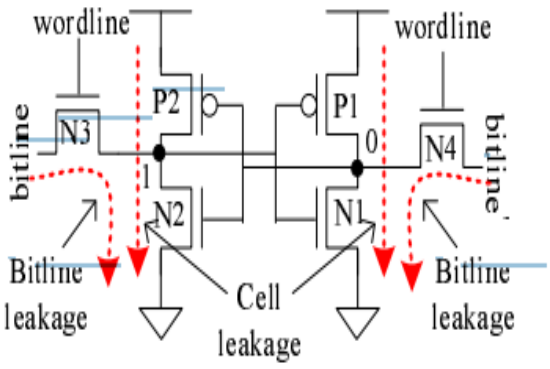

Fig 2.3: SRAM cell leakage paths

In this section, we explain the major subthreshold leakage components in a 6-T SRAM cell. The subthreshold leakage current in an SRAM cell is typically categorized into two kinds as shown in Figure 3: (i) cell leakage current that flows from Vdd to Gnd internal 14 to the cell and (ii) bit line leakage current that flows from bitline (or bitl ine') to Gnd. Although an SRAM cell has two bit line leakage paths, the bitline leakage current and

bitline' leakage current differs according to the value stored in the SRAM bit. If an SRAM cell holds '1' as shown in Figure 3, the bitline leakage current passing through N3 and N2 is effectively suppressed due to two reasons.

First, after precharging bitline and bitline' both to '1,' the source voltage and the drain voltage of N3 are the same, and thus potentially no current flows through N3. Second, two stacked and turned off transistors (N2 and N3) induce the stack effect. Meanwhile, for this case where the SRAM bit holds value '1,' a large bitline' leakage current flows passing through N4 and N1. If, on the other hand, the SRAM cell holds '0,' a large bitline leakage current flows while bitline' leakage current is suppressed. Our results in Section indicates that bitline leakage accounts for approximately 35% of SRAM cell leakage power consumption. In this section, Section 3.2, we explain the two major types of leakage paths in an SRAM cell (cell leakage and bitline leakage). In next section, we explain tradeoffs between switching power and delay

3. DIFFERENT SRAM CELL DESIGNS

3.1 CONVENTIONAL 6T SRAM CELL

The conventional SRAM cell made of 6 MOSFETs is the most basic SRAM cell. Fig 3.1 shows the conventional 6T SRAM cell schematic. This cell consists of two access transistors and two cross-coupled inverters with a common read and write port. Asserting a high value to WL enables the access transistors for both read and writes operations. For hold operation, WL is set to a low value.

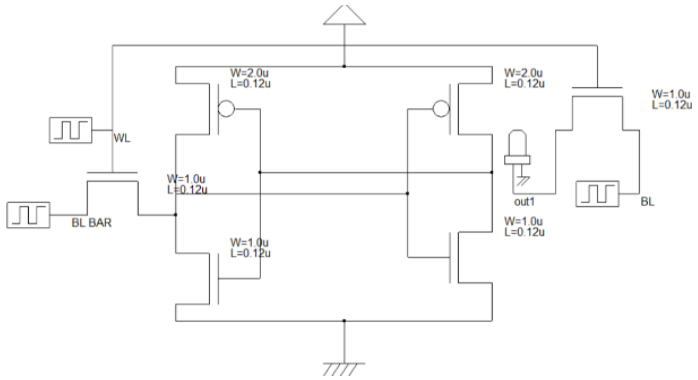

Fig 3.1: Schematic diagram of 6T SRAM cell

3.2 5T SRAM Cell

Fig 3.2 shows another SRAM cell designed to achieve area reduction and is obtained by removing one access transistor from the 6T SRAM cell giving a 5-transistor cell. This 5T cell has a single bit-line 'BL' [4].

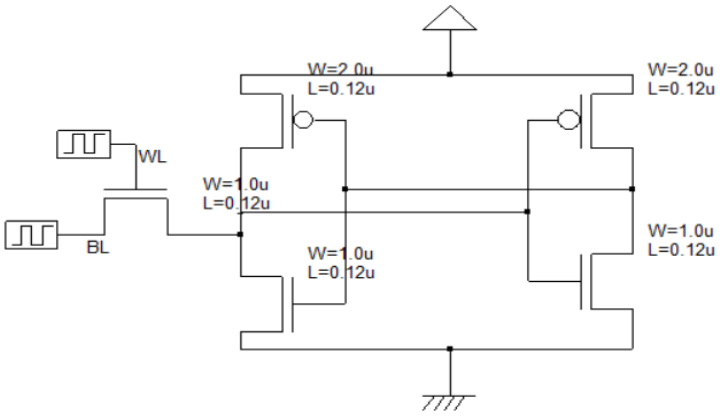

Fig-3.2: Schematic diagram of 5-T SRAM cell

3.3 7T SRAM Cell

Fig 3.3 shows a 7T SRAM cell [5] that has an additional NMOS transistor N5 as compared to the conventional 6T SRAM cell. The write operation in this cell depends on removing the feedback connection between the two inverter pairs before the write operation, and the transistor N5 serves the purpose of feedback connection and disconnection. For writing in this cell, N5 is turned OFF. During the read operation, the cell behaves like a conventional 6T SRAM cell with N5 in ON state.

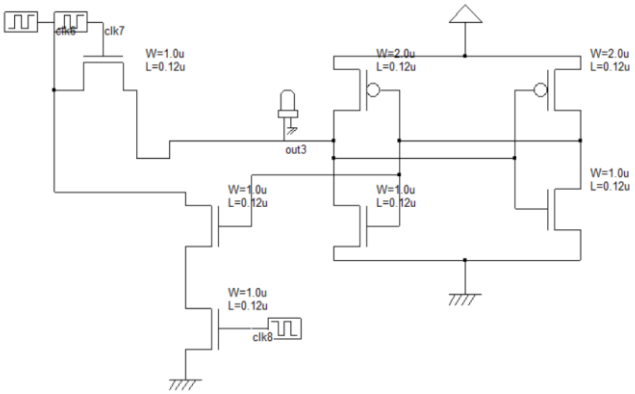

Fig-3.3: Schematic diagram of 7-T SRAM cell

3.4:8T SRAM Cell

Figure 3.4 shows the circuit diagram of the 8T SRAM cell. This cell consists of a separate circuit consisting of two additional NMOS transistors for the read operation. This read circuit provides a read mechanism that does not disturb the internal nodes of the cell and thus improves the stability of the cell. This cell has separate read and write word lines and accommodates dual-port operation with separate read and write bit lines [6].

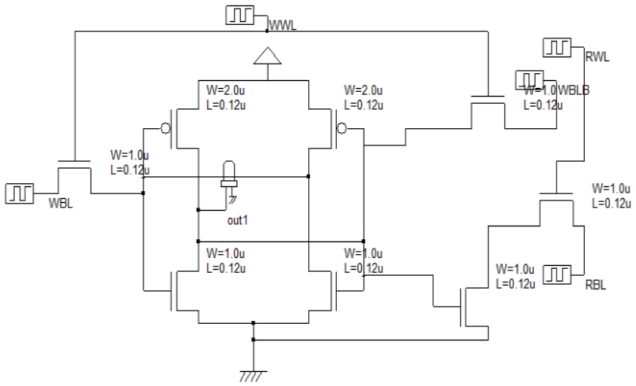

Fig-3.4: Schematic diagram of 8-T SRAM cell

3.5 9T SRAM Cell

Figure 3.5 shows the schematic of a nine transistor SRAM cell. This cell is designed with the aim of improving stability and reducing power consumption. It can be viewed as a combination of two sub-circuits – the upper and lower sub-circuits. The upper sub-circuit is responsible for data storage, and the lower sub-circuit contains transistors for bit line access and read access. This cell uses a separate read signal that controls the read access transistor N7 [7].

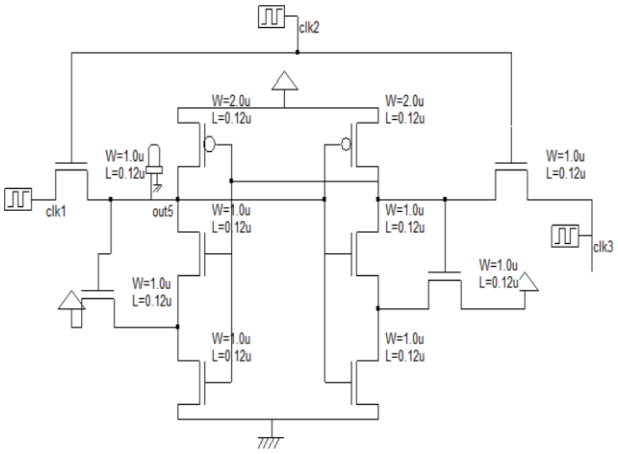

Fig-3.5: Schematic diagram of 9-T SRAM cell

3.6 10T SRAM

Cell Figure 3.6 shows the differential-ended PPN10T SRAM cell that consists of ten transistors and uses a different version of the read path to achieve a reduction in the read access path's leakage current. As compared to the 6T cell, this cell has an additional signal VGND that is attached to GND only during read operation else it is connected to VDD. This cell uses PPN inverters. This design has two different storage nodes- the pseudo storage nodes (pQ and pQb) and the actual storage nodes (Q and Qb). These pseudo storage nodes present between the two series-connected PMOS transistors are responsible for providing an isolation mechanism between the bit line pair and the actual storage nodes during the read operation [8].

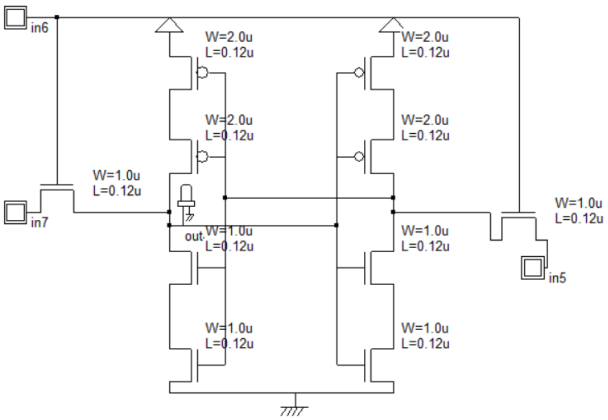

Fig-3.6: Schematic diagram of 10-T SRAM cell

3.7: 11T SRAM Cell

ST11T is another ST based cell consisting of 11 transistors, and it has a separate read decouple circuit with single-ended cell operation. Figure 11 shows the ST11T SRAM cell. This cell consists of cross-coupled ST inverters, a read path comprised of two transistors, and a write-access transistor. The internal storage nodes Q and QB are responsible for controlling feedback transistors of Schmitt Trigger, MNFL, and MNFR, respectively, with their drains attached with a control signal Wordline_bar (WLB) (complement of write enable signal) [13].

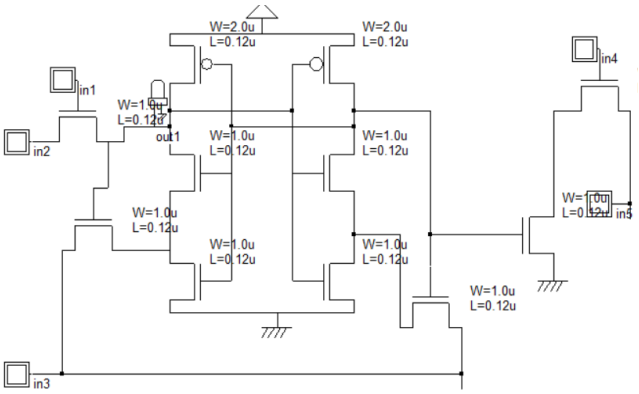

Fig-3.7: Schematic diagram of 11-T SRAM cell.

4. RESULTS

The proposed design is successfully implemented in MICROWIND tool.

4.1. SIMULATION LAYOUT AND WAVEFORM

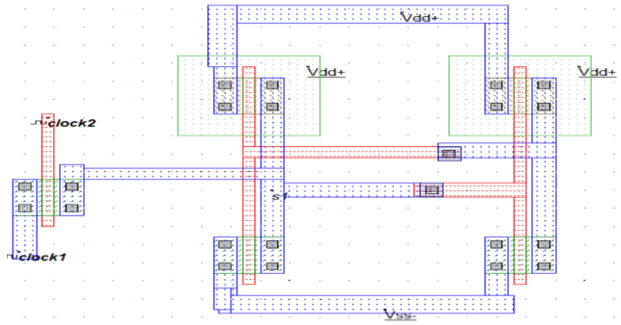

Fig-4.1 (a): Analog layout design of 5-T SRAM cell.

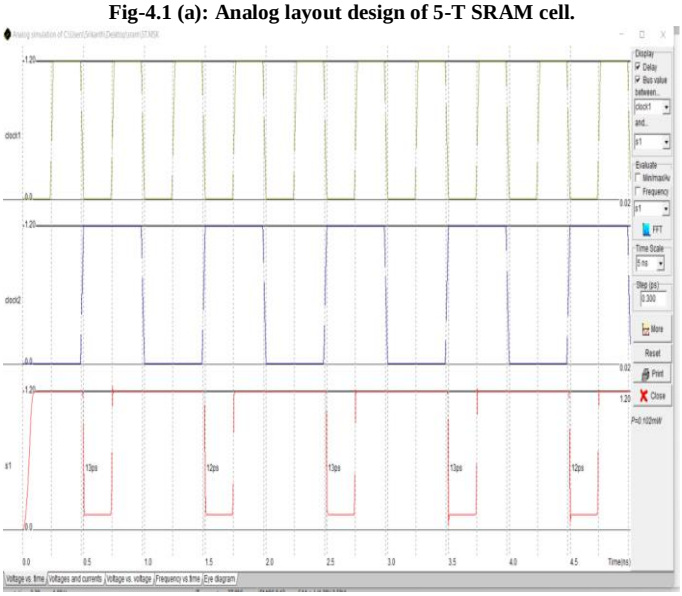

Fig-4.2 (b): Output Waveform of 5-Transistor SRAM cell.

ADVANTAGES: This cell has a significant area and power reduction as compared to 6T cell. DISADVANTAGES: This cell suffers from difficulty in write '1' operation and relies on a particular cell sizing strategy to ensure correct write operation.

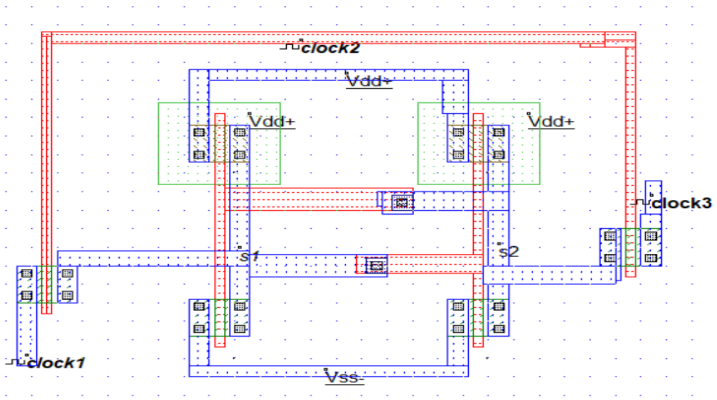

Fig-4.2 (c): Analog layout diagram of 6-T SRAM cell

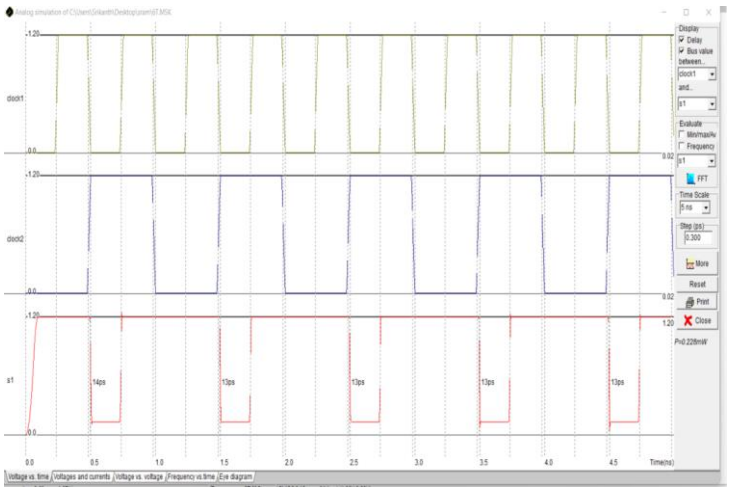

Fig-4.2 (d): Output Wave form of 6-T SRAM cell

ADVANTAGES: This cell is simple in design and consumes less area and thus can be used to design high-density memory chips.

DISADVANTAGES: This cell fails to maintain its stability at smaller-scaled technology. It suffers from read and write instability, has high power consumption, and increased access time when voltage scaling is done

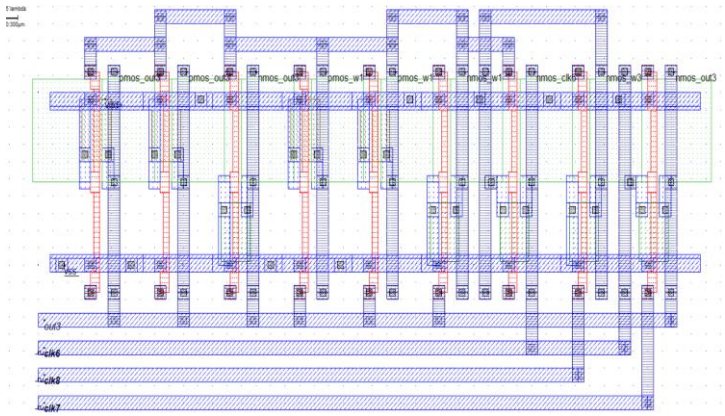

Fig-4.2 (e): Analog layout of 7-T SRAM cell.

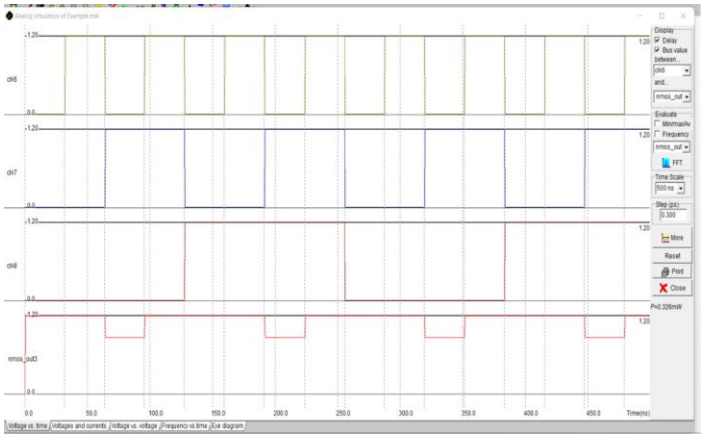

Fig-4.2 (f): Output Wave form of 7-T SRAM cell.

ADVANTAGES: This cell has better cell operation and lower write power dissipation as compared to the conventional SRAM cell.

DISADVANTAGES: Due to the additional transistor, the cell area is 12.25% more than the 6T cell

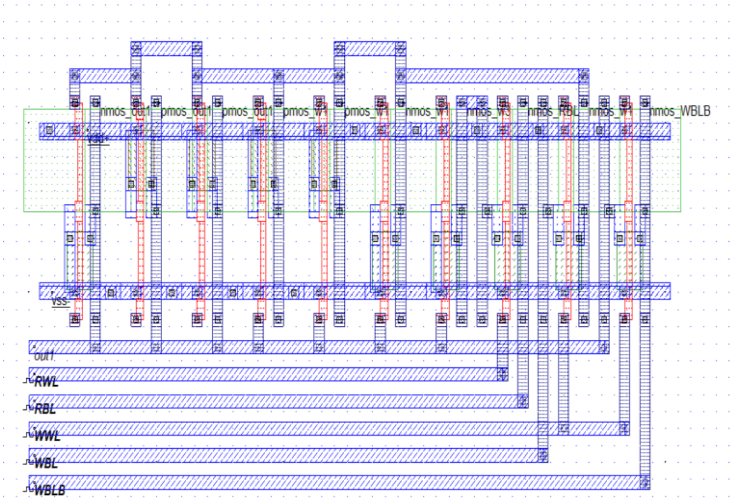

Fig-4.2 (g): Analog layout Design Of 8-T SRAM cell.

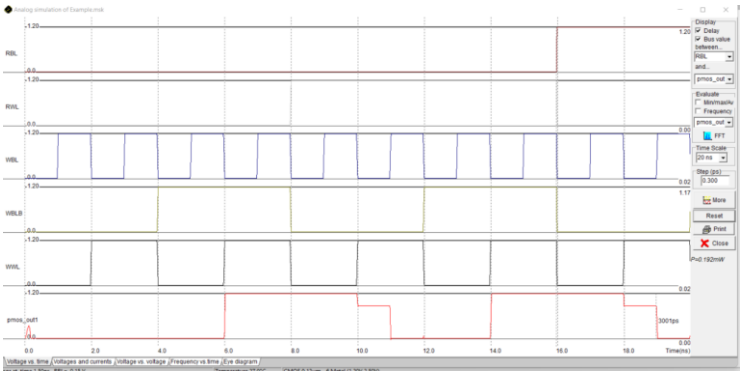

Fig-4.2 (h): Output Wave form Of 8-T SRAM cell.

ADVANTAGES: The 8T cell has better stability, higher SNM, and lower power consumption. This cell also allows for continued scaling compared to 6T cell that suffers from various issues when scaled down.

DISADVANTAGES: The 8T cell consumes 30% more on the chip as compared to the conventional 6T cell.

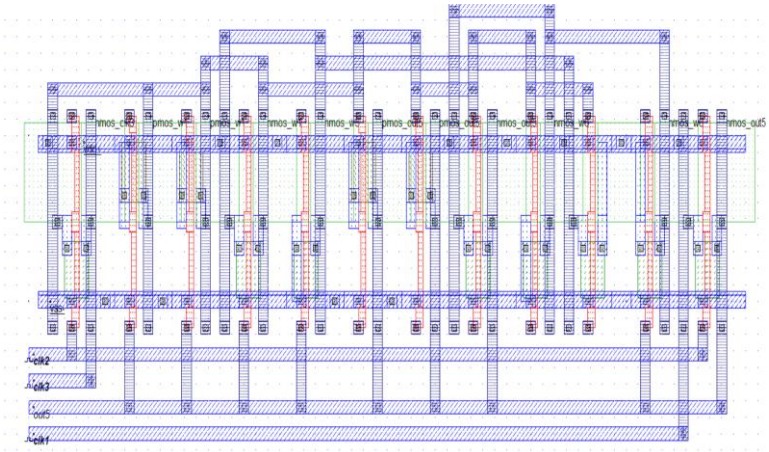

Fig-4.2 (i): Analog layout of 9-T SRAM cell.

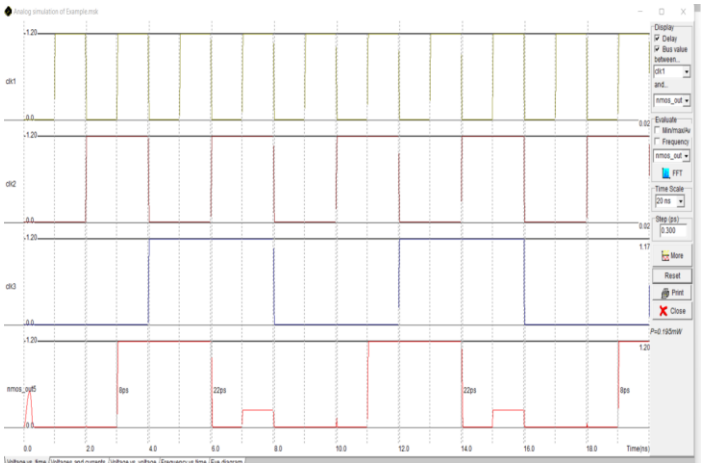

Fig-4.2 (j): Output wave form of 9-T SRAM cell.

ADVANTAGES: This cell has 7.7% less leakage power and also has better read stability as compared to the typical 6T SRAM cell. DISADVANTAGES: The area consumed by this cell is 37.8% more than the 6T cell, and the presence of three stacked transistors in the read circuit increases the read access time.

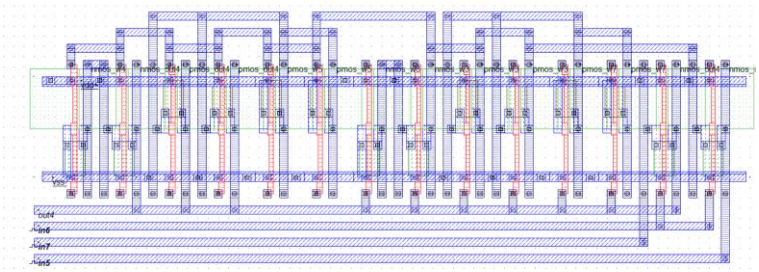

Fig-4.2 (k): Analog layout of 10-T transistor SRAM cell

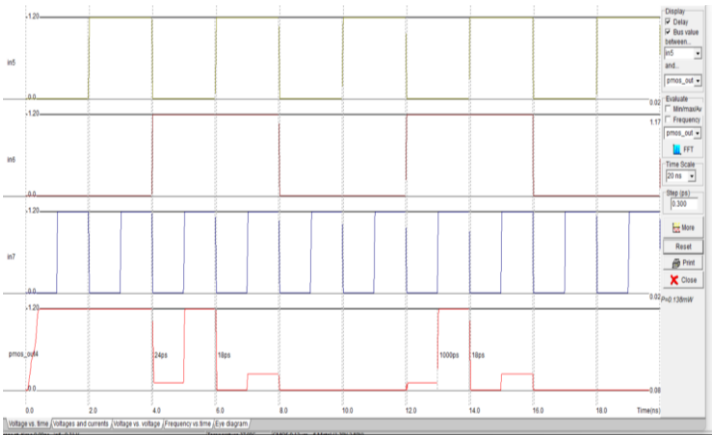

Fig-4.2 (l): Output wave form of 10-T SRAM cell.

ADVANTAGES: This design has low power dissipation as compared to 6T cell and also works better at low sub-threshold voltage. Moreover, the separate read path in this cell increases the read stability of the cell. DISADVANTAGES: Since the number of transistors is more as compared to the conventional SRAM cell so the area covered by the cell is more and the presence of two series-connected transistor s in its write path, the write stability is degraded

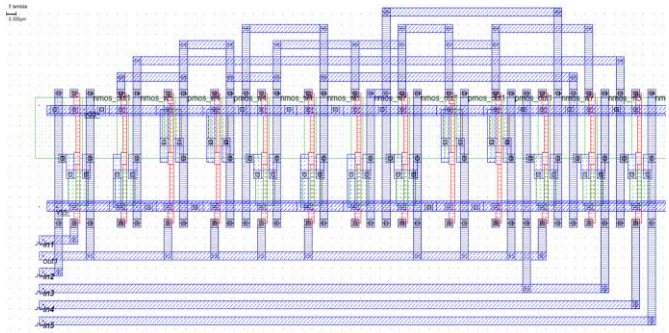

Fig-4.2 (j): Analog layout of 11-T SRAM cell.

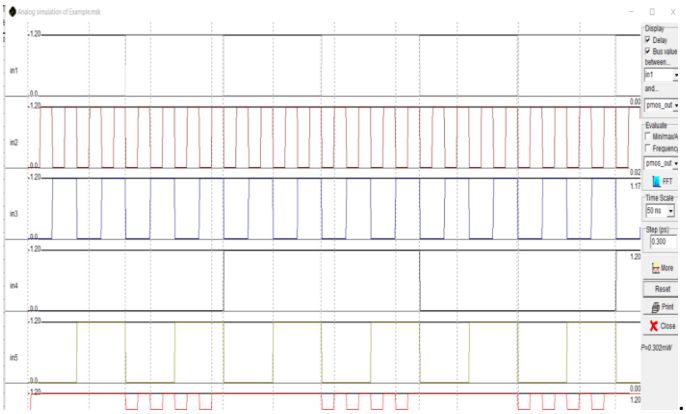

Fig-4.2 (k): Output wave form of 11-T SRAM cell.

ADVANTAGES: Due to the feedback mechanism, this cell has increased data holding capacity. Also, this cell has reduced power and leakage current and improved read stability.

DISADVANTAGES: This cell has a failure to write '1' operation. Being a single-ended cell, it suffers from write access time and require write assist circuits to minimize write '1' access time.

5. CONCLUSION

Besides the different SRAM cells reviewed here, various other SRAM cells using transistors 7, 8, 9, 10, and 11 are also designed to meet different design goals according to the device's need. In the future, analysis of existing designs is possible by applying various techniques for power reduction, voltage scaling and stability improvement. Also, since today's need is the design of low-power devices, optimization of designs can be done to reduce power consumption. Device space is also an important parameter today, allowing the design of new SRAM cells with low power consumption and fewer transistors.

REFERENCES

[1] N. K. Khokhara and B. H. Nagpapa. Comparative Analysis of 1 bit SRAM using Different SRAM cells in 45nm CMOS Technology, International Journal of Innovative Research in Computer and Communication Engineering, Vol. 5, no. 1, pp. 251-258, January 2017.

[2] S. Rehlan, A. Yadav, B. Goel and J. Raheja. comparative analysis of low power 4T SRAM cell, International Journal of Technical Research (IJTR), Vol. 3, no. 1, Mar-Apr 2014.

[3] Integrated Circuit Engineering Corporation, SRAM Technology, pp. 8.10-8.11.

[4] Carlson, S. Anderson, S. Natarajan and A. Alvandpour. A High Density, Low Leakage, 5T SRAM for Embedded Caches, ESSCIRC, 2004.

[5] R. E. Aly, Md I. Faisal, and M. A. Bayoumi. Novel 7T SRAM cell for low power cache design, in Proc. IEEE SOC Conf., 2005, pp. 171–174.

[6] L. Chang et al. Stable SRAM cell design for the 32nm node and beyond, Proceedings of the IEEE Symposium on VLSI Technology, June 2005, pp. 128-129.

[7] Z. Liu and V. Kursun. Characterization of a Novel Nine-Transistor SRAM Cell, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, no. 4, pp. 488-492, April 2008.

[8] C. H. Lo and S. Y. Huang. PPN based 10T SRAM cell for low-leakage and resilient subthreshold operation, IEEE J. Solid State Circuits, Vol. 46, no. 3, pp. 695-704, 2011.

[9] J. P. Kulkarni, K. Kim and K. Roy. A 160 mV robust Schmitt trigger based subthreshold SRAM, IEEE J. Solid State Circuits, Vol. 42, no. 10, pp. 2303-2313, 2007.

[10] J. P. Kulkarni and K. Roy. Ultralow-voltage process-variation-tolerant Schmitt-trigger-based Aparna et al., International Journal of Emerging Trends in Engineering Research, 9(3), March 2021, 303 – 309 309 SRAM design, IEEE Trans. Very Large Scale Integration (VLSI) Syst., Vol. 20, no. 2, pp. 319-332, 2016.

[11] Islam and M. Hasan. Leakage Characterization of 10T SRAM Cell, IEEE Trans. On Electron Devices, Vol. 59, no. 3, March 2017.

[12] P. Singh and S. K. Vishvakarma. Ultra-Low Power, Process-Tolerant 10T (PT10T) SRAM with Improved Read/Write Ability for Internet of Things (IoT) Applications, Journal of Low Power Electronics and Applications, Vol. 7, no. 3, p. 24, September 2019.