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# Design a Bridge for Advanced High Performance Bus to Advanced Pheripheral Bus

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**ABSTRACT:**

The advanced microcontroller bus architecture bus protocol is used to build high performance SOC design .This achieves communication through the connection of different functional blocks .By using multiple controller and pheriperials,it male possible to develop multiprocessor unit.It provides reusability of IP of different buses of AMBA,which can reduce the communication gap between high performance buses and low speed buses.To perform high speed pipelined data transfers ,AMBA based embedded system becomes a demanding hypothesis analytical wise,by using different bus signals supported by AMBA.To synthesize as well as simulate the composite annexation which connects advance high performance bus and advanced low performance bus which is know as AHP2APB bridge in addition to no data loss during transfer is the main target of this work.Implementation of bridge module is designed in Verilog HDL and functional and timing simulaton of bridge module are done on a platform of Xilinx.

**Keywords:**Bus Architecture, Handshaking Signal, Systemonchip.

## 1. Introduction

AMBA's AHB is a bus interference suitable for high performance synthesizable designs. AHB supports the efficient content of processors ,off-chip external memory and on-chip memories interferences with low- power pheripheral microcell functions

APB and implements the features required for high clock frequency and high performance system including pipeline data operation ,split transaction ,burst transfers ,single cycle bus master handover ,single clock edge operation.

APB is one of the components of the AMBA bus architecture .APB is low performance and low consumption band width .APB can be used in conjuction with either version of the system bus. APB used to connect the peripherial like keyboard,timer,UART.

Function for apb is low power consumption ,small bandwidth ,reduce interference complexity, pipelined operation is not supported by APB so it makes communication with ASB or a AHB. Here we used Verilog HDL for designing the RTL code . synthesis and simulation is done using Xilinx and Modelsim[3].

### 2.AMBAbasedmicrocontroller

To sustain external memory bandwidth,dynamic memory access (DMA),on-chip memory resides on chip AMBA based microcontroller provides a high performance bus (AHB). This bus helps in providing a bandwidth interference between those blocks where majority of data transfer is involved. Also provides the interface between the high bandwidth bus elements and low bandwidth bus elements.
APB, Low bandwidth bus is the where all low performance pheriperials are located .A sequence class contains a user defined task body that is called when the sequence is started. The task body does the work of the sequence .A sequence that directly generates transactions must always execute on a sequencer.

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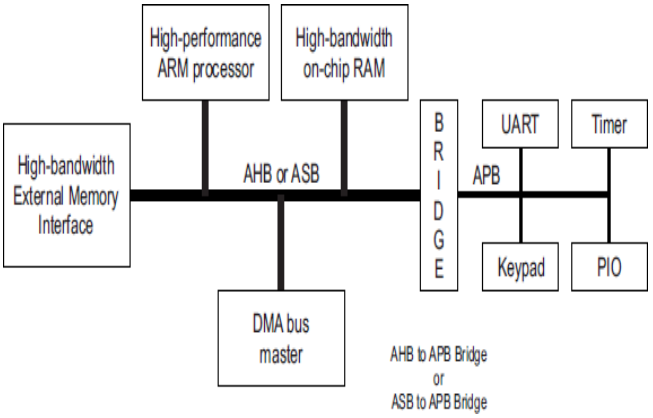


**Fig.AMBA block diagram3.**

**3. AHB2APBBridge**

TheAHB2APBis an AHB slave,providing an interference between the high speed AHB and low power APB .read and write transfer s on the AHB are converted into equivalent transfer on the APB . As the APB is not pipelined , then wait states are added during transfer to and from the APB when the AHB is required to wait for the APB. The AHB2APB interfaces AHB and APB . It buffers address, controls and data from the AHB, drives theAPB peripherals and return data along with response signal to the AHB.Supports for the following

- APBcompliantslavesandperipherals.
- Peripheralswhichrequireadditionalwaitstates

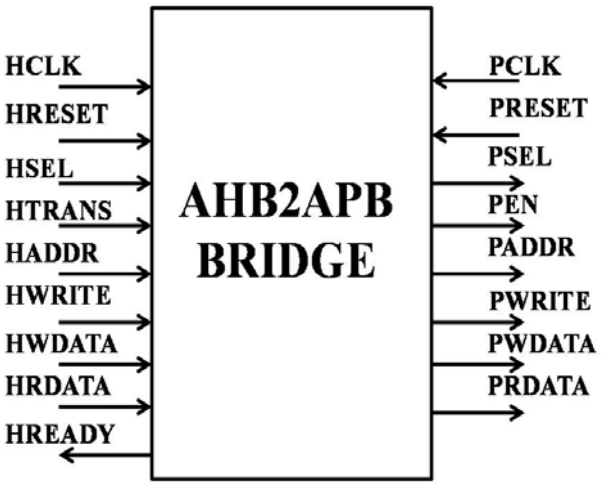


Fig. block diagram of AHB to APB bridge

**4.Implementation& verification plan**

The verification plan address to the design item to be verified and here in this topic it is based on system Verilog language constructs and constrained random driven coverage verification methodology. We will be verifying the signals coming from sequence item and checking the corresponding

1. Feature Extraction: To Guarantee exact design functionality all the features are needed to verify as per the specification, so all the features should be extracted to ensure thefunctionality
2. Stimulus Generation Plan: Using the constrained randomization concept here we can generate all the possible exhaustive test cases, and stimulus can beapplied randomly to the design as the specification.

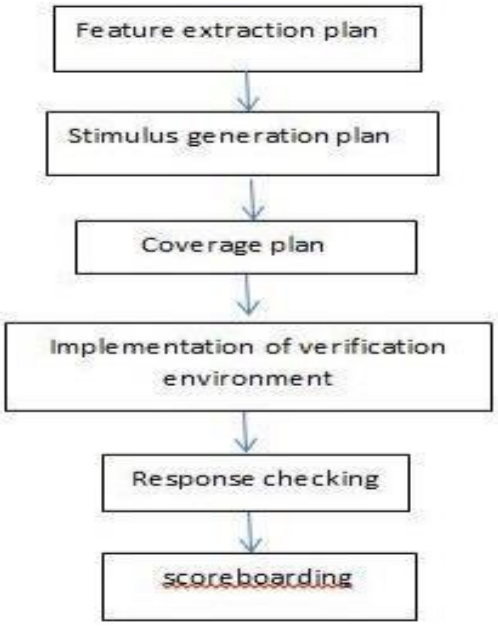


**Fig.. verification flow of implementation model**

3. Coverage Plan: coverage plan includes both the code coverage and functional coverage. So what all are the functionalities to verified will be planned and coverage report for that can be obtained using cover groups and assertions. Code coverage aims at 100 percent which includes branch, block, expressional, FSM, and arc coverages.

4.Implementing the Verification Environment: implementing the verification environment starts with the architecture build. This architecture enables all the signals to be verified as per the protocol and also allows reusability. All the test vectors are applied to designedare generated herein the verification environment and stimulus is applied the design and the correspondingoutput is evaluated to confirm functionality

**6.1 AHB Waveformss**

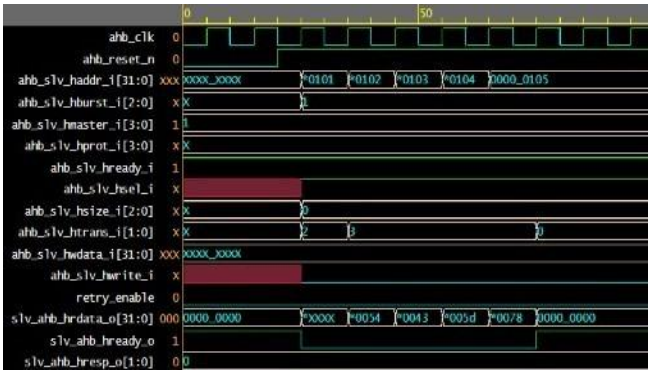


Fig.AHB Waveforms

6.2APB Waveforms s

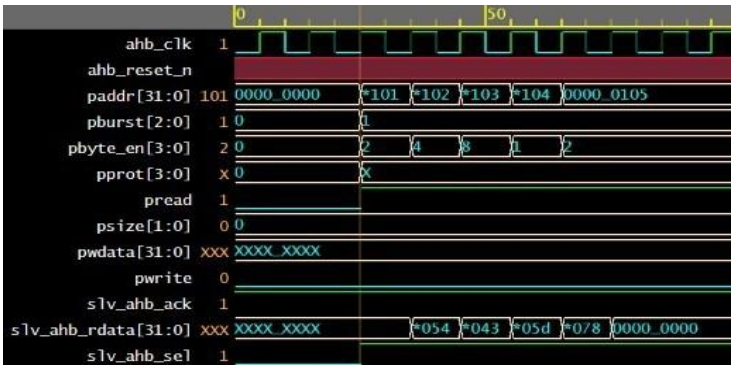


fig..APB Waveforms

**6.3** AHB and APB Waveforms

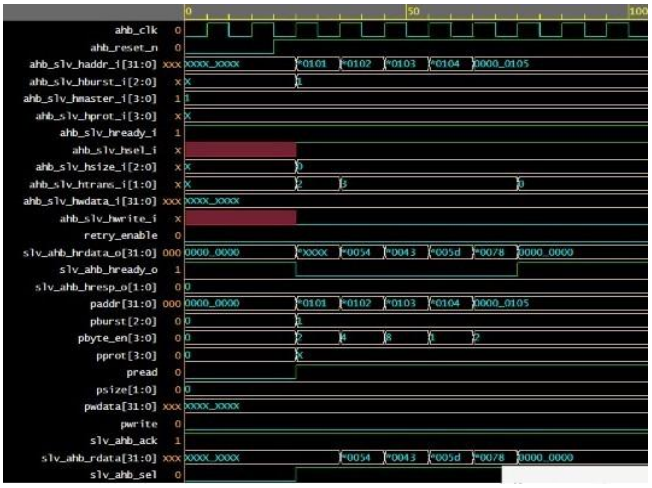


**Fig 6.3 AHB AND APB Waveforms**

## 7. ADVANTAGES OF UVM Compared to other Verification Methodologies

1. Modularity and Reusability – The verification methodology is developed as modular components (Test, Environment, Agent, Driver, Monitor, Scoreboard etc) this enables reusing components across unit level to multi-unit or chip level verification as well as across projects.

2. Separating Tests from Testbenches – Tests are not in the testbench hierarchy, test are kept inside sequencers and used inside the testbench this allows reuse of testcases across different phases and units of project.

3. Simulator independent – There is no dependency of class library and methodology on simulator almost all simulatorssupports methodologyso designed testbench is not specific to one simulator, it can be used across all simulators.

4. In this methodology object sequence has good control on stimulus generation. There are several ways in which sequences can be developed which include randomization, layered sequences, virtual sequences etc which provide good control and rich stimulus generation capability.

5. Objects can be configured using the config mechanism. Test components can be easily configured using the configuration mechanism based on which verification environment uses it.

6. Factory mechanisms in UVM help in modifying a component. Factory mechanism allows for overriding different tests or environments without changing the original code.

## 8.APPLICATIONS (UVM)

s

1. Designing VIP"S.
2. Functional exhaustive verification of a design.
3. To design a reusable and configurable testbench environment.
4. To design an interoperable testbench.

## 9. CONCLUSION

Using UNIVERSAL VERIFICATION METHODOLOGY, AMBA AHB2APB Bridge functionality was verified and a functional coverage report is obtained. Using UVM for designing a verification environment makes the verification environment reusable and portable. UVM verifies the design in the most effective wayand the code is reusable with constrained random test cases.

## 10. FUTURE WORK

Automated test-case patterns can be generatedand applied to DUVs using Perl scripts and reports can be extracted. Since UVM Architecture is portable (System C-based golden file) can be included which results in better comparability of obtained results with the reference model. Since UVM architecture is reusable, by making necessary modifications this architecture can be used to verify advanced AMBA protocols

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