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Time to Digital Converter Using CMOS Pulse Shrinking Mechanism

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ABSTRACT

This brief presents anCMOS pulse-shrinking time-to-digital converter (TDC). A pulse generator is used to generate a time-added pulse. A cyclic delay line (DL) composed of a pulse-shrinking DL becomes area efficient and achieves sufficiently wide dynamic range. A time subtractor that eliminates the effect of the offset error enhances accuracy. The proposed TDC is simulated with TSMC 0.180-µm CMOS process. The effective time resolution is approximately 17.00 ps.

Index Terms—CDL (Cyclic Delay Line), CNT (Counter),DL (Delay Line),PG (Pulse Generator),TDC (Time to Digital Converter),TS (Time Subtractor).

Introduction:

Time-to-digital converters (TDCs) are used to convert a time interval into a corresponding digitalcode. TDC has major requirements include a fine resolution, low cost, less power dissipation, and higher linearity. Thus, to fulfilthese requirements TDCs implemented using the CMOS process. High performance CMOS TDCs are an essential component in numerous precise instrumentation systems, automated test equipment, and timing circuitry. They are also used in industrialchips.

There are some popular methodologies, such as time amplification, time(phase) interpolation,local passive interpolation (LPI) TDC, inverter based TDC, and the Vernier principle have beenreported to achieve high resolution for the TDCs. But pulse-shrinking approach without a complex circuit and the operation was presented to easily achieve a sub gate resolution.Based on the pulse shrinking TDCsisdesigned. This convertercan perform time-to-digital conversions to increase the circuit value and to save the circuit cost. To accelerate the design procedure, cost of circuit and reduce the effort, the digital CMOS design was applied. The of this TDC brief is organized as follows. Detailed literature survey is given in Section II. The circuit description is detailed in Section III.

Literature Survey:

This study presents the first CMOS single converter. The proposed circuit has fully digital CMOS logic gates to eliminate time-consuming full-custom CMOS design [1].This study represents Time to Digital Converter using conventional i.e.,multistage pulse shrinking mechanism [2]. In this study they use pulse shrinking based delay element for the conversion of time pulses into digital pulses [3].This paper shows using pulse mixing circuitry for the pulse shrinking TDC to overcome the non-linearities in the conventional pulse shrinking circuit [4].In this study the dynamic range of Time to Digital converter using pulse shrinking is improved using pulse mixing scheme [5]. This paper showsa simple offset error cancellation circuitry for the pulse shrinking TDC to eliminate the undesired offset error to widen the DR and to improve the accuracy without increasing the circuit complexity considerable[6].

Circuit Description:

Fig. 1 displays the simplified structure of the proposed TDC, which comprises a pulse generator (PG), a cyclic delay line (CDL) and pulse-shrinking time measurement, a time subtractor (TS), and a counter (CNT).

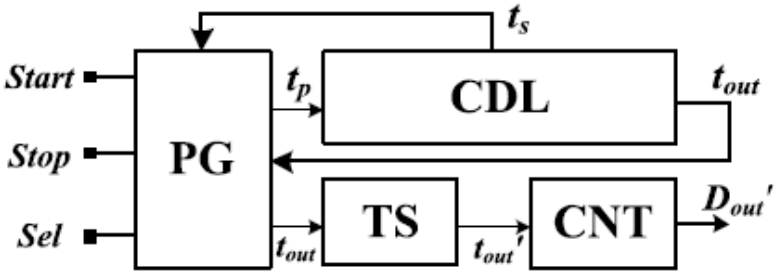

Figure 1:Proposed TDC

3.1Pulse Generator

The circuit and timing diagram of the PG are shown in Fig. 2. In this, PGgenerates a time-added pulse tp, T.For TDC,the main function is the PG can be regarded as the time adder to cancel the effect of the offset error. The added time *ta* is the summed delay of a delay line and a multiplexer (MUX1). tp, T is equal to *t*in + *t*a and enters the CDL for time measurement conversion. By triggering the D-type flip-flop (DFF), the lower path of the two MUXs is selected to cause MUX1 and MUX2 to pass "0" and "*t*out," respectively. With cyclic shrinkage of the pulse in the CDL, *t*out is transmitted through MUX2 to the TS. When necessary, an extra delay chain can be added in the *t*a path to ensure that *t*a is wider than *t*err for the offset-error cancellation.

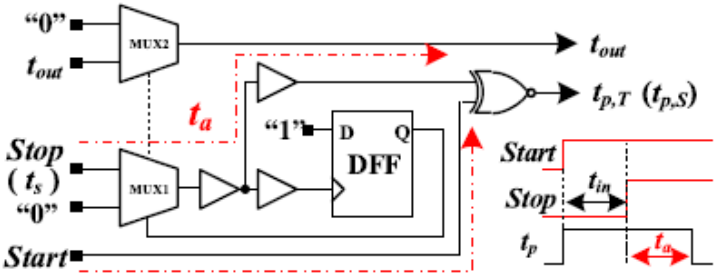

Figure 2: Pulse Generator

3.2Cyclic Delay Line:

The circuit diagram of the control delay line in the proposed TDC is displayed in Fig. 3. It is consisting of a pulse-shrinking delay line (PSDL), where the PSDL is combination of a coupling unit (CU) with two NAND gates and an inverter-based delay line (DL). The coupling unit coupled the measured pulse *tp* into the CDL for cyclic pulse-shrinking time measurement. An area-efficient and wide-DR CDL was achieved by adapting a longer *L*. Since the longer *L* decreased the resolution. Correspondingly, an all-digital pulse-mixing unit was adopted in the PSDL for significant resolution improvement. The delay time *t*d of the inverter-based DL was expressed as follows:

$$\mathrm{Td} = \mathrm{k} \times \mathrm{L}^2 \times \frac{4}{\mu}\mathrm{VDD} \times \frac{\ln(3 - 4\mathrm{Vth}/\mathrm{VDD})}{1 - \mathrm{Vth}/\mathrm{VDD}} = \mathrm{k} \times \mathrm{L}^2 \times \gamma \quad (1)$$

Where*k* is the number of cascading inverter gates, *t*NOT = $L^2 \times \gamma$ is a delay time of one inverter gate, and$\gamma = (4/\mu\, VDD) \times \frac{\ln(3 - 4Vth/VDD)}{(1 - Vth/VDD)}$is a constant factor that is dependent on the CMOS process. A large $k \times L^2$.Value results in a wide *t*d. Therefore, using a longer *L* is an effective method to obtain a sufficient *t*d. A smaller area CDL and the effectively reduced power dissipation can be achieved using fewer stages (smaller *k* value). By simply estimating the area of the inverter gate as $W \times L$, the area of the CDL (*A*CDL*)* can be expressed as,*A*CDL can be derived as follows:

$$\mathrm{ACDL} = \frac{\mathrm{td}}{\mathrm{L}^2 \times \gamma} \times \mathrm{W} \times \mathrm{L} = \left(\frac{\mathrm{td}}{\gamma}\right) \times \left(\frac{\mathrm{W}}{\mathrm{L}}\right) (2)$$

With the same DR (*td)*, the area of the CDL can be reduced by using longer channel length *L*. At the same time, the reduced number of inverter gates required in the CDL decreases the power dissipation.

The all-digital pulse-shrinking theory and the pulse-shrinking (Fig.4.) amount (i.e., time resolution, *R)* in the single-stage mechanism can be expressed as

$$R = \left(m + 1 - \frac{1}{m+1}\right) \times \alpha, \text{ where } \alpha = Ci \times \left(\frac{1}{Kp} - \frac{1}{Kn}\right) \times \varphi \quad (3)$$

Where $\varphi = \left[\left(\frac{2Vth}{VDD\ 2}\right) + \frac{1}{VDD - Vth} \times \ln\frac{1.5VDD\ - 2\ Vth}{0.5\ VDD}\right]$, α is a CMOS process-dependent factor, and *m* is the number of inverter gates to determine the resolution. A lower value of *R* implies that a higher resolution is realized. Further, considering the size (*L* and *W)* of inverter gates, α can be further expressed as follows

$$\alpha = L^2 \times 2\left(\frac{1}{\mu P} - \frac{1}{\mu n}\right) \times \varphi \quad (4)$$

The α value is also related to L^2. The CDL becomes area efficient and wide DR because of the large value of *L*; however, it substantially decreases the resolution.

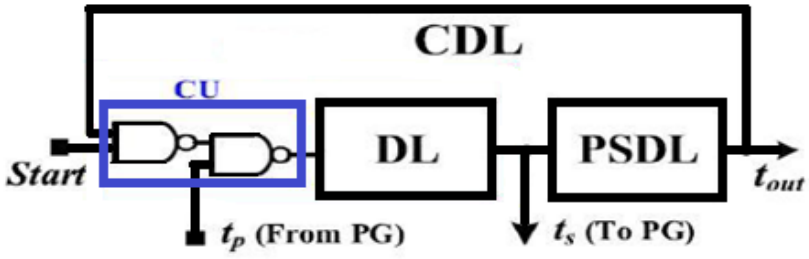

Figure 3: Cyclic Delay Line (CDL)

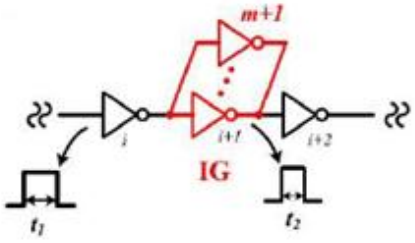

Figure 4 : Pulse Shrinking Unit

3.3Time Subtractor:

The schematic of time subtractor is shown in Fig.5.To avoid the offset-error problem, first, the PG was used for the time addition of *t*a. Then, the TS shown in Fig. 5 was used for the minimization of *t*a. The delay circuit in this TS is consists of buffers to provide delay accordingly. The pulse width of *t*out was detected to determine whether the pulse was wider or narrower than *t*a. When the shrinking width of the *t*out became less than that of *t*a, the end of conversion (EOC) was activated through the AND gate to obtain *ts_out* as the output. Similarly, with the TS, *t*a was subtracted and only the desired *t*in (=*tp*−*t*a*)* was entirely converted for the final digital output. The undesired offset error can be effectively eliminated to enhance accuracy.

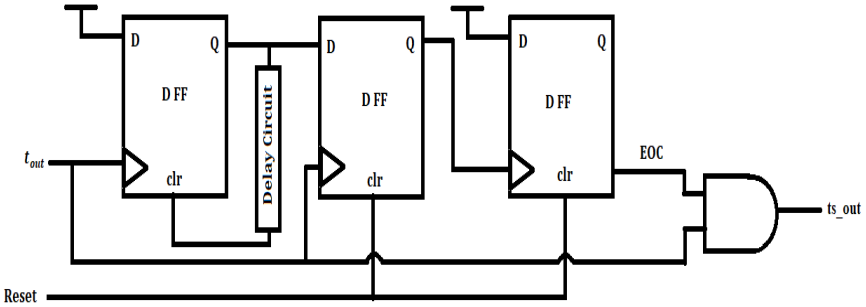

Figure 5 : Time Subtractor

3.4Pulse Generator:

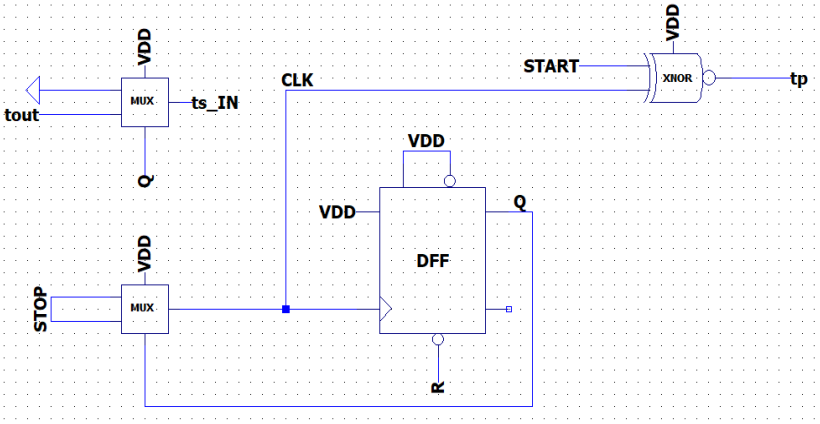

Figure 6 : Pulse Generator Schematic

Pulse generator (in Figure 6) consists of 2 MUX bottom one to use to select CLK for D-FF and one of the inputs to XNOR gate. Upper one is fed with the PSDL output (t_{out}) and gives input to TS(ts_{IN}).D-FFs output is fed to select line input for 2 MUXs according to it corresponding input is selected in MUX. At last, XNOR generates time pulse(tp) when both i.e., START and CLK input is HIGH.

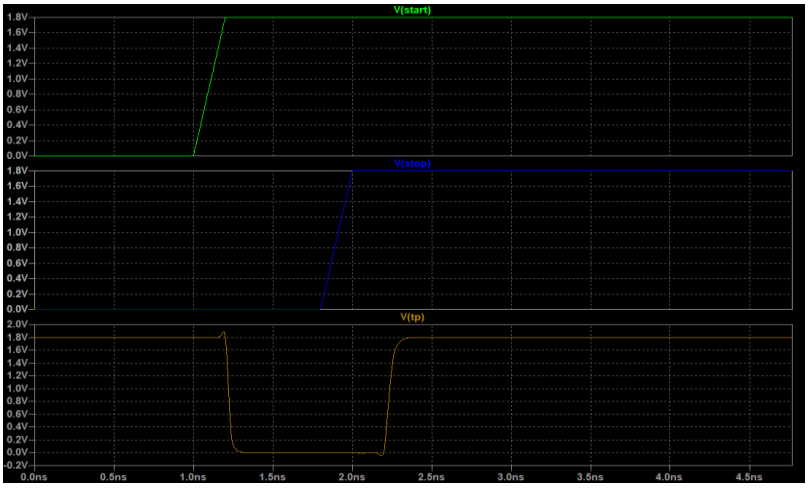

Figure 7 : Pulse Generator Waveforms

Figure 7 shows how the tp is generated in the pulse generator. The difference between start and stop pulsegenerates tp (time pulse).

3.5Cyclic Delay Line:

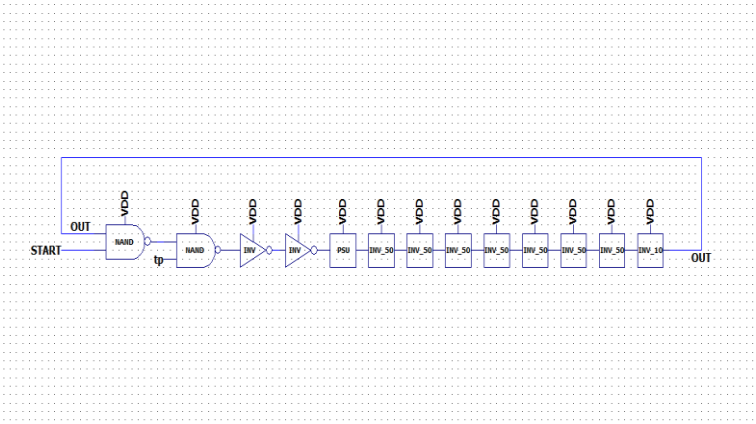

Figure 8 : Cyclic Delay Line Schematic

Above figure 8 shows the schematic of cyclic delay line, which consist of coupling unit, and pulse shrinking unit and n number of inverter, which results in shrinking of pulse and after some time it vanishes completely.

3.6Pulse Shrinking Unit

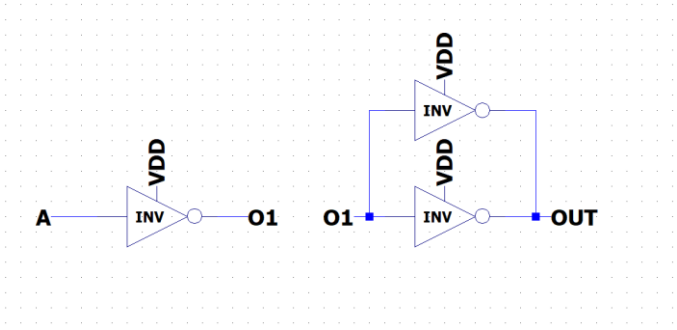

Figure 9 : Schematic of Pulse Shrinking Unit

In the pulse shrinking unit (in figure 9)there are two inverters of different sizing, we made intentionally different according to our requirement i.e., for achieve delay and for pulse reduction purpose. 1st inverter is of normalsize (1:2) and 2nd inverter is of double size(2:4).

3.7 Time Subtractor:

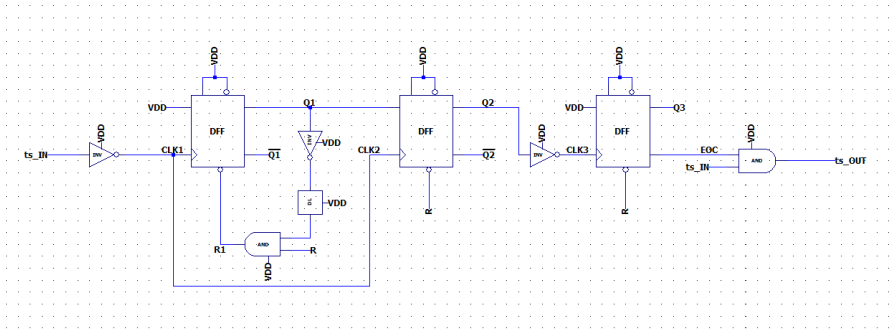

Figure 10:Schematic of Time Subtractor

Time subtractor(Figure 10)minimizes offset error generated in pulse generator. Basically, it consists of 3D-FFs with resetting function and a delay element which includes buffers it provides delay for reducing offset error. At last, there is AND gate which passes the output to counter the EOC in AND gate is goes down to 0 when the input to TS is smaller than offset.

Results:

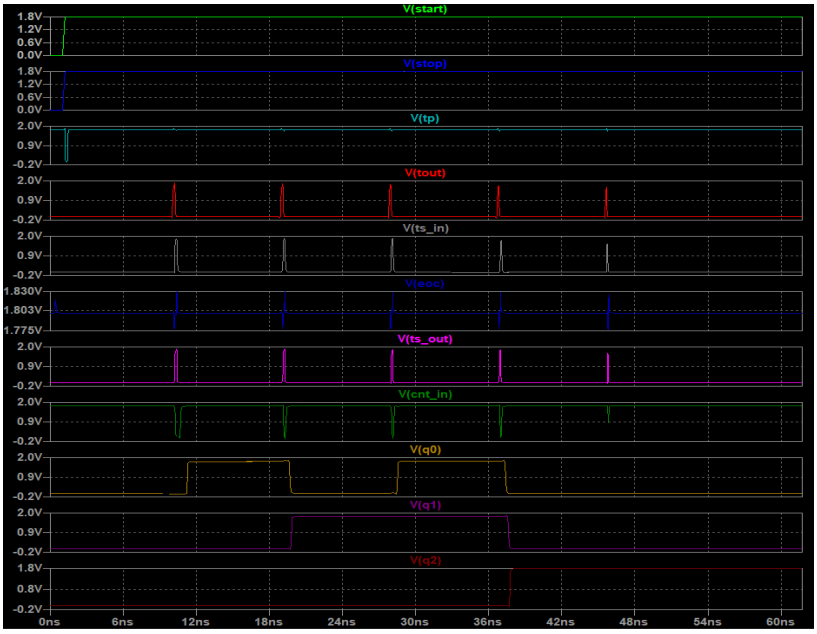

Figure 11 : Output waveforms with zero pulse width with 4 offset counts

When start and stop applied at same time,ideally tp (time pulse) should not be generated, but we get tp having pulse width of 207.32psec as shown in Fig. 11. Then by applying it to DL it gets shrinked and after 5 pulses it vanishes completely. And counter shows $(100)_2 = (4)_{10}$.

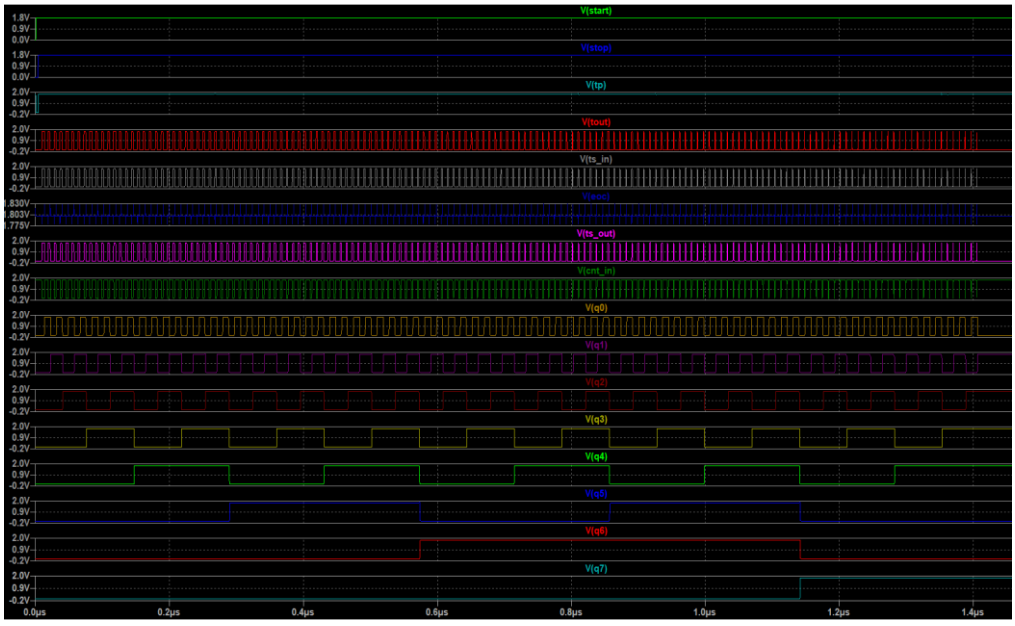

Figure 12 : Output waveforms of3209.5106psec pulse width with 158 counts and including 4 offset counts.

By specifying inputs to START and STOP pulse we generate time pulse tp=3204.5106 psec in PG. The generated pulse is then applied to CDL for pulse shrinking it shrinks by average 17psec each and after 158 pulses it completely vanishes. Then this pulse fed to TS in this, it minimizes the offset. And fed

input to counter and at output of counter it shows $(10011110)_2 = (158)_{10}$.

Applications:

Time-to-digital converters are used in high energy and particle physics, for measurement and instrumentation applications, for time-of-flight measurement, digital PLLs, and data converters.The first and currently most important TDC application in integrated electronics is definitively the digital phase-locked-loop (PLL). The purpose of phase-locked-loops is to generate a (quasi-)periodic signal, i.e., an output frequency, that has a fixed frequency ratio with respect to a reference signal received at its input. The TDC can be used in TOF laser range finders to measure distance to a target. Besides surveying and navigation, distance measurement using TOF laser range finders is used for collision avoidance and safety in several systems like drones, robotics, and autonomous vehicles. The system consists of a laser pulse emitter or transmitter, an echo receiver, and a TDC. In this system, TDC can measure the round-trip time between a light pulse emission and its echo from the target. The light pulse transmitter triggers the TDC measurement by providing the start input and the receiver stops the TDC. Using the equation D = C × TOF / 2, where C is the speed of light, the distance D to the target can be calculated once the TOF is known.

Conclusion:

In this paper by using pulse shrinking mechanism,we achieved dynamic range andarea efficiency. We get a resolution of 17.00ps. As we have import cells (NMOS, PMOS) from library(from TSMC 0.180-μm) lot of nonlinearities is coming, the accuracy of the circuit can be improved if we design cells ourselves.Stack of pulse shrinking, and expansion can be further improved to get good resolution**.**

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