WWW.IJRPR.COM

International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

Investigation of Low Power Circuit Design by Improved Feed through Logic-A Review

Prerna Wagadre[1], Anil Khandelwal[2]

[1]M Tech Scholar, Department Of Electronics & Communication Engineering, VNS Group Of Institutions Bhopal M.P.
[2]Assistant Professor, Department Of Electronics & Communication Engineering, VNS Group Of Institutions Bhopal M.P.

ABSTRACT:

The design of a low-power dynamic circuit using a new CMOS domino logic family termed feed through logic is shown in this study. In comparison to static CMOS logic circuits, dynamic logic circuits are more important due to their higher speed and lower transistor requirement. In comparison to recently reported circuit techniques for dynamic logic types, the proposed circuit consumes extremely less dynamic power. Extensive simulation is used to validate the concept. In addition, the suggested architecture fully eliminates the need for an output inverter and non-inverting logic.

Keywords: Feedthrough Logic (FTL); Dynamic CMOS LogicCircuit; Low-Power Adder.

1. INTRODUCTION:

Dynamic logic is a type of circuit architecture that uses less transistors to implement a given logic. When compared to static CMOS logic, the reduced number of transistors results in a significant reduction in device area [1,2,3]. However, the major disadvantage of this logic is its excessive power dissipation due to switching activity and clock, as well as charge redistribution and the need for an additional output inverter. A combination of dynamic and static circuit types [4], usage of multiple supply voltages [5], and dual threshold voltage (VT) [6] have all been proposed in the literature to prevent excessive power dissipation of dynamic logic circuits.

A novel logic family called feedthrough logic (FTL) is presented in [7] to further improve the power consumption of dynamic logic circuits with a very deep logic depth. The FTL concept is expanded for the creation of low power arithmetic circuits.

The authors successfully use FTL for integrated circuits in GaAs technology in [8]. Furthermore, FTL [7] eliminates the issues associated with dynamic logic in [1].

$$P_{total} + P_{static} + P_{dynamic} + P_{short\ circuit}$$
$$= V_{dd} I_l + V_{dd} F_{clk} \sum V_{i\ swing} C_{i\ load} \alpha_i + V_{dd} \sum I_{i\ sc}$$

Where F_{clk} denotes the system clock frequency, $V_{i\ swing}$ is the voltage swing at node i, $C_{i\ load}$ is the load capacitance at node i, α_i the activity factor at node i, $I_{i\ sc}$ is the short circuit current and I_l is the leakage current.

We present a new circuit architecture that improves feedthrough logic in this study [7]. One more PMOS transistor is used in the suggested circuit.

When compared to FTL [7], simulation results suggest that the proposed circuit's power consumption is reduced by around 40%. It can also be utilized in a cascaded domino stage.

2.CONVENTIONAL HIGH-SPEED STRUCTURE

A NMOS reset transistor (M2) and a pull-up PMOS load transistor make up the circuit (M1). The clock signal is in charge of M1 and M2 (CLK). Here's a quick rundown of the operation's key principles. The output node (OUT) is brought to ground through M2 at CLK =1 (reset phase). M2 is turned off and M1 conducts when CLK = 0 (evaluation phase). Depending on the input (IN) to M3, the output node evaluates to either a logic high or low level. The output node is dragged towards VDD if IN=0; else, it remains low. The output is charged to V_{DD} in typical domino logic [1], causing cascading problems and significant dynamic power consumption, but here the output is reset to low during the reset phase. The use of an inverter for cascading these logic blocks is no longer necessary. This logic is faster because the output merely transitions from V_{TH} to V_{OH} or V_{OL} [7], but it consumes more power due to the fact that VOL is not 0 V.

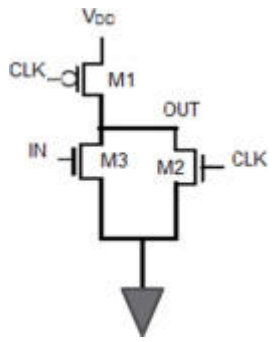

Fig. 1. HS0 Structure in [7]

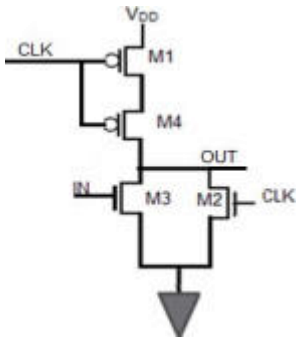

Fig. 2. Proposed HS0

3.PROPOSED CIRCUIT:

Figure 2 depicts the proposed low-power circuit. It consists of a fourth PMOS transistor (M4) connected to M1 in series. The transistor M4 raises the overall resistance between V_{DD} and output. In comparison to HS0, V_{OL} decreases due to ratio logic [7]. This decrease in VOL aids in lowering dynamic power consumption.

The proposed HS0 circuit operates in the same way as HS0 [7] during the reset phase. If the input (IN) is logic-1 during the evaluation phase, the output node is dragged down to logic low, i.e. V_{OL}. Because this V_{OL} is smaller than that of HS0 [7], the suggested HS0's power consumption is reduced.

4.FULL ADDER DESIGN USING PROPOSED HS0

In this section we present the design of a basic sum and carry cell for the full adder using proposed HS0 logic. Fig.3.shows the implementation of $\overline{sum}$ and Fig. 4. shows c_{out} of the adder. An 8-bit ripple carry adder is designed byusing these basic sums and carry cell.

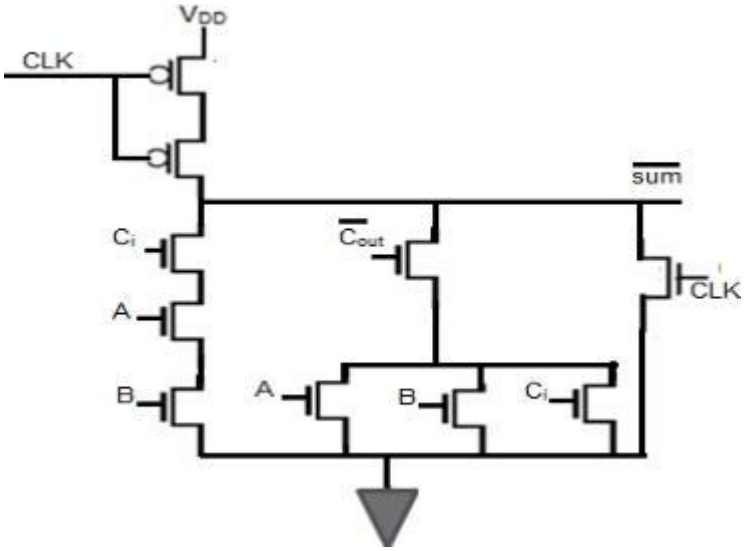

Fig. 3. Sum cell

5.SIMULATION RESULTS AND COMPARISONS:

We used the UMC 0.18 m CMOS process technology model library, with the parameter for typical process corner at 25^{0}C. For all simulations, the power supply V_{DD} remains constant at 1.8 V. The HSPICE simulator is used to simulate circuits. The behavior of a lengthy chain (10) of inverters and 8-bit ripple carry adders is simulated to compare the proposed structure to the existing HS0 structure [7]. For a 10 fF capacitive load at 100 MHz, Table I illustrates the dynamic power comparison for 10 stages of inverter developed by proposed HS0 in Fig.5 and current HS0 in [7].Fig. 6. Plot the output voltage from the first to the tenth stages of an inverter with 10 fF capacitive loads. The output voltage drops to a lower VOL, which is lower than V_{OL} in [7].

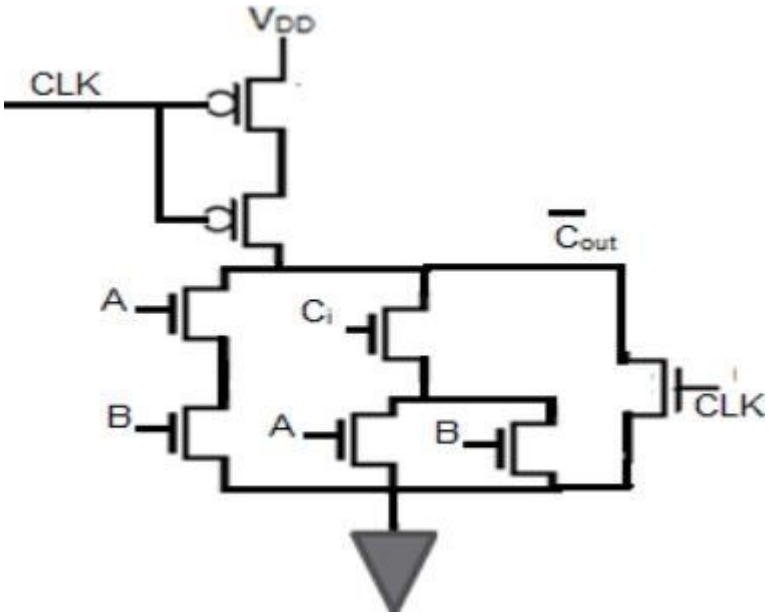

Fig. 4. Carry cell

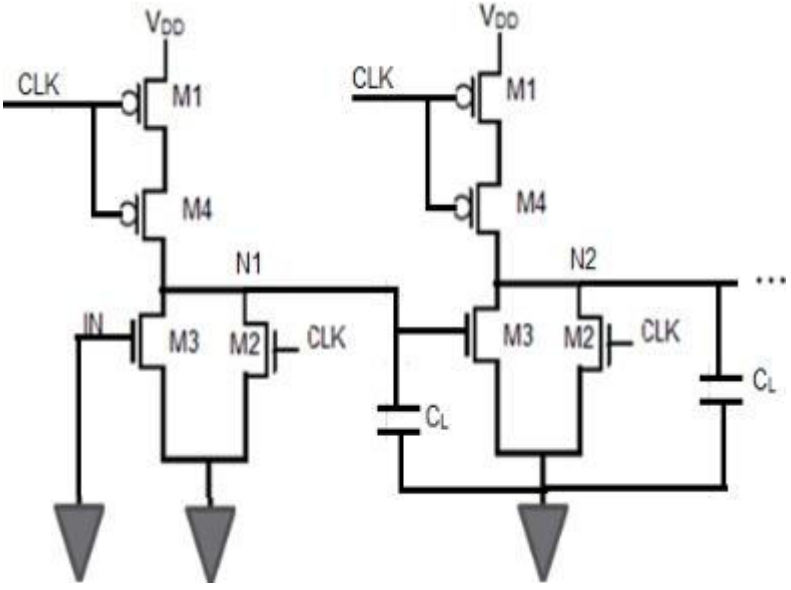

Fig. 5 . Long chain of inverters designed by proposed HS0 (10-stage)

The sum and carry cells in Figs. 3 and 4 are used to create an 8-bit ripple carry adder. Table II compares the propagation delay and dynamic power of the proposed structure's 8-bit ripple carry adder to that of the present HS0 in [7]. The simulation results show that the suggested adder consumes relatively less power when compared to the present adder in [7].

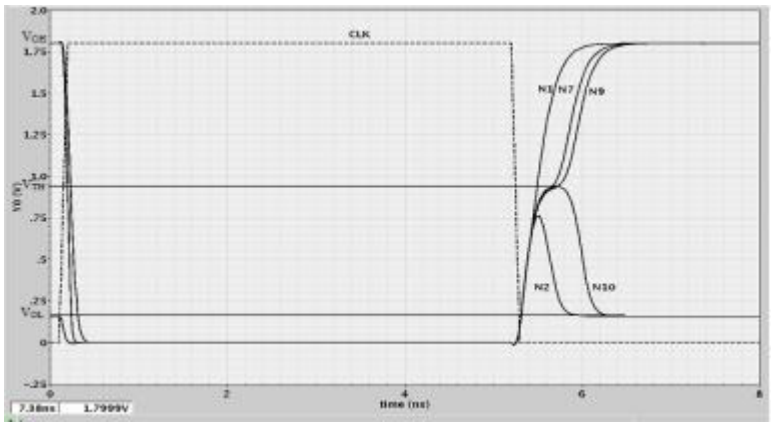

Figure 6 shows the output voltages of inverters from the first (N1) to the tenth (N10) stages.

The power delay product is shown in Fig.7. The PDP chart confirms that the proposed structure has less PDP as compared to HS0 in [7].

In Fig.8. The propagation delays of both structures are shown with respect to output load capacitance C_L. The gap between proposed structure and HS0 in [7] increases with increase in C_L. The proposed circuit is slower as compared toHS0.

The effect of C_L on dynamic power for both structures are shown in Fig.9. C_L is varies from 1 fF to 20 fF. The dynamic power dissipation of the proposed structure is lessas compared to HS0.

TABLE I. SIMULATION RESULTS FOR DYNAMIC POWER FOR THE PROPOSED CIRCUIT IN FIG.5 AND THE EXISTING HS0 STRUCTURE IN [7].(10-INVERTER)

Logic family	Power (μ)
HS0 in [7]	268
Proposed HS0	151

TABLE II. SIMULATION RESULTS FOR DYNAMIC POWER FOR AN 8-BITRIPPLE CARRY ADDER DESIGNED BY PROPOSED CIRCUIT AND THE EXISTING HS0 STRUCTURE IN [7]

Logic family	Power(μW)	tp (ns)
HS0 in [7]	601	0.507
Proposed HS0	335	0.690

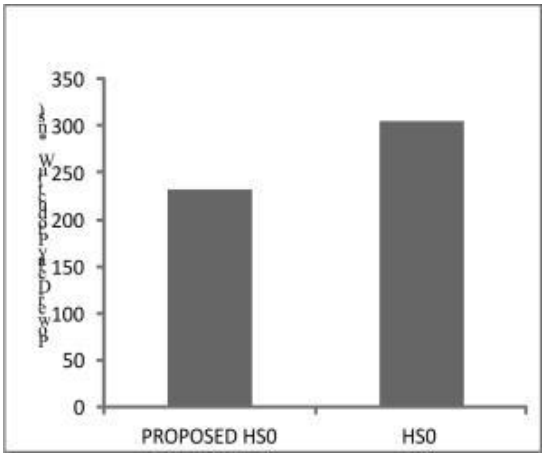

Fig.7. Power delay product of proposed structure and existing HS0

The power delay product is shown in Fig.7. The PDP chart confirms that the proposed structure has less PDP as compared to HS0 in [7]. In Fig.8. The propagation delays of both structures are shown with respect to output load capacitance C_L. The gap between proposed structure and HS0 in [7] increases with increase in C_L. The proposed circuit is slower as compared to HS0.The effect of C_L on dynamic power for both structures are shown in Fig.9. C_L is varying from 1 fF to 20 fF. The dynamic power dissipation of the proposed structure is lessas compared to HS0.

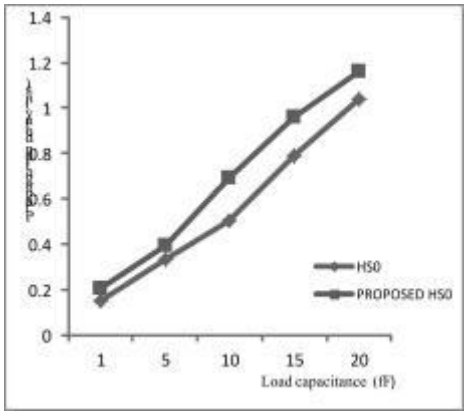

Fig.8. Effect of output load on propagation delay of proposed structure and existing HS0

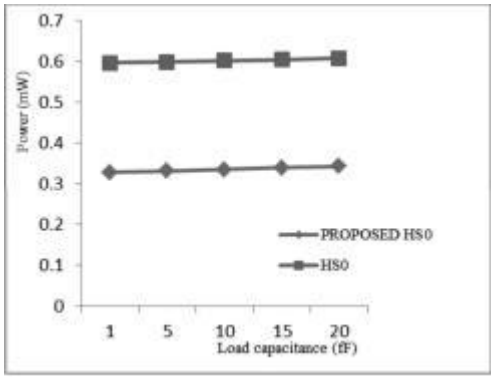

Figure 9 shows the impact of output load capacitance on dynamic power dissipation in the proposed and existing HS0 structures.

6.CONCLUSION

We suggested a low-power dynamic circuit in this paper. The suggested circuit is modelled using UMC's 0.18-micron CMOS manufacturing technology. When compared to the recently proposed FTL system, the proposed circuit consumes 40% less dynamic power. This paper also includes a simulation of an 8-bit ripple carry adder. The simulation results show that the suggested circuit's power delay product outperforms the present HS0 structure for a particular load and at the same frequency of operation. The proposed circuit can be utilized to create a low-power processor with a primary focus on reduced power consumption.

REFERENCES

[1] J.M. Rabaey, A. Chandrakasan, B. Nikolic, 'Digital Integrated Circuits: A Design perspective' 2e Prentice-Hall, Upper saddle River, NJ, 2002.

[2] S. M. Kang, Y. Leblebici, 'CMOS Digital Integrated Circuits: Analysis & Design', TATA McGraw- Hill Publication, 3e, 2003.

[3] N. Weste, K. Eshraghian, 'Principles of CMOS VLSI Design, A systems perspective', Addision Wesley MA, 1988.

[4] S .Mathew, M. Anders, R. Krishnamurthy, S. Borkar, "A 4 GHz 130 nm address generation unit with 32-bit sparse-tree adder core," IEEE J. Solid State Circuits Vol.38 (5) 2003, pp. 689-695.

[5] R.K. Krishnamurthy, S. Hsu, M. Anders, B. Bloechel, B. Chatterjee, M. Sachdev, S. Borkar, "Dual Supply voltage clocking for 5GHz 130nm integer execution core," proceedings of IEEE VLSI Circuits Symposium, Honolulu Jun. 2002, pp. 128-129.

[6] S. vangal, Y. Hoskote, D. Somasekhar, V. Erraguntla, J. Howard, G. Ruhl, V. Veeramachaneni, D. Finan, S. Mathew, and N. Borkar, "A 5-GHz floating point multiply-accumulator in 90-nm dual VT CMOS," in Proc. IEEE Int. Solid-State Circuits Conf., San Francisco, CA, Feb.2003, pp. 334–335.

[7] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, " Analysis of high performance fast feedthrough logic families in CMOS,"

IEEE Trans. Cir. & syst. II, vol. 54, no. 6, Jun. 2007, pp. 489-493.

[8] S. Nooshabadi and J. A. Montiel-Nelson, "Fast feedthrough logic: A high performance logic family for GaAs," IEEE Trans. Circuit Syst. I, Reg. Paper, vol. 51, no. 11, Nov.2004, pp. 2189-2203.

[9] K. Navi, V. Foroutan, M. Rahimi Azghadi, M. Maeen, M. Ebrahimpour, M. Kaveh, O. Kavehei, "A Novel low power full-adder cell with new technique in designing logical gates based on static CMOS Inverter," ELSEVIER Microelectronics Journal, Vol.40, 2009,pp.1441–1448.

der cell with new technique in designing logical gates based on static CMOS Inverter," ELSEVIER Microelectronics Journal, Vol.40, 2009,pp.1441–1448.