WWW.IJRPR.COM

**International Journal of Research Publication and Reviews**

Journal homepage: www.ijrpr.com ISSN 2582-7421

# Study of Total Harmonic Distortion Systems and Control Strategies for Diode Clamped Multilevel Inverter

***Sanyam Kumar[1], Sitaram Pal[2]***

[1]M. Tech Scholar, *Department of Electrical and Electronics Engineering, Rbindranath Tagore University, Bhopal, Madhya Pradesh, India*
Email- kumar.sanyam97@gmail.com

[2] Assitant Professor, *Department of Electrical and Electronics Engineering, Rbindranath Tagore University, Bhopal, Madhya Pradesh, India*
Email- palifit2013@gmail.com

**ABSTRACT**

Improved power quality, fewer switching losses, better electromagnetic compatibility, and higher voltage capability have all contributed to the popularity of multilayer power conversion. Due to their capacity to synthesis waveforms with a superior harmonic spectrum and achieve greater voltages with a limited maximum device rating, these converters are appropriate for high-voltage and high-power applications. These gains in power conversion are made possible by employing a multiple voltage steps technique, which is critical for medium voltage operation in order to reduce dv/dt and stress on motor winding insulations. In recent years, multilevel power conversion has gotten a lot of interest for high-power applications. In recent literatures, a variety of topologies and modulation algorithms have been presented and intensively investigated for utility and driving applications. The diode clamped inverter is the most typical multilevel design, in which a diode is employed as a clamping device to clamp the DC bus voltage and achieve steps in the output voltage. Two series connections of DC capacitors, C1 and C2, divide the DC bus voltage into three voltage levels. Electricity generation (AC power), electric power transmission, and finally electricity distribution are all part of the electric power sector.

Keywords : Clamping diodes DC 1 and DC 2, Power Quality Improvement, THD, DC /AC converter topologies .

## Introduction

The notion of multilayer power conversion is gaining traction, owing to better power quality. The diode clamped inverter is the most typical multilevel design, in which a diode is employed as a clamping device to clamp the DC bus voltage and achieve steps in the output voltage. Nabae, Takahashi's neutral point converter was essentially a three-level diode-clamped inverter. Two pairs of switches and two diodes make up a three-level diode clamped inverter. The diodes used to give AC cess to mid-point voltage work in complementary mode for each switch pair. In a three-level inverter, each of the inverter's three phases shares a common DC bus that has been separated into three levels by two capacitors.

## Background of the research

For more than three decades, multilevel inverters have been under development and have found successful industrial uses. However, this is still a developing technology, with numerous new contributions and commercial topologies reported in recent years. The goal of this dissertation is to gather and examine recent contributions in order to determine the current state of the art and technological trends in order to give readers with a thorough and informative overview of where multilevel converter technology stands and is headed. This chapter begins with a quick survey of well-known multilevel inverters, with a special focus on their current state in industrial applications.

## Concept of multilevel inverters

The output of a multilevel inverter is voltages with stepped waveforms, which are generated by an array of power semiconductor devices and capacitor voltage sources. The commutation of the switches allows the capacitor voltages to be added to generate a high-voltage output, while the power semiconductors can only sustain lower voltages. A two-level inverter produces an output voltage with two values (levels) in relation to the capacitor's negative terminal. In multilayer converter topologies, a voltage level of three is considered the smallest.

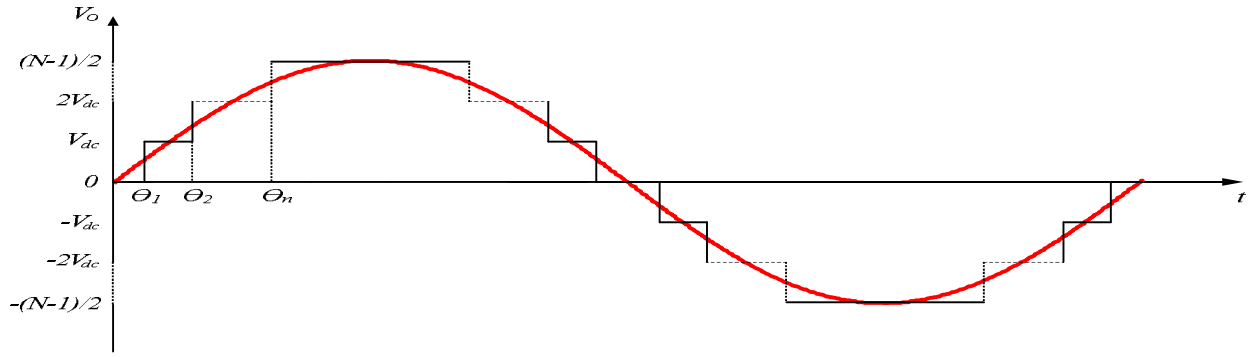


**Figure 1. Multilevel inverters' generalized stepped waveform**

## Classification of multilevel inverters

The diode-clamped multilevel inverter (DCMLI), the flying-capacitors multilevel inverter (FCMLI), and the cascaded H-bridge multilevel inverter are the three topologies used to classify multilevel inverters (CHBMLI).

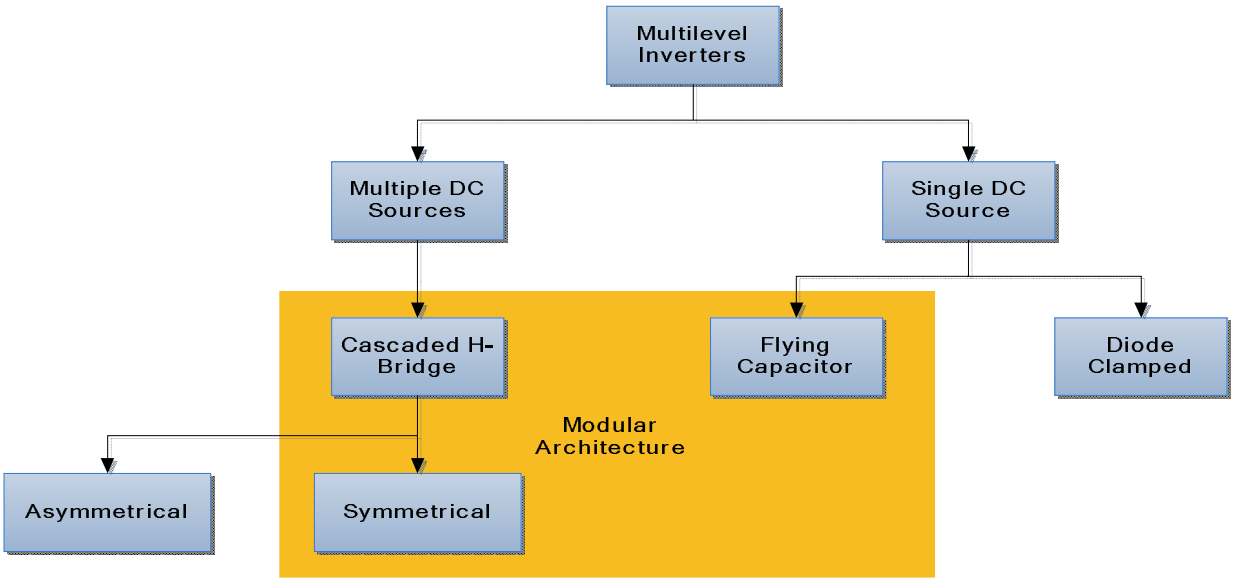


**Figure 2. Multilevel inverter classifications**

## Diode clamped multilevel inverter

The term "diode-clamped multilevel inverter" refers to a neutral-point clamped PWM inverter that has been expanded to a larger number of levels [3, 4]. Because of its capacity to operate at high voltage and efficiency, the diode-clamped multilevel inverter has gained widespread appeal. a 5-level diode-clamped inverter's power circuit It requires four complementary switch pairs ($S_1$, $S_1'$), ($S_2$, $S_2'$), ($S_3$, $S_3'$) and ($S_4$, $S_4'$) that are defined in such a way that turning on one pair of switches prevents the activation of the other switch pairs. At any given time, a set of four switches on a 5-level inverter are active. $C_1$, $C_2$,$C_3$and $C_4$ are DC-link capacitors that maintain a constant voltage. The capacitor voltages will be VDC /4 if they are fed by a DC link voltage of $V_{dc}$. Clamping diodes are used to limit the voltage stress across the power switch to the voltage level of one capacitor. The number of clamping diodes increases quadratically with the number of output levels as the number of output levels increases.

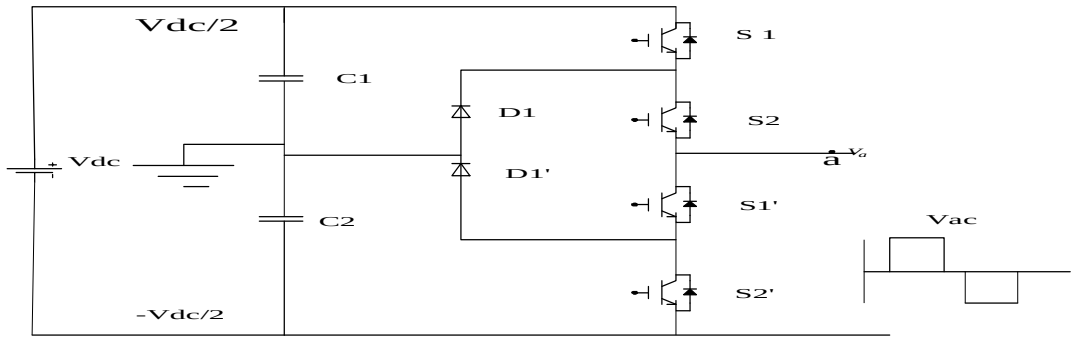


Figure 3. 7 3-level Diode-clamped inverter

In the balanced state, the three-level inverter. A phase-leg a voltage and a phase-leg b voltage make up the line voltage $V_{ab}$. For a three-level inverter, the resulting line voltage is a 5-level staircase waveform, and for a five-level inverter, it is a 9-level staircase waveform..

## Operation of DCMLI

The DC bus of a three-level diode-clamped converter is made up of two capacitors $C_1$, $C_2$. The voltage across each capacitor is $V_{DC}$ /2 for DC-bus voltage Vdc, and each device voltage stress is confined to one capacitor's voltage level $V_{DC}$ /2 via clamping diodes. The output phase voltage reference point is the neutral point n, which is used to describe how the staircase voltage is generated. Three switch combinations are used to create three-level voltages.

Table-1 Switching states in one leg of the five-level diode clamped inverter

| Voltage $V_{ao}$ | Switch state | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_1$' | $S_2$' | $S_3$' | $S_4$' |
| $V_{ao}= V_{DC}$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $V_{ao} = V_{DC/2}$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| $V_{ao} = 0$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $V_{ao} = - V_{DC/2}$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| $V_{ao} = - V_{DC}$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Capacitor voltage unbalance**

A power converter is used to convert real power from AC to DC (rectifier operation) or DC to AC in most applications (inverter operation). The charging time for rectifier operation (or discharging time for inverter operation) is variable for each capacitor while running at unity power factor.

## The proposed modulation scheme

Eight switches in the upper leg and eight switches in the lower leg are clamped by diodes in the proposed nine-level multilevel inverter. The suggested inverter uses a carrier-based modulation approach to fire the eight switches on the upper leg, and eight triangular carrier waveforms are compared to a reference sinusoidal waveform. In order to realize harmonic injection modulation schemes, the third harmonic signal is now inserted on the reference sinusoidal wave shape.

.

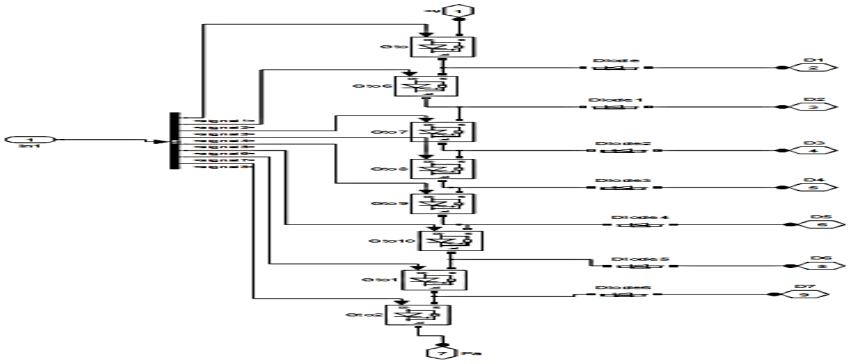

Fig.4. subsystem for one leg of 9 level DCMLI

The amount of harmonic injection will be controlled by the third harmonic injected waveform's changeable amplitude. K is the parameter that represents the magnitude of the injected third harmonic. Where K is the ratio of the amplitude of the reference fundamental waveform to the amplitude of the injected third harmonic waveform. The value of k is 0.5 if the amplitude of the reference fundamental waveform is equal to 12 and the magnitude of the third harmonic injected waveform is 6.

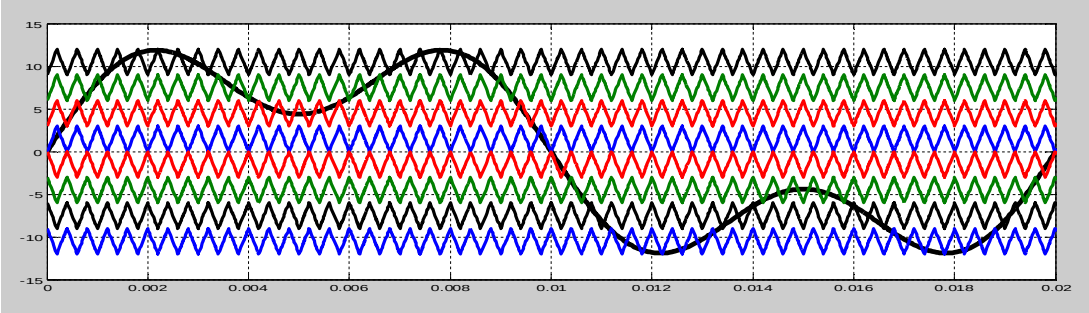


Fig.5. Third harmonic injection modulation scheme for K=0.5

## Analysis of THD and RMS value for variation in modulation index for K = 0.25

The waveforms for the third harmonic reference injected for modulation index Ma=1, 0.9, and 0.8, respectively, are shown in Figure 6 (a), (b), and (c).

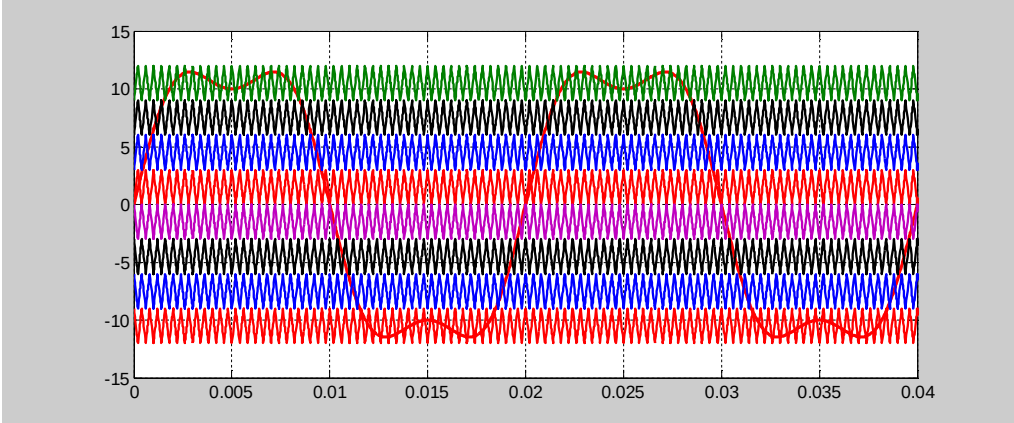


Fig. 6.(a) Carrier and reference waveform, K=0.25, Ma=1

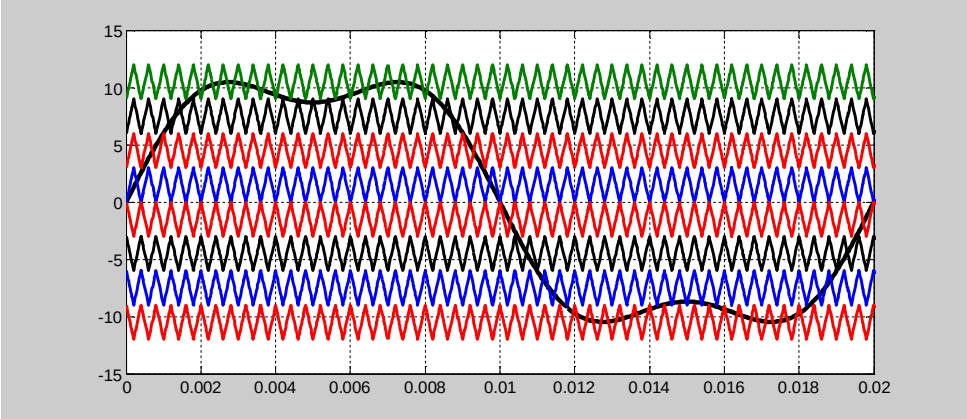


Fig. 6. (b) Carrier and reference waveform, K=0.25, Ma=0.9

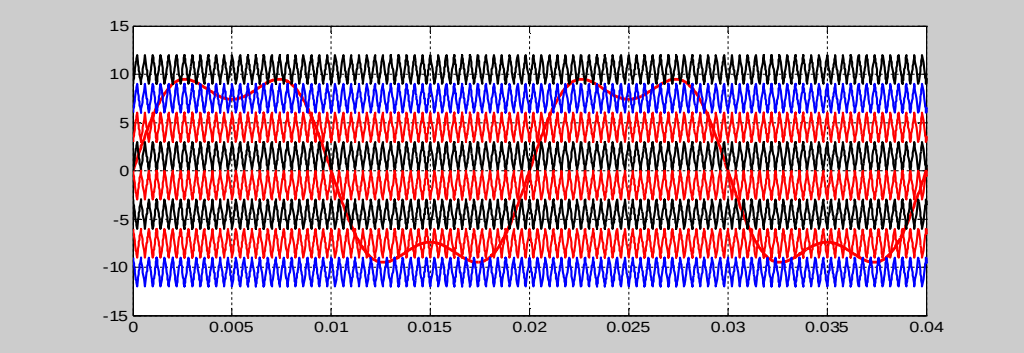


Fig. 6. (c) Carrier and reference waveform, K=0.25, Ma=0.8

A modulation index variation is also used to see how it affects the magnitude of output voltage and THD. The phase voltage waveform for modulation index 1 is shown in Figure 6. The r.m.s. value of the fundamental component is 432.7V, and the THD is 24.85 percent, as shown in the figure

## Analysis of THD and RMS value for variation in modulation index for K = 0.5

The reference and carrier waveforms for K =0.5,Ma=1.0 can easily be seen in the figure, with a bigger dip in the peak value. A modulation index variation is also used to see how it affects the magnitude of output voltage and THD.

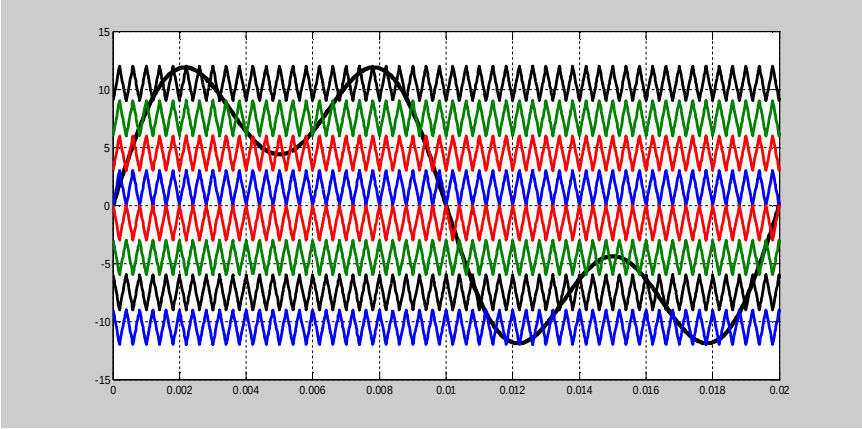


Fig.7. (a) Carrier and reference waveform, K=0.5, Ma=1

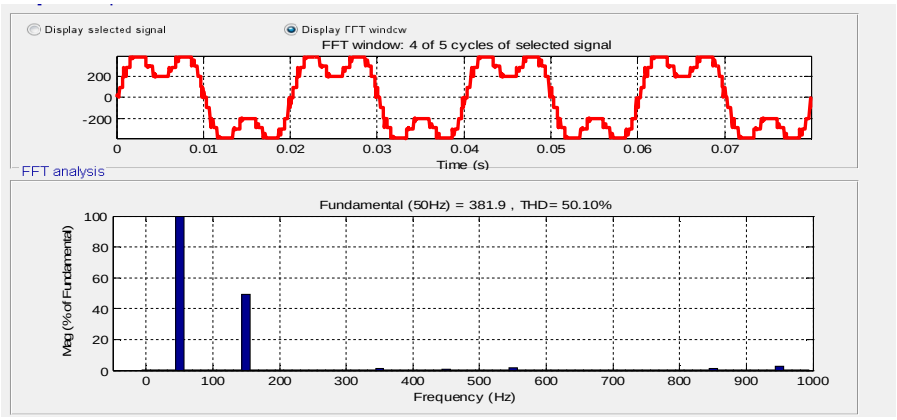


Fig. 7 .(b) Phase voltage waveform and its harmonic spectrum, K=0.5, Ma=0.8

The phase voltage waveform for modulation index 0.9 is shown in Figure 7. The r.m.s. value of the fundamental component is 381.9V, and THD is 50.10 percent, as shown in the figure.

***The comparison of THD and rms vaule for the different value of k is given in the following table.***

| **Harmonic Injection factor K=0.25** | | | **Harmonic Injection factor K=0.5** | | |
|---|---|---|---|---|---|
| Modulation index | THD in % | R.m.s. value In Volt | Modulation index | THD in % | R.m.s. value In Volt |
| 0.8 | 28.64 | 341.1 | 0.8 | 57.96 | 349.1 |
| 0.9 | 25.84 | 379.2 | 0.9 | 50.10 | 381.9 |
| 1.0 | 24.85 | 432.7 | 1.0 | 45.63 | 436.4 |

## Conclusion

The third harmonic injection was used in this extensive study on a nine level diode clamped MLI. The findings were obtained for various third harmonic injected signal magnitudes and modulation indexes. The simulation findings indicate that injecting the third harmonic signal enhances DC bus consumption, but it significantly changes the spectrum features of the output voltage signal. Similarly, THD is compared for various values of k and modulation index, and it is discovered that increasing k, which is the factor controlling injected 3rd Harmonic, results in an increase in output voltage THD.

**References**


[1] Pregelj, A.; Begovic, M.; Rohatgi, A. "Impactt of inverter configuration on PV system reliability and energy production," Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE , vol., no., pp. 1388-1391, 19-24 May 2002

[2] Jih-Sheng Lai; Fang ZhengPeng; "Multilevel converters-a new breed of power converters," Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE , vol.3, no., pp.2348-2356 vol.3, 8-12 Oct 1995.

[3] Rodriguez, J.; Jih-Sheng Lai; Fang ZhengPeng; "Multilevel inverters: a survey of topologies, controls, and applications," Industrial Electronics, IEEE Transactions on, vol.49, no.4, pp. 724- 738, Aug 2002.

[4] Rodriguez, J.; Franquelo, L.G.; Kouro, S.; Leon, J.I.; Portillo, R.C.; Prats, M.A.M.; Perez, M.A.; , "Multilevel Converters: An Enabling Technology for High-Power Applications," Proceedings of the IEEE , vol.97, no.11, pp.1786-1817, Nov. 2009.

[5] Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Pérez, M.A. "A Survey on Cascaded Multilevel Inverters," Industrial Electronics, IEEE Transactions on, vol.57, no.7, pp.2197-2206, July 2010.

[6] Panagis, P.; Stergiopoulos, F.; Marabeas, P.; Manias, S. "Comparison of state of the art multilevel inverters," Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, vol., no., pp.4296-4301, 15-19 June 2008.

[7] Tolbert, L.M.; Fang ZhengPeng; Habetler, T.G. "Multilevel converters for large electric drives," Industry Applications, IEEE Transactions on, vol.35, no.1, pp.36-44, Jan/Feb 1999.

[8] Fang ZhengPeng; , "A generalized multilevel inverter topology with self voltage balancing," Industry Applications, IEEE Transactions on , vol.37, no.2, pp.611-618, Mar/Apr 2001.

[9] Teodorescu, R.; Blaabjerg, F.; Pedersen, J.K.; Cengelci, E.; Enjeti, P.N.; , "Multilevel inverter by cascading industrial VSI," Industrial Electronics, IEEE Transactions on , vol.49, no.4, pp. 832- 838, Aug 2002.

[10] Nabae, Akira; Takahashi, Isao; Akagi, Hirofumi; , "A New Neutral-Point-Clamped PWM Inverter," Industry Applications, IEEE Transactions on , vol.IA-17, no.5, pp.518-523, Sept. 1981

[11] T. A. Meynard and H. Foch, “Multi-level choppers for high voltage applications,” in Proc. Eur. Conf. Power Electron. Appl., 1992, vol. 2, pp. 45–50.

[12] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, “A non-conventional power converter for plasma stabilization,” in Proc. Power Electron. Spec. Conf., 1988, pp. 122–129.

[13] De, S.; Banerjee, D.; Siva Kumar, K.; Gopakumar, K.; Ramchand, R.; Patel, C.; , "Multilevel inverters for low-power application," Power Electronics, IET , vol.4, no.4, pp.384-392, April 2011.

[14] Liu, Y.; Luo, F.L. "Multilevel inverter with the ability of self voltage balancing," Electric Power Applications, IEE Proceedings - , vol.153, no.1, pp. 105- 115, 1 Jan. 2006.

[15] A. Rufer, M. Veenstra, and K. Gopakumar, “Asymmetric Multilevel Converter for HighResolution Voltage Phasor Generation”, in Proceedings of the European Power Electronics and Applications Conference (EPE 1999), 1999