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3D Integrated Circuits

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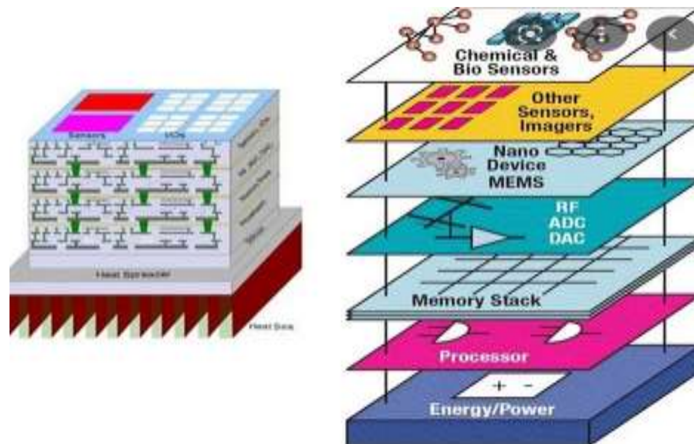
ABSTRACT:

3D integration with through-silicon via (TSV) is a promising candidate to perform system-level integration with smaller package size, higher interconnection density, and better performance. TSV fabrication is the key technology to permit communications between various strata of the 3D integration system. TSV fabrication steps, such as etching, isolation, metallization processes, and related failure modes[4]

Introduction:

A **three-dimensional integrated circuit** (**3D IC**) is a MOS (metal-oxide semiconductor) integrated circuit (IC) manufactured by stacking silicon wafers or dies and interconnecting them vertically using, for instance, through-silicon vias (TSVs) or Cu-Cu connections, so that they behave as a single device to achieve performance improvements at reduced power and smaller footprint than conventional two dimensional processes. The 3D IC is one of several 3D integration schemes that exploit the z-direction to achieve electrical performance benefits in microelectronics and nanoelectronics.[1]



Definition: A 3DIC is a three-dimensional integrated circuit (IC) built by vertically stacking different chips or wafers together into a single package. Within the package, the device is interconnected using through-silicon vias (TSVs) or hybrid bonding.[2]

Manufacturing Technology Of 3d Ics :

There are four ways to built 3D ICs :- 1. Monolithic 2. Wafer on wafer 3. Die on wafer 4. Die on die

1.Monolithic Electronic components and their connections (wiring) are built in layers on a single semiconductor wafer, which is then diced into 3D ICs. There is only one substrate, hence no need for aligning, thinning, bonding, or through-silicon vias.

2. Wafer on wafer Electronic components are built on two or more semiconductor wafers, which are then aligned, bonded, and diced into 3D ICs.

3. Die on wafer Electronic components are built on two semiconductor wafers. One wafer is diced aligned and bonded onto die sites of the second wafer.

4.Die on die Electronic components are built on multiple dice, which are then aligned and bonded. One advantage of die-on-die is that each component die can be tested first, so that one bad die does not ruin an entire stack[5]

Challenges:

Because this technology is new, it carries new challenges, including:

Cost: While cost is a benefit when compared with scaling, it has also been identified as a challenge to the commercialization of 3D ICs in mainstream consumer applications. However, work is being done to address this. Although 3D technology is new and fairly complex, the cost of the manufacturing process is surprisingly straightforward when broken down into the activities that build up the entire process.

Yield: Each extra manufacturing step adds a risk for defects. In order for 3D ICs to be commercially viable, defects could be repaired or tolerated, or defect density can be improved.

Heat: Heat building up within the stack must be dissipated. This is an inevitable issue as electrical proximity correlates with thermal proximity. Specific thermal hotspots must be more carefully managed.

Design complexity: Taking full advantage of 3D integration requires sophisticated design techniques and new CAD tools.

TSV-introduced overhead: TSVs are large compared to gates and impact floorplans. At the 45 nm technology node, the area footprint of a 10μm x 10μm TSV is comparable to that of about 50 gates.Furthermore, manufacturability demands landing pads and keep-out zones which further increase TSV area footprint. Depending on the technology choices, TSVs block some subset of layout resources.

Testing: To achieve high overall yield and reduce costs, separate testing of independent dies is essential. However, tight integration between adjacent active layers in 3D ICs entails a significant amount of interconnect between different sections of the same circuit module that were partitioned to different dies.

Lack of standards: There are few standards for TSV-based 3D IC design, manufacturing, and packaging, although this issue is being addressed. Heterogeneous integration supply chain: In heterogeneously integrated systems, the delay of one part from one of the different parts suppliers delays the delivery of the whole product, and so delays the revenue for each of the 3D IC part suppliers.

Lack of clearly defined ownership: It is unclear who should own the 3D IC integration and packaging/assembly.[1]

What is 2.5D & 3D IC Packaging?

2.5D / 3D are packaging methodology for including multiple IC inside the same package. In 2.5D structure, two or more active semiconductor chips are placed side-by-side on a silicon interposer for achieving extremely high die-to-die interconnect density. In 3D structure, active chips are integrated by die stacking for shortest interconnect and smallest package footprint.

ASE is one of the pioneers in 2.5D/3D packaging technology and has successfully launched world's first mass production of 2.5D IC package equipped with High Bandwidth Memory (HBM). [6]

Advantages:

3D integrated circuits evolved from planar processes to create multilayer semiconductor packages with multiple feature levels.

- Lower Power Consumption.
- Faster Signal Transitions.
- Analog and Digital Integration.
- Space Savings.

Conclusion :

3D ICs will be the first of a new generation of dense, inexpensive chips having less delay and interconnection losses that will replace the conventional storage and recording media. [5]

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