WWW.IJRPR.COM

International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

Radical Low Power Compressor Using Sub threshold Adiabatic Logic

Geethu N

Student,CEC,India

A B S T R A C T

Sub threshold adiabatic logic is analyzed under sub threshold regime to improve the efficiency of power consumption in ultra low power circuit designs. The schematics and layout of various compressors like 4-2,5-2,7-2 has been designed to show the workability of the proposed logic. Further, a parameter variation over temperature effects and process on sub threshold adiabatic logic based compressors has also been addressed separately. A comparative study of conventional logic implemented compressors and SAL[sub threshold adiabatic logic] compressors has been done.

Keywords: Adiabatic Logic, Sub Threshold Regime, Compressors, Leakage, Low Power.

INTRODUCTION:

The demand for implementing ultralow-power digital systems in many modern applications, such as mobile systems, sensor networks, and implanted biomedical systems, has increased the importance of designing logic circuits in sub threshold regime. These emerging applications have low energy as the primary concern instead of performance, with the eventual goal of harvesting energy from the environment. In sub threshold logic circuits operate with a supply voltage VDD lower than the transistor threshold voltage VT and utilize the sub threshold leakage current as the operating current.

Conventional CMOS logic circuits utilizing sub threshold transistors can typically operate with a very low power consumption, which is mainly due to the dynamic (switching) power consumption and is quadratically dependent upon the supply voltage as CL fV2 DD (where CL, f , and VDD are the load capacitance, operating frequency, and the supply voltage Recently, adiabatic logic (or energy recovery logicstyle has emerged as a promising approach in strong inversion regime, to reduce dynamic power consumption significantly without sacrificing noise immunity and driving ability. These circuits achieve ultralow energy consumption by steering currents across devices with low voltage differences and by gradually recycling the energy stored in their capacitive loads, especially in low-frequency regime. Since the performance requirements are quite relaxed in many of these

* *Corresponding author*. Tel.: +0-000-000-0000 ; fax: +0-000-000-0000.
E-mail address: author@institute.xxx

energy- efficient sub threshold applications we believe that the adiabatic style can be used efficaciously in a sub threshold regime to make the circuit more energy efficient.

To the best of our knowledge, no paper emphasizes the application of adiabatic logic in weak inversion regime for advanced technology node such as 22 nm. Therefore, the attempt to realize the sub threshold adiabatic logic (SAL) concept is a new endeavor. In general, the design of SAL requires a deep knowledge of the main features of the adopted logic style, such as power dissipation, leakage current, and impact of temperature variation, operating frequency, and noise immunity. In this paper, the behaviors of adiabatic logic in sub threshold regime are discussed in depth.

To demonstrate the workability of the adiabatic logic circuits in sub threshold regime, a 4-2,5-2,7-2 compressors is adopted as a reference circuit. Analysis of energy dissipation along with the sensitivity of energy dissipation on supply voltage and temperature variations is also discussed in depth. Moreover, the analytical expression of optimum frequency and supply voltage under minimum energy condition has been verified through simulations. Extensive experiments are carried out using MICROWIND to ensure the high energy efficiency and design feasibility of the proposed logic in weak inversion regime compared with other conventional CMOS logic.

II. DESIGN LOGICS:

A.Sub threshold adiabatic logic:

In this section, SAL-based gates are designed. After verifying the logical functionality of the gates, we implemented an SAL-based standard cell library, consisting of common digital gates, such as buffer/inverter, two-input and three-input functions, complex gates, and special gates like multiplexers and XOR-XNOR gates , which are necessary to implement the proposed compressors. Hence, our transistor-level designs which guarantee the manufacturability of our designs under all normal conditions with favorable yields.

B. Operations of sub threshold adiabatic logic :

The SAL gate structures resemble either the pull-up or the pull- down network of the static conventional logic. For example, to implement a NAND or a NOR gate, simply the pull-up network can be placed between the supply clock and the output load capacitors, whereas an AND or an OR gate can be implemented using the pull-down network between the supply clock and the output load capacitors. In case of a NAND structure, for every input combination except A = B = 1, the output node voltage will follow the supply clock closely, and we get a triangular output waveform. When A = B = 1 through parallel pMOS transistor, leakage currents will flow as the transistors will behave almost as a constant current source. A very small amount of charge will be stored across the load capacitor, i.e., instead of ground potential, very small voltage will be dropped across the output.

III. COMPRESSOR:

Compressors are arithmetic components, similar in principle to parallel counters, but with two distinct differences: (1) they have explicit carry-in and carry-out bits; and (2) there may be some redundancy among the ranks of the sum and carry-output bits . A. Sub threshold adiabatic 4:2 compressor The 4:2 compressor has 4 input bits and produces 2 sum output bits (out0 and out1), it also has a carry-in (cin) and a carry-out (cout) bit (thus, the total number of input/output bits are 5 and 3); All input bits, including cin, have rank 0; the two output bits have ranks 0 and 1 respectively, while cout has rank 1 as well.

Thus, the output of the 4:2 compressor is a redundant number; for example, out1 = 0 and cout = 1 is equivalent to out1 = 1 and cout = 0 in all cases.

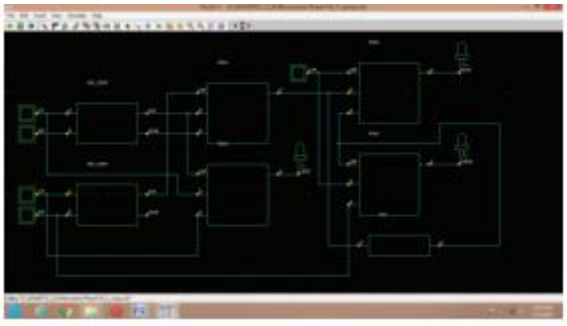

Fig 1: SAL 4:2 Compressor

A. Sub threshold adiabatic 5:2 compressor :

The 5:2 compressor has 5 input bits and produces 2 sum output bits (sum and cout3), it also has a carry-in (cin1, cin2) and a carry-out (cout1, cout2,cout3) bit (thus, the total number of input/output bits are 7 and 4); All input bits, including cin1, have rank 0 and cin2 has rank 2 ; the two output bits have ranks 0 and 1 respectively, while cout2 has rank 1 and cout1 has rank 2.

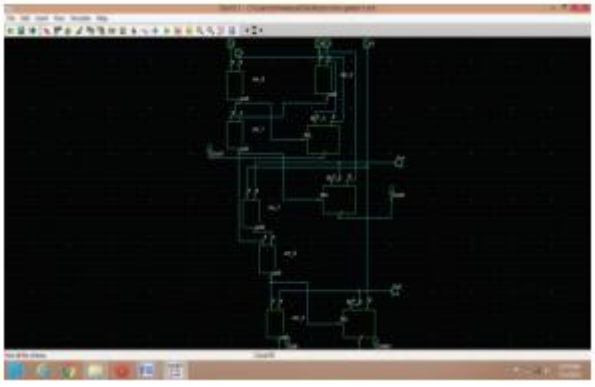

Fig 2: 5:2 Compressor.

B. Sub threshold adiabatic 7:2compressor:

The 7:2 compressor has 7 input bits and produces 2 sum output bits (out0 and out1), it also has a carry-in (Cin0, Cin1) and a carry-out (Cout0, Cout1) bit (thus, the total number of input/output bits are 9 and 4); All input bits, including Cin0, have rank 0 and Cin1 has rank 1 ; the two output bits have ranks 0 and 1 respectively, while Cout0 has rank 1 and Cout1 has rank 2.

Fig 3: 7:2 Compressor

IV. SIMULATION RESULTS

The resultant simulations are observed from the below given post layout simulation results where the various compressors are discussed and the obtained output is more efficient when compared to the existing conventional CMOS compressors. Thus the results show that SAL compressors are more efficient and consume less power compared to conventional logics. The output of the designed SAL are given below

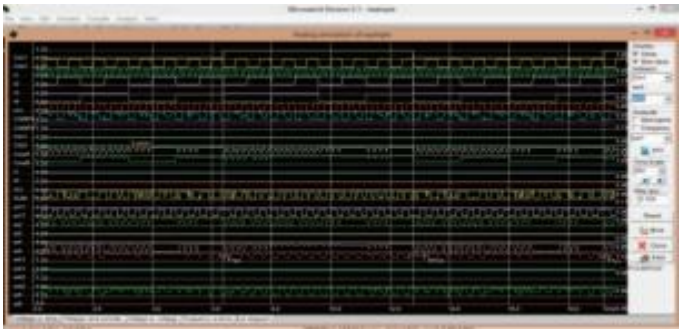

Fig 4:. Post layout simulation of 4:2 SAL compressor.

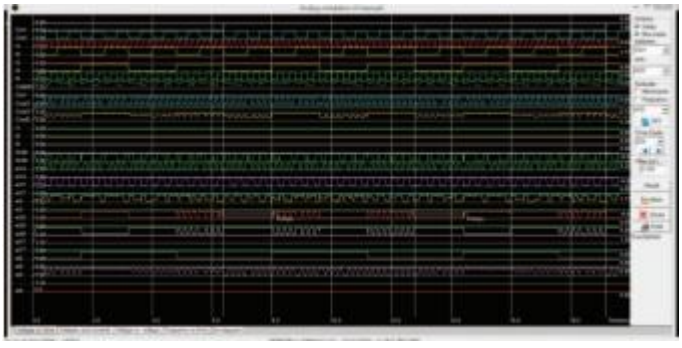

Fig.5: post layout simulation of SAL 5:2 compressor.

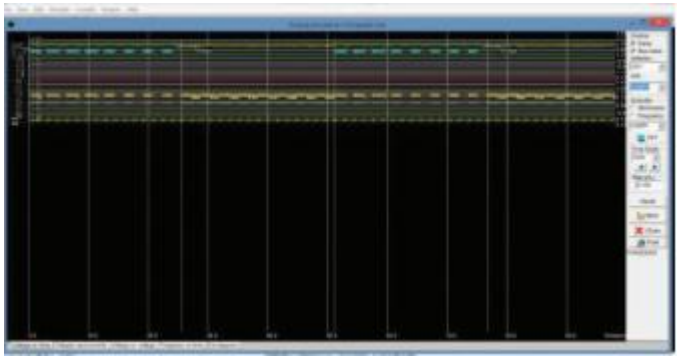

Fig 6. Post layout simulation of SAL 7:2 compressor

V. CONCLUSION

Various compressor circuits based on Subthreshold adiabatic logic has been proposed which provide better performance. The proposed SAL compressor designed with area of 101.500µm and maximum power obtained as 8.623mvand compared with conventional logics in all aspect.

REFERENCES

[1] J. Kwong, Y. K. Ramadass, N. Verma, and A. P. Chandrakasan, "A 65 nm sub-Vt microcontroller with integrated SRAM and switched capacitor DC-DC converter," IEEE J. Solid-State Circuits, vol. 44, no. 1, pp. 115–126, Jan. 2009.

[2] T.-T. Liu and J. M. Rabaey, "A 0.25 V 460 nW asynchronous neural signal processor with inherent leakage suppression," IEEE J. Solid-State Circuits, vol. 48, no. 4, pp. 897–906, Apr. 2013

[3]] A. Calimera, A. Macii, E. Macii, and M. Poncino, "Design techniques and architectures for low-leakage SRAMs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 9, pp. 1992–2007, Sep. 2012

. [4] H. Soeleman, K. Roy, and B. C. Paul, "Robust subthreshold logic for ultra-low power operation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 9, no. 1, pp. 90–99, Feb. 2001.

[5] C.-S. A. Gong, M.-T. Shiue, C.-T.Hong, and K.-W. Yao, "Analysis and design of an efficient irreversible energy recovery logic in 0.18-µm CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 9, pp. 2595–2607, Oct. 2008.