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Synthesis of 8-Bit Reversible Multipler

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ABSTRACT

A systems performance is generally determined by the speed of the multiplier since multiplier is one of the key hardware components in high performance systems such as FIR filters, digital signal processors and microprocessors etc. Multipliers have large area, long latency and consume considerable power. Hence good multiplier architecture increases the efficiency and performance of a system. Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies, such as low power CMOS, Nano-computing and optical computing. Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat. Reversible logic gates produce zero power dissipation. So these can be used for low power VLSI design. Hence a signed multiplier using reversible logic gates will play an important role in every vlsi circuit.

Keywords—Reversible Logic, Reversible logic gates, signed multiplier, Nano-computing.

I. INTRODUCTION

The multipliers are the most important part of all digital signal processors; they are very important in realizing many important functions such as fast Fourier transforms and convolutions. Since a processor spends considerable amount of time in performing multiplication, an improvement in multiplication speed can greatly improve system performance. It has applications in various research areas such as optical computing, low power CMOS design, DNA computing, quantum computing, thermodynamic technology, bioinformatics and nanotechnology. Multiplication can be implemented using many algorithms such as array, booth, carry save, and Wallace tree algorithms. Reversible logic is a promising area of study with regard to the future low power technology.

II. REVERSIBLE LOGIC

A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. Thus inputs to reversible gates can be uniquely determined from its outputs. A reversible logic gate must have the same number of inputs and outputs [6].

In an n-output reversible gate the output vectors are permutation of the numbers 0 to 2n-1. A reversible gate is balanced, i.e. the outputs are is for exactly half of the inputs. A circuit without constants on its inputs and composed of reversible gates realizes only balanced functions. It can realize non balanced functions only with garbage outputs. Some of the major problems with reversible logic synthesis are fan outs cannot be used, and also feedbacks from gate outputs to inputs are not permitted. [6] Features for any gate to become reversible gate as follows: [7] Number of input and output lines must be the same. Feedback (loop) is not allowed in reversible logic. Fan-out is not allowed in reversible logic; Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed. One of the major constraints in reversible logic is to minimize the number of reversible gates used. Minimizing the garbage outputs produced; Garbage output refers to the output that is not used for further computations. Garbage is the number of outputs added to make an n-input k output Boolean function (n,k) function reversible Using minimum number of input constants.

III. LITERATURE SURVEY

Landauer [1] has shown that for every bit of information lost in logic computations that are not reversible, KT ln2 joules of heat energy is generated, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. The amount of energy dissipation in a system

increases in direct proportion to the number of bits that are erased during computation. Bennett [2] showed that KT ln2 energy dissipation would not occur, if a computation were carried out in a reversible way. Thus, a reversible operation ensures low energy dissipation. Since the energy dissipated in CMOS cells is proportional to the number of transitions, to the output load, and to the square of the operating voltage. Energy of E= ½CV2 is stored and this energy gets dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology, we reduce the number of transitions, the capacitance, and the voltage [9]. There are a variety of considerations that must be taken into account in low-power design which include the style of logic, the technology used, and the logic implemented. Factors that were shown to contribute to power dissipation included spurious transitions due to hazards and critical race conditions, leakage and direct path currents, pre-charge transitions, and power-consuming transitions in unused circuitry.

IV. TPS GATE

In order to design a 4*4 signed multiplier a new logic gate is introduced and the block schematic of TPS gate is shown in figure 1. It is having 4 inputs and 4 outputs. The quantum representation is shown in figure 2 and the quantum cost is 4.TPS gate also acts as full adder by connecting D input to 0. The full adder block using this gate is shown in the figure 3.

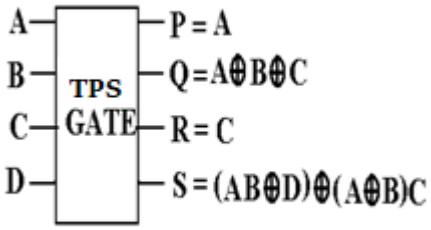


Figure 1: TPS Gate

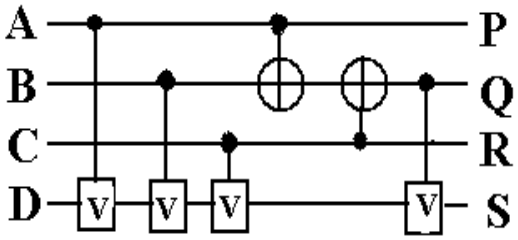


Figure 2: Quantum implementation

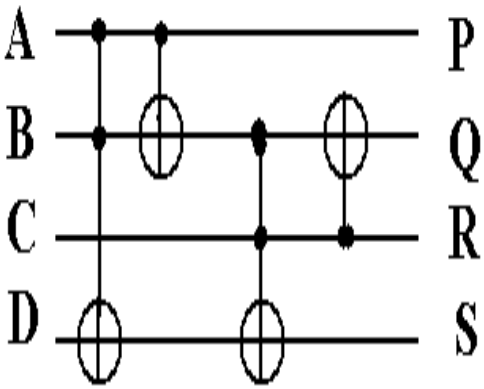


Figure 3: Quantum representation and full adder

V. REVERSIBLE MULTIPLIER WITH TPS GATE

Most of the existing reversible multiplier circuits [13], [10], [14], [8], [11] are counterpart of the conventional multiplier circuit proposed by Maaz [16]. Figure 10 illustrates a 4 × 4 multiplication process. The multiplier structure is based on generating all partial products in one step and then summing their partial products using binary tree network. Therefore, it has the following two components: reversible partial product generation circuit (PPGC) and reversible parallel adder circuit (PAC). The combination of both PPGC and PAC gives the multiplier circuit which is shown in figure 5. The partial products can be generated in parallel using 16 TPS gates. Because of its lower hardware complexity, we use TPS gate instead of other reversible gates. This structure is proposed in [15].

Fast multipliers are essential parts of digital signal processing systems. The speed of multiply operation is of great importance in digital signal processing as well as in the general purpose processors today, especially since the media processing took off. In the past multiplication was generally implemented via a sequence of addition, subtraction, and shift operations. Multiplication can be considered as a series of repeated additions. The number to be added is the multiplicand, the number of times that it is added is the multiplier, and the result is the product.

Each step of addition generates a partial product. In most computers, the operand usually contains the same number of bits. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content. This repeated addition method that is suggested by the arithmetic definition is slow that it is almost always replaced by an algorithm that makes use of positional representation. It is possible to decompose multipliers into two parts. The first part is dedicated to the generation of partial products, and the second one collects and adds them. The basic multiplication principle is twofold i.e., evaluation of partial products and accumulation of the shifted partial products.

$$
\begin{array}{rcccccccccc}
 & & & & a_7 & a_6 & a_5 & a_4 & a_3 & a_2 & a_1 & a_0 \\
 & & & & b_7 & b_6 & b_5 & b_4 & b_3 & b_2 & b_1 & b_0 \\
\hline
 & & & \overline{p}_{08} & p_{08} & p_{08} & p_{07} & p_{06} & p_{05} & p_{04} & p_{03} & p_{02} & p_{01} & p_{00} \\
 & & 1 & \overline{p}_{18} & p_{17} & p_{16} & p_{15} & p_{14} & p_{13} & p_{12} & p_{11} & p_{10} & & N_0 \\
 & 1 & \overline{p}_{28} & p_{27} & p_{26} & p_{25} & p_{24} & p_{23} & p_{22} & p_{21} & p_{20} & & N_1 & \\
\hline
p_{15} & p_{14} & p_{13} & p_{12} & p_{11} & p_{10} & p_9 & p_8 & p_7 & p_6 & p_5 & p_4 & p_3 & p_2 & p_1 & p_0
\end{array}
$$

Figure 4: 8*8 signed multiplication procedure

In this first partial products are generated and then these are given to the parallel adder circuit. The 8 partial products can be generated by TPS gate and is shown in figure 4. The parallel adder circuit is shown in figure 5.

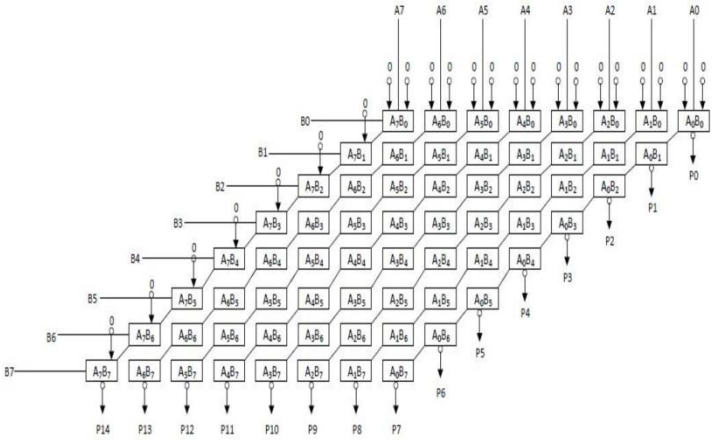
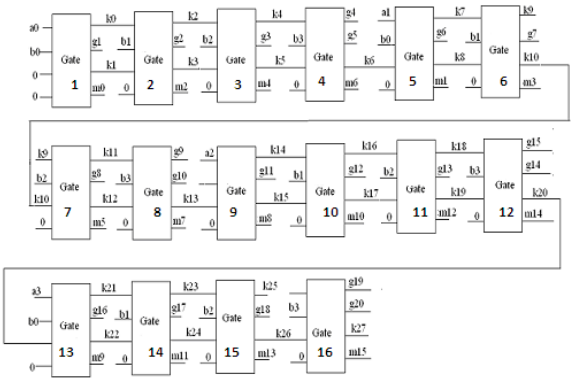


Figure 5: Array structure of parallel multiplier



(a)

Figure 6: Partial product generation using TPS gates

VI. EXPERIMENTAL RESULTS

The performance parameters like gate count, quantum cost, and number of garbage outputs obtained for the TPS reversible multiplier circuit shown in TABLE 1 and is compared with those of other multiplier circuits available in the literature. the output of the reversible signed multiplier is shown in figure 6.

Table 1: Comparison of performance parameters

S.No	Name	Gate count	Quantum cost	Garbage outputs
1	Proposed(TPS)	28	168	42
2	M.Z.Moghadam,K.Navi (Design I) [8]	32	136	28
3	Haghparast et al.[5]	52	152	52
4	Islam et.al [6]	52	144	52

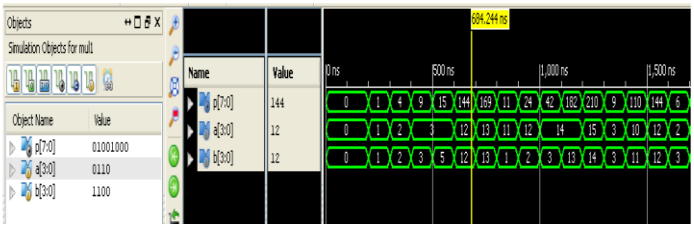


Figure 7: Output of multiplier

VII. CONCLUSION

A new gate called TPS gate is proposed and a 4×8 multiplier is synthesized using this gate. The gate is implemented with CMOS transistors and various performance parameters such as gate count, quantum cost, and numbers of garbage outputs are measured for the multiplier. A comparison of these parameters with the available reversible multiplier circuits shows that the proposed multiplier realized with TPS gates gives optimum values of these parameters. This work also presents a design-for-testability technique for testing stuck-at and missing-gate faults.

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