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Unsigned Array Multiplier Design Using Reversible Logic

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A B S T R A C T

The major problem of designing any circuit is the consumption of more power which can be optimized by using reversible logic gates. The computation of circuits using reversible logic is one of the innovative methods to optimize or reduce the consumption of power. An Array Multiplier is proposed in reversible logic using reversible gates. Array multiplier is computer simulated in Verilog HDL using EDA tool Vivado 2018.3. The multiplier is optimized either with respect to quantum cost, reversible logic gate counts, constant inputs and garbage outputs.

Keywords:Array multiplier, Reversible Logic Gates, Garbage Outputs, Quantum Cost, Constant Inputs.

1. Introduction

As many electronic devises are crowded in smaller and smaller area and clocked in higher and higher frequencies, a circuit generates more and more heat. As a result, at least three concerns arise:

- Money is spent on energy.
- The batteries in portable systems run out.
- The systems become overheated.

When a computer system erases a bit of data each time it performs a logic operation, it is referred to as "irreversible."

As a result, today's computers erase a bit of information inefficiently, resulting in substantially more heat being dissipated for each bit eliminated.

The conventional irreversible logic gates such as the NOR gate, AND, OR gate, NAND, XOR and XNOR gate in which 2 bits of input state are mapped to 1bit of the output state. This results in erasure of 1 bit of data and thus impossible to trace the input from the output. This led to the emergence of Reversible Logic computations.

To eliminate the heat dissipation, two inputs are mapped out to two outputs, allowing inputs to be distinctly retrieved from outputs, gate is considered reversible in these cases. It is proving to be a viable option because they do not allow feedback.

Reversible gates have their inputs and outputs in a one-to-one relationship, that is each individual input has a separate output assignment. As a result, the input combinations as well as output combinations in reversible gate can be uniquely defined. A reversible gate must have the same counts of input combinations and output combinations so as to function as reversible logic. Bennett demonstrated that when a network is constructed using reversible gates, power dissipation is 0 under perfect physical conditions. Reversible circuits allow circuit elements to be reduced to atomic size and packaging density to be increased.

The limitations of reversible logic computing are fan-out and feedback, the input combinations are supposed to be distinctly derived using the given output combinations. The performance factors for constructing an efficient reversible circuit are reversible gate count (GC), amount of constant inputs (CI), garbage outputs (GO), total quantum cost (QC), and latency.

The reversible network considers various specifications like amount of reversible gates used, constant inputs, quantum cost and garbage outputs. The reversible logic computations have a wide range of practice in, Nanotechnology, low power Complementary Metal Oxide Semiconductor (CMOS), DSP, DNA computation, Communication, Quantum computation, Cryptography, Optical computing and Filter design [10][11].

2. Literature Survey

A 4-bit array multiplier is designed using the fig 3 from [5] and block diagram from [6]. The irreversible block diagram was changed to reversible by using the reversible gates. Quantum cost is equal to 128, total 28 reversible gates are used, garbage output is 52 and constant input is 28 were obtained. This design was extended to 8-bit design.

The Quantum cost of reversible logic gates used are shown in table 1.

Table 1 – Quantum Cost of Reversible Logic Gates

Gates [Reference]	Number of bits	Quantum Cost
Feymann [7]	2	1
Peres [7]	3	4
Fredkin [7]	3	5
Toffoli [7]	3	5
DPG [7]	4	6
HNG [7]	4	6
RMUX [8]	3	4
TR [9]	3	4

3. Reversible Logic

3.1 Basic Terminologies:

A gate is said to be reversible if every output has a unique pre image that is the number of input bits and the number of output bits should be equal.

i. *Quantum Cost:* It equals the overall cost of the circuit's basic gates. It is the cost of implementing the reversible circuit using the NOT and CNOT gates. Basically, the cost of the design in the specifications of a fundamental gate's part is assigned to it.

ii. *Constant Inputs:* Constant inputs are pairs of inputs that are fixed at a constant value of either logic zero or one for generating the specified logically defined function.

iii. *Garbage Outputs:*refers to the output that is neither an output utilized for further computations nor an input to another gate. Constant input + Input = Garbage output + Output

iv. *Reversible Logic:* A digital circuit with k outputs if there are k inputs. Each combination in the output is distinct from the input. This is referred to one to one mapping and can be depicted as k*k.

v. *Width of Reversible Gate:* The amount of output bits or the amount of input combinations of the gate.

vi. *Flexibility:* More functions can be realised using the reversible gates.

3.2 Reversible Logic Gates:

Reversible logic gates like Feymann, Peres, Toffoli, HNG, DPG, Fredkin, RMUX, TR.

i.Feymann Gate: 2x2 reversible gate having a Quantum cost equal to 1. Feymann gate is depicted in fig.1

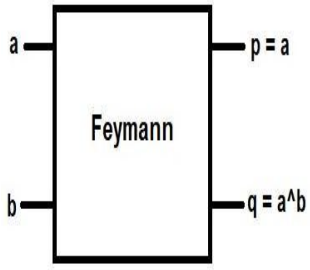

Fig.1. Feymann Gate

ii. Toffoli Gate: 3x3 reversible gate having a Quantum cost equal to 5. Toffoli gate is depicted in fig.2

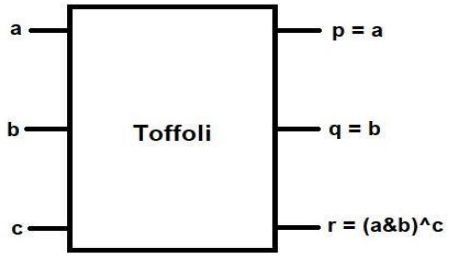

Fig.2. Toffoli Gate

iii. Peres Gate: 3x3 reversible gate having a Quantum cost of 4. It works as Half adder when c=0.The Peres gate is depicted in fig.3

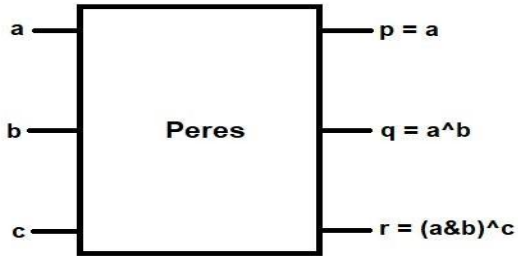

Fig.3. Peres Gate

iv. Fredkin Gate: 3x3 reversible gate having Quantum cost of 5. It works as a 2:1 Mux. The Fredkin gate is depicted in fig.4

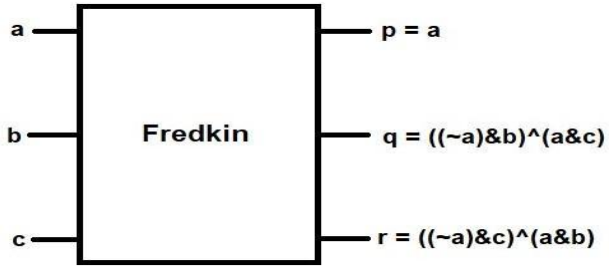

Fig.4. Fredkin Gate

v. HNG Gate: 4x4 reversible gate with quantum costequal to 6. It is implemented as FA when d=0. HNG gate is depicted in fig.5

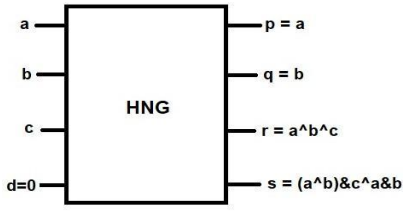

Fig.5. HNG Gate

vi. DPG Gate: 4x4 reversible gate with Quantum cost equal to 6. It works as FA when c=0. DPG gate is depicted in fig.6

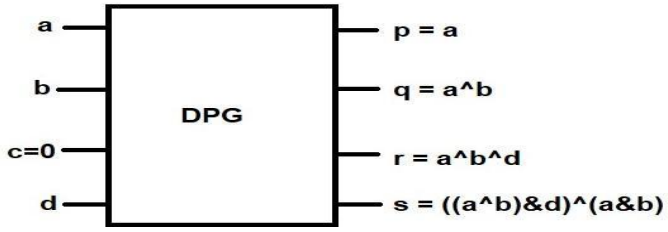

Fig.6. DPG Gate

vii.*TR Gate:* 3x3 reversible gate with a quantum cost equal to 4. TR gate is shown in fig.7

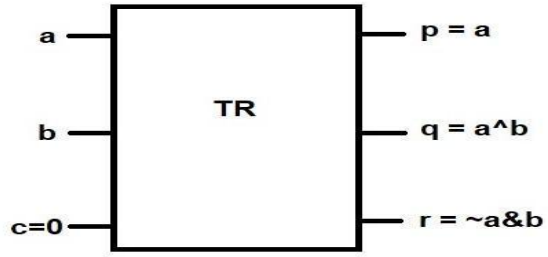

Fig.7. TR Gate

viii. RMUX *Gate:* 3x3 reversible gate with a Quantum cost equal to 4. RMUX gate is shown in fig.8

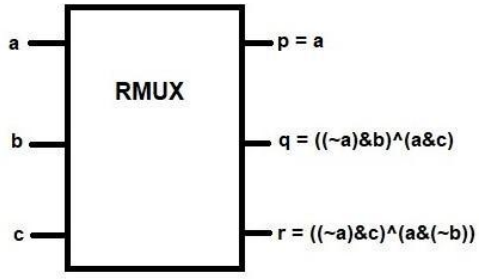

Fig.8. RMUX Gate

4. 8- Bit Reversible Multiplier

A binary multiplier is a digital or combinational logic circuit that multiplies two binary values. The two numbers are called multiplicand and multiplier, respectively, and the result is called a product. The bit size of the product is determined by the bit size of the multiplicand and multiplier. Performance of the multiplier depends on the number of multiplication operations performed per unit time.

Multipliers are mainly used in Digital signal processing applications such as in filter design, FFT computations …

The multiplication of 2 binary numbers will include a pair of intermediate products and an adder to sum of the partial products. To compute the intermediate products (which are 0 or the first number), left shift, and then add them together is how you find the product of two binary numbers (a binary addition, of course). It's a lot easier than the decimal system.

4.1. Array Multiplier:

An Array multiplier utilizes half adders to obtain the partial products and full adders to sum up these partial products. These partial products are shifted to left and then get summed up.

It has a conventional design methodology i.e., add shift algorithm approach. The multiplicand * the multiplier bit equals the partial product.

The addition is implemented using FA and HA, where the intermediate product is transitioned in accordance with their bit ordering, where AND gates are utilized for the product. In a n*n array multiplier, partial products are computed by n*n AND gates, and partial product addition is accomplished by n* (n – 2) FA and n HA.

Basic building block of this type of multiplier is a FA with 3 input vectors and 2 output vectors, which are implemented as a basic building block in the 8x8 array multiplier. The Least Significant Bit of intermediate product is the leftmost bit. The Most Significant Bit of intermediate product is the rightmost bit. Upon multiplication, partial products are now pushed to the left side and summed to obtain the final output product.

Sixty-four AND gates, eight HAs, and forty-eight FAs are required for an 8x8 array multiplier. Summation of all products is partial products, where a0, a1, a2, a3, a4, a5, a6, a7 and b0, b1, b2, b3, b4, b5, b6, b7 are Multiplicand and Multiplier, respectively. A product is the result of adding the partial products together.

A reversible array multiplier is designed as shown in fig.9 using 72 Peres gates and 48 HNG gates. This design has 120 reversible gates, 120 constant inputs, 576 Quantum cost and 232 garbage outputs.

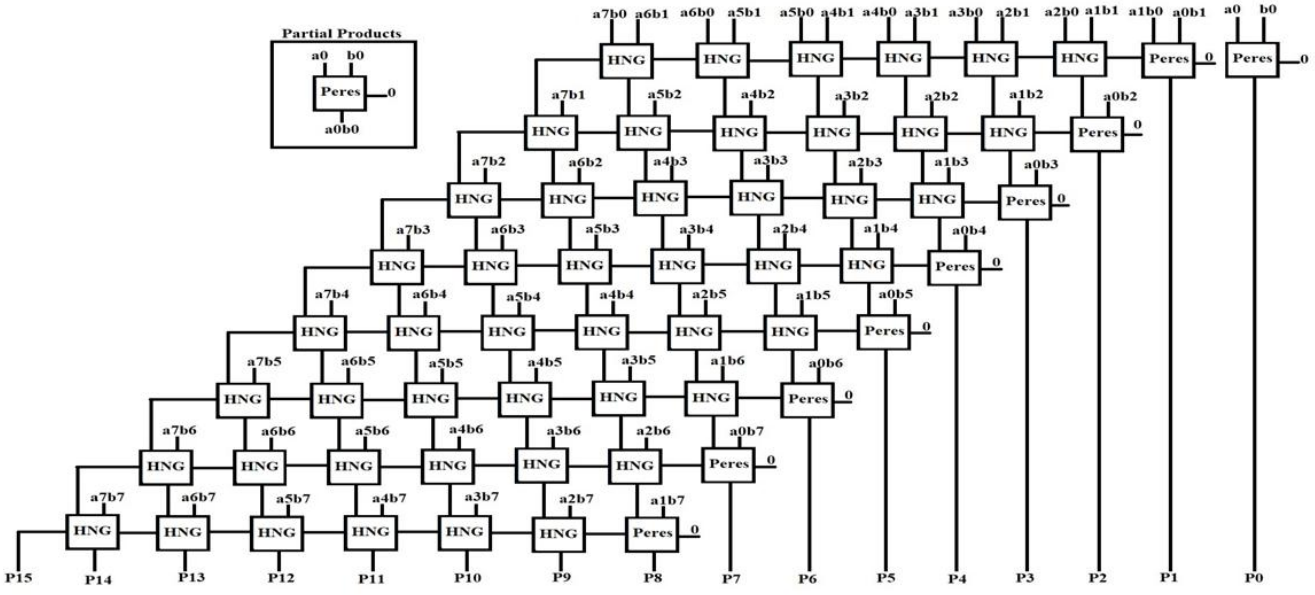

Fig.9. Array multiplier using HNG gates

5. Results and Simulations

By using Vivado 2018.3 the multiplier is designed, simulated and functionally verified by writing a test bench code.

5.1. Simulations

The waveforms generated for 8-bit array multiplier is as shown in fig.10.

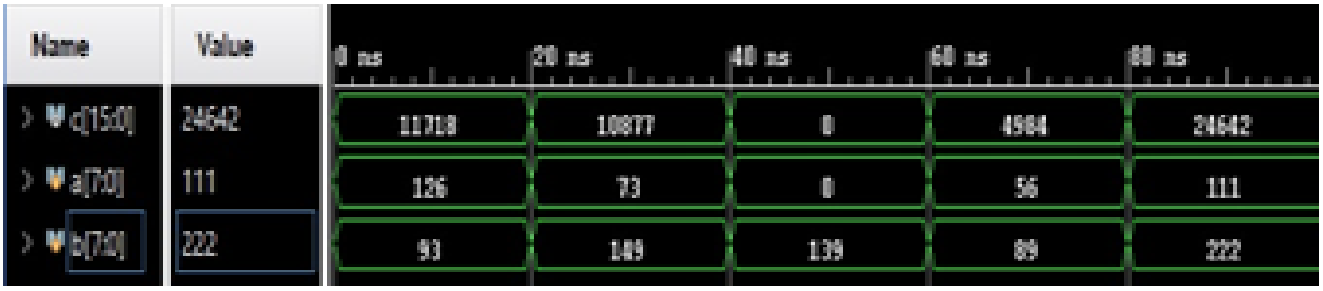

Fig.10. Simulation of Array multiplier

5.2. Results

Quantum Cost of Multiplier Designed: The Quantum cost, constant inputs, reversible gate counts and garbage outputs of the multiplier designed is depicted in table 2.

Table 2 - Specifications

Multipliers	Number of gates	Quantum cost	Constant inputs	Garbage output
Array	120	576	120	232

6. CONCLUSION

Here, 8-bit Array multiplier is constructed using reversible logic gates. Significant reduction of Quantum cost is achieved in the design.The multiplier can be used to design complex circuits like filters, digital signal processors, low power consumption circuits, high performance and high-speed processors.

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